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Electrical Performance of 4H-SiC MOSFETs with Different Gate Oxide Processes

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Abstract. This work investigates the impact of different gate oxide fabrication schemes on the electrical characteristics of 4H-SiC planar MOSFETs. Three processes with a target thickness of 50 nm were implemented: (1) thermal oxidation with NO annealing at 1350°C (actual thickness: 52 nm), (2) ALD-grown oxide with NO annealing at 1250°C (actual thickness: 43 nm), and (3) a stacked 20 nm thermal/30 nm ALD oxide structure with NO annealing at 1250°C (actual thickness: 47 nm). Electrical characterization included I_dV_g, CV, and I_gE_{ox} measurements.
Results show that Condition 1 exhibits the lowest leakage and best uniformity, and demonstrates strong oxide integrity without soft breakdown events. In contrast, Condition 2 and 3 show increased leakage, higher variability, and evidence of soft breakdown, suggesting greater interfacial weakness likely due to incomplete passivation of ALD-related defects at the lower annealing temperature. However, a surprising trend was observed in the CV analysis: Condition 2's flat band voltage (V_{FB}) is closest to the ideal 0V, indicating a lower fixed charge density than Condition 1 [1], which has the most negative V_{FB} (≈ -2V). The hysteresis results further highlight differences, with Condition 3 showing the largest hysteresis window (ΔV_{th}=0.13V).
These findings suggest that while the ALD process coupled with a lower-temperature NO anneal (Condition 2) can effectively reduce fixed charges, it does not fully eliminate interfacial defects responsible for increased leakage and soft breakdown. Our results underscore the complex trade-offs in different fabrication schemes, emphasizing that careful interface engineering beyond conventional NO annealing is required to ensure reliable performance in SiC MOSFETs.

Introduction

Wide bandgap semiconductors such as 4H-SiC have enabled significant progress in high-power and high-temperature electronics, offering advantages in efficiency and miniaturization compared to traditional Si devices [2]. However, the performance and reliability of SiC MOSFETs remain constrained by the quality of the gate oxide and the SiC/SiO_2 interface. Unlike Si MOSFETs, where decades of process optimization have led to highly controlled interface states, the SiC/oxide system still suffers from high interface trap density (D_{it}), charge trapping, and threshold voltage instability.
While thermal oxidation followed by nitric oxide (NO) annealing remains the industrial standard [3], alternative approaches such as atomic layer deposition (ALD) or composite dielectric stacks are actively investigated [4]. These three specific schemes, thermal, ALD, and stacked oxides were selected in this study to compare the trade-offs between the superior interface quality of high-temperature thermal oxides, the low-temperature deposition benefits of ALD, and the potential synergistic effects of a combined stack. Each oxide scheme affects key device parameters such as threshold voltage (V_{th}), leakage current, channel mobility, and long-term reliability. Therefore, systematic evaluation of different oxide processes is critical for advancing SiC MOSFET performance.

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This work investigates three gate oxide formation schemes applied to lateral n-channel 4H-SiC planar MOSFETs. Both capacitance voltage (CV) and current voltage (I_dV_g) characteristics were measured to capture interface-related effects such as hysteresis and trap activity, in addition to standard parametric testing of leakage and breakdown reliability.

Experimental

The baseline process flow for lateral n-channel 4H-SiC MOSFETs is shown in Figure 1. Only the gate oxide formation step differs among the three experimental conditions:

- Condition 1: 50 nm thermal oxidation + NO annealing at 1350°C for 1 hr (actual thickness: 52 nm).
- Condition 2: HF surface clean + 50 nm thermal ALD + NO annealing at 1250 °C for 1 hr (actual thickness: 43 nm).
- Condition 3: 20 nm thermal oxidation + 30 nm ALD + NO annealing at 1250 °C for 1 hr (actual thickness: 47 nm).

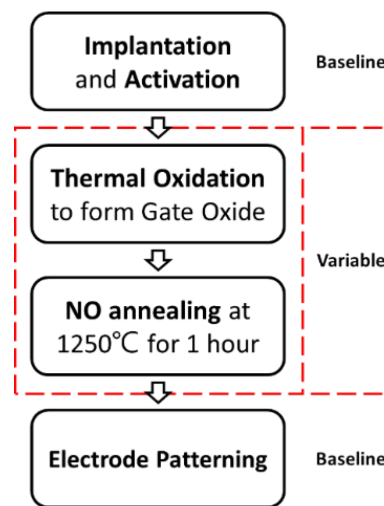


Fig. 1. Baseline thermal oxidation process flow after implantation and activation.

Electrical characterization:

- CP testing: threshold voltage (Vth), leakage (IDSS), and body diode forward drop (VSD). Good die rate was defined as the % of dies falling within median ± 3σ.
- IdVg sweeps: measured with Vd fixed at a small bias, gate bias swept forward/reverse. Vth extracted at Id = 1×10^{-5} A. Hysteresis window defined as ΔVth between sweeps.
- CV sweeps: small-signal AC capacitance measurement across accumulation and inversion, forward/reverse bias. Frequency dispersion and stretch-out analyzed for trap effects.
- IgEOX test: oxide integrity verified by gate leakage breakdown measurement.

Results and Discussion

Electrical Properties

Tables 1 and 2 summarize statistical results.

- Condition 1 shows the highest V_{th} (2.49 V), lowest leakage (I_{DSS}: 6.1E-5 A), and best uniformity.
- Condition 2 and 3 demonstrate comparable V_{SD} but increased leakage and higher σ, suggesting greater variability.

These differences indicate that ALD-based oxide processes may introduce additional interfacial issues not fully addressed by conventional NO annealing. Furthermore, the variations in V_{th} and leakage across these schemes are expected to influence the carrier mobility and channel resistance. While not directly measured here, the increased variability in Condition 2 and 3 potentially stems from a higher density of near-interface traps (N_{it}) which can enhance Coulomb scattering, thereby impacting the overall MOSFET conduction performance.

Table 1. Gate oxide thickness and error for Each Gate Oxide Process Condition.

Experiment	Condition 1		Condition 2		Condition 3	
Ideal = 50 nm	Measure	Error	Measure	Error	Measure	Error
Thickness (nm)	52	4.0%	43	14.0%	47	6.0%

Table 2. Summary of Electrical Performance and Yield for Each Gate Oxide Process Condition.

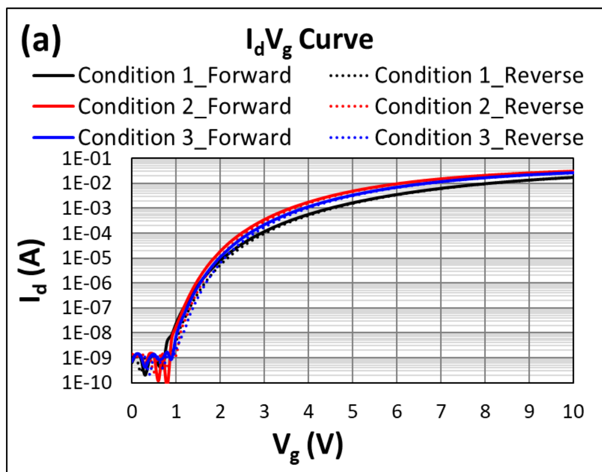
Experiment	Condition 1		Condition 2		Condition 3	
Item	Median	$Rate_{Good\ die}$ / STDEV	Median	$Rate_{Good\ die}$ / STDEV	Median	$Rate_{Good\ die}$ / STDEV
V_{th} (V)	2.49	**100.0%** / 0.06	2.13	**100.0%** / 0.06	2.28	**97.2%** / 0.10
IDSS (A)	6.1E-05	**100.0%** / 6.00E-05	1.0E-04	**88.9%** / 1.10E-03	2.9E-04	**83.3%** / 1.70E-03
V_{SD} (V)	3.42	**100.0%** / 0.04	3.24	**100.0%** / 0.04	3.24	**100.0%** / 0.04

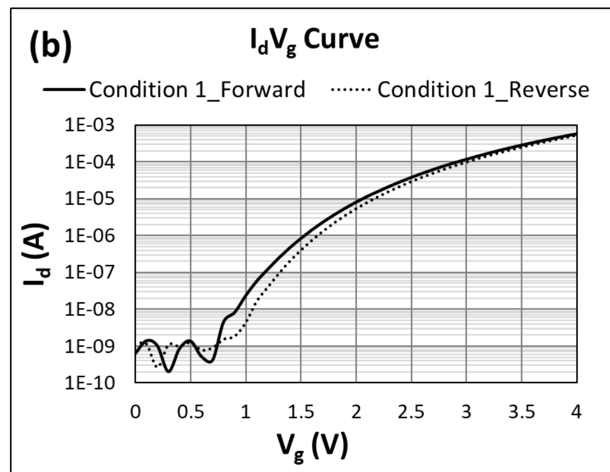
I_dV_g Characteristics and Hysteresis

Representative I_dV_g curves for the three conditions, measured at a drain bias of V_{DS} = 0.1 V, are shown in Figure 2. All devices exhibit complete channel switching behavior. Extracted hysteresis windows are:

- Condition 1: ΔVth = 0.10 V
- Condition 2: ΔVth = 0.11 V
- Condition 3: ΔVth = 0.13 V

Although all shifts are relatively small, the trend clearly indicates that Condition 3 has more active trap states, consistent with its stacked oxide scheme [4]. This increased hysteresis in the stacked structure may be attributed to a higher density of near-interface traps (N_{it}) and border traps, which are often formed at the transition interface between the thermal and ALD layers. Condition 1, with high-temperature NO passivation, shows the most stable switching characteristics, indicating effective reduction of shallow traps at the SiC/SiO_2 interface.





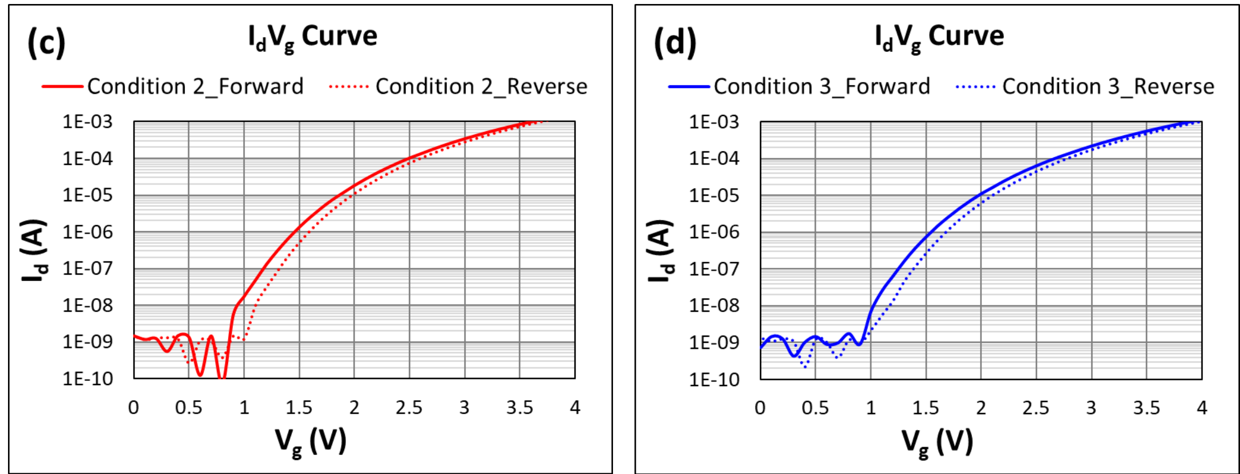


Fig. 2. (a) Forward and reverse I_dV_g curves for three conditions. (b) Curves for Condition 1. (c) Curves for Condition 2. (d) Curves for Condition 3.

CV Characteristics

Figure 3 shows the CV results measured on dedicated MOS capacitor structures, which reveals distinct electrical characteristics, directly correlated with the oxide layer properties.

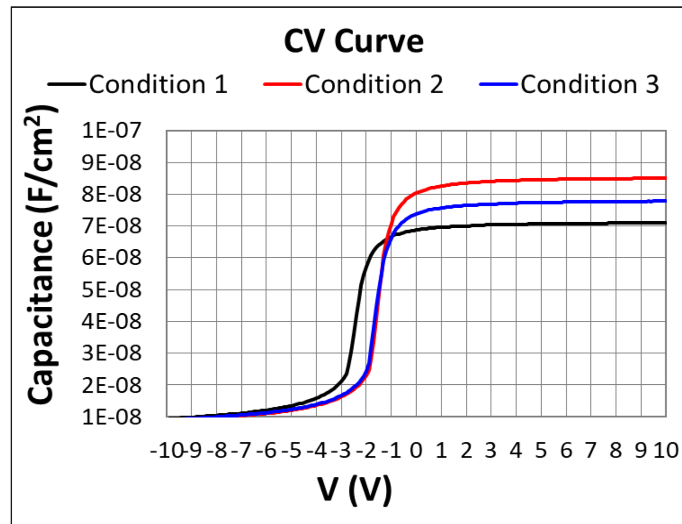


Fig. 3. CV Curves for 3 Conditions.

The accumulation capacitance (C_{ox}), measured at positive gate bias, inversely correlates with the oxide thickness. Our results show that Condition 2, with a measured thickness of 43 nm, exhibits the highest capacitance (8.5×10^{-8} F/cm^2). In contrast, Condition 1, at 52 nm, has the lowest capacitance (7.1×10^{-8} F/cm^2), and Condition 3, at 47 nm, falls in between (7.8×10^{-8} F/cm^2). This data confirms the expected relationship between oxide thickness and capacitance [5].

The flat band voltage (V_{FB}), a key indicator of fixed charge density, shows a surprising trend. The CV curve for Condition 2 is positioned closest to the ideal 0V ($V_{FB} \approx -1$V), suggesting it has the lowest positive fixed charge density among the three. Condition 1's curve is the most negatively shifted ($V_{FB} \approx -2$V), indicating a higher concentration of positive fixed charges, despite being a thermal oxidation process. Condition 3's V_{FB} is intermediate ($V_{FB} \approx -1.5$V). This suggests that the NO annealing process at 1250°C for the ALD film (Condition 2) is more effective at reducing fixed charges than the 1350°C NO annealing for the thermal oxide (Condition 1). The lower fixed charge in Condition 2 may be attributed to reduced thermal-induced stress compared to the 1350°C process.

In conclusion, while Condition 2 demonstrates the lowest fixed charge density and highest capacitance due to its thinner film, its interface quality is not optimal [6]. This is evidenced by the increased frequency dispersion and stretch-out observed in the CV characteristics, pointing to a higher

density of interface traps (D_{it}) in the ALD-based samples. Conversely, Condition 1 and Condition 3 show better interface quality but suffer from higher fixed charge densities. These results highlight the complex trade-offs between different fabrication processes in achieving optimal electrical properties for MOS devices.

Oxide Reliability (I_gE_{OX})

Figure 4 compares the gate leakage and breakdown characteristics of the three process conditions.

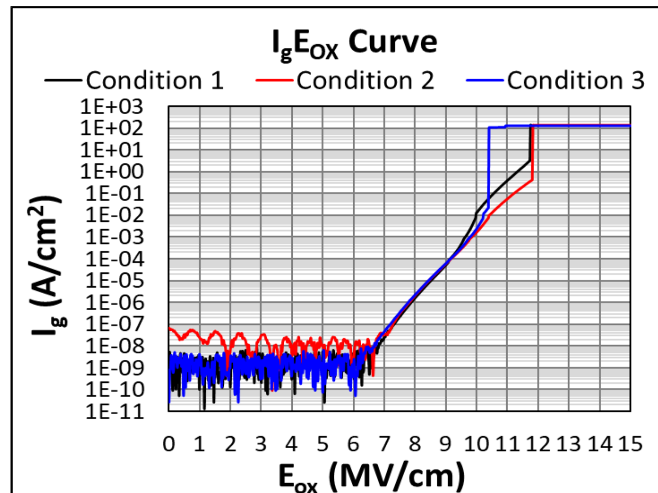


Fig. 4. I_gE_{ox} Curves for 3 Conditions.

An examination of the initial leakage current reveals a distinct difference. At low electric fields, Condition 2 exhibits a slightly higher initial leakage current compared to Conditions 1 and 3. This observation strongly suggests that defects are present not only within the bulk of the pure ALD film but, more importantly, at the direct interface between the ALD layer and the SiC substrate. Such an interface, formed without an intervening thermal oxidation layer, may contain a higher density of dangling bonds and defects that act as easy pathways for current, even under low-stress conditions [7]. Specifically, the interface chemistry of ALD films on SiC often suffers from residual carbon clusters or sub-oxides (e.g., SiO_x) formed during the initial deposition stages, which are not effectively removed by the 1250 °C NO anneal.

The breakdown behavior also highlights the critical role of the interface. Condition 3, which combines a thermal oxide layer with an ALD layer, shows the weakest performance, experiencing a hard breakdown at a relatively low electric field of approximately 10 MV/cm. This premature failure can be attributed to the combined effects of defects from both processes, creating a vulnerable interface at the junction of the thermal oxide and ALD layers, leading to an early breakdown.

In contrast, while the pure thermal oxide in Condition 1 and the pure ALD film in Condition 2 ultimately fail at a higher electric field, their breakdown characteristics differ. Condition 2's curve is notably smooth and free of significant steps, indicating a high-quality, uniform dielectric with superior integrity. Condition 1, however, shows several soft breakdown events sudden increases in leakage current before its final hard breakdown. Despite these soft breakdown events, the ultimate hard breakdown voltage for both Condition 1 and 2 is remarkably close, both occurring around 11.5 to 12 MV/cm. The soft breakdown events in Condition 1 and the increased leakage in Conditions 2 and 3 likely stem from localized defect-assisted tunneling. In the ALD-based samples, this is intensified by the high density of near-interface traps (N_{it}) that facilitate trap-assisted tunneling (TAT) at lower fields, acting as precursors to breakdown.

Summary

This study systematically compared three gate oxide schemes in 4H-SiC planar MOSFETs, revealing nuanced trade-offs in their electrical performance.

- Condition 1 (thermal + high-temp NO): This scheme demonstrates the best overall device uniformity and lowest leakage current. The I_gE_{ox} curve confirms its superior dielectric integrity, showing no soft breakdown events. However, its CV curve is the most negatively shifted, indicating the highest concentration of positive fixed charges among the three.
- Condition 2 (ALD + low-temp NO): While this process results in the highest capacitance and the most ideal flat band voltage (V_{FB} closest to 0V), it exhibits slightly higher initial leakage and shows evidence of increased trap activity. This suggests that while the low-temperature NO anneal effectively passivates fixed charges by reducing thermal stress, it is not sufficient to fully mitigate the near-interface traps (N_{it}) and carbon-related defects responsible for gate leakage and soft breakdown.
- Condition 3 (stacked thermal/ALD + low-temp NO): This stacked structure demonstrates the weakest oxide reliability, with the earliest hard breakdown and the largest hysteresis window (ΔV_{th}), pointing to the highest trap activity likely at the stacked oxide interface.

In conclusion, our results highlight that no single process provides a clear advantage across all electrical metrics. While ALD-based approaches offer flexibility for future scaling, achieving stable and reliable performance requires dedicated interface engineering to address both fixed charges and trap-assisted conduction mechanisms. Future work should explore optimized pre-cleaning, alternative passivation chemistries, or modified stack architectures to improve the reliability of ALD-based gate oxides.

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