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# Impact of ALD Oxidant and Deposition Temperature on Electrical Characteristics of $Al_2O_3/SiO_2/SiC$ MOS-Capacitors

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**Keywords:** 4H-SiC MOS capacitors, MOSFET, bilayer gate dielectric, $Al_2O_3/SiO_2$ stacks, atomic layer deposition (ALD), oxidant chemistry, flat band voltage shift, conduction mechanisms, interface trap density, dielectric strength, high electric field barrier suppression.

**Abstract.** The increased demand for SiC power MOSFETs requires gate dielectrics with low defect densities and high reliability under high electric field and temperature conditions. In this work, we examine how oxidant chemistry and deposition temperature affect the electrical properties of $Al_2O_3/SiO_2$ bilayer dielectrics formed in n-type 4H-SiC MOS capacitors. These structures consist of a thin $SiO_2$ interfacial layer, over which $Al_2O_3$ is deposited via ALD using three different oxidants at a temperature of 150–350°C. Electrical characterization shows that the choice of oxidant influences the flat band voltage shift and leakage current density, with a process-dependent trade-off between optimizing each parameter. These findings highlight that precise control of oxidant chemistry during ALD is essential for balancing flat band voltage stability with leakage suppression, and that multilayer-specific conduction models are critical for accurately predicting high electric field leakage characteristics in advanced SiC gate stacks.

## Introduction

Silicon carbide (SiC) has emerged as a leading wide-bandgap semiconductor for high-voltage and high-power electronic devices due to its large critical electric field (~3 MV/cm), high electron saturation velocity (~$2 \times 10^7$ cm/s), and superior thermal conductivity (~3.7 W/cm·K) [1, 2]. These intrinsic material properties enable the fabrication of compact devices with reduced specific on-resistance and enhanced efficiency compared to silicon-based power devices [3]. A unique advantage of SiC compared to other wide band gap materials is its ability to form a silicon dioxide ($SiO_2$) through thermal oxidation, enabling the development of SiC MOSFETs with a well-established dielectric system [4]. Thermally grown $SiO_2$/SiC interfaces currently exhibit the lowest interface state density ($D_{it}$) among alternative dielectrics on SiC [5]. However, the $D_{it}$ at the $SiO_2$/SiC interface remains one order of magnitude higher than that of conventional $SiO_2$/Si interfaces, leading to mobility degradation, threshold voltage instabilities, and long-term reliability concerns [6–7, 15].
Furthermore, the reliance on $SiO_2$ as a gate dielectric in SiC-based devices constitutes a fundamental limitation that hinders the full exploitation of SiC's superior intrinsic properties. Due to the relatively low dielectric constant of $SiO_2$ ($\kappa \approx 3.9$), nearly 2.5 times smaller than that of 4H-SiC ($\kappa \approx 9.7$), a significant portion of the applied bias drops across the oxide rather than the semiconductor, resulting in elevated electric fields within the dielectric [5, 15]. To address this imbalance, high-κ dielectrics have been widely investigated. High-k dielectrics offer several advantages: their higher dielectric constant reduces the equivalent oxide thickness (EOT) while lowering the electric field in the dielectric for a given applied voltage [8, 15]. The significant advantages of using aluminum oxide ($Al_2O_3$) are its large bandgap, the large band offsets to SiC, and the high breakdown electric field compared to other high-k dielectrics. [8]. Nevertheless, the direct deposition of high-k dielectrics on SiC surfaces typically introduces higher defect densities than thermal $SiO_2$, mainly due to dangling bonds, oxygen vacancies, and interface reaction products formed during deposition [9, 16]. These

interfacial traps cause charge trapping/detrapping dynamics, manifesting as detrimental threshold voltage shifts in MOSFETs.

A promising strategy to mitigate these challenges uses hybrid gate stacks, where a thin interfacial $SiO_2$ layer (1–2 nm) is thermally grown on SiC, followed by deposition of a thicker high-k dielectric such as $Al_2O_3$ by atomic layer deposition (ALD) [6, 9]. This stack architecture leverages the superior interface quality of $SiO_2$ with the enhanced dielectric properties of $Al_2O_3$. However, introducing an additional $SiO_2$/high-k interface creates another potential defect plane, and its structural and electrical properties are strongly influenced by ALD process conditions such as oxidant chemistry**,** precursor reactivity**,** and deposition temperature. For instance, oxidants can significantly alter the defect density and chemical bonding at the interface, while deposition temperature dictates the film's density, hydroxyl incorporation, and stoichiometry [10–12]. In addition to interface quality, understanding the conduction mechanisms governing leakage currents is critical for assessing dielectric robustness. Several leakage pathways are typically observed in SiC MOS capacitors with high-k or hybrid dielectrics, including Schottky emission (SE)**,** Poole–Frenkel emission (PFE)**,** trap-assisted tunneling (TAT), and Fowler–Nordheim (FN) tunneling [13, 14]. The dominant leakage mechanism can be extracted by analyzing temperature-dependent leakage current measurements and fitting the respective conduction mechanism models, providing insights into trap distributions and dielectric reliability.

In this work, we systematically study the influence of different ALD oxidants (like $O_2$-plasma, water, Ozone) and deposition temperatures on the dielectric properties of $Al_2O_3/SiO_2$/SiC stacks, and examine the conduction mechanisms responsible for the observed leakage currents. The breakdown electric field, leakage current density, and conduction mechanisms are analyzed to assess capacitors.

## Experimental Methods

Metal–oxide–semiconductor capacitors (MOSCAPs) were fabricated on n-type 4H-SiC substrates with a 2 nm $SiO_2$ interfacial layer. A 20 nm $Al_2O_3$ film was deposited by ALD using trimethylaluminum (TMA) as the aluminum precursor and three different oxidants (A, B, C), with deposition temperatures between 150°C and 350°C. Following dielectric deposition, a 10 nm TiN layer was deposited by reactive sputtering under ultra-high vacuum to serve as the gate electrode. Then, post-deposition annealing at 480°C for 1 min in an argon ambient was performed, which kept the $Al_2O_3$ film in an amorphous state. The electron-beam evaporation of 10 nm Ti / 30 nm Pt circular pads (diameter varying from 100 to 200 μm) achieved final contact metallization through a precision shadow mask. Device isolation was performed via dry etching to define the active capacitor regions. A schematic of the test structure is shown in Fig. 1.

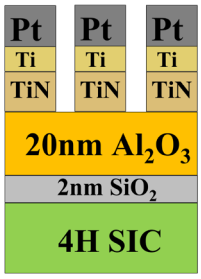


**Fig. 1.** Cross-section schematic of the fabricated MOS capacitor on n-type 4H-SiC with a 2 nm $SiO_2$ interlayer, 20 nm ALD-deposited $Al_2O_3$, TiN gate, and Ti/Pt contacts used for electrical characterization.

Electrical characterization employed a Keithley 4200A-SCS parameter analyzer. Capacitance Voltage (C–V) measurements were conducted in dual-sweep mode (from depletion to accumulation and vice versa) to assess the flat band voltage shifts ($\Delta V_{fb}$), using an AC modulation frequency of 100 kHz with an amplitude of 25 mV. Current–voltage (I–V) measurements were carried out over a bias range extending into accumulation until dielectric breakdown, with additional temperature-dependent I–V measurements performed from 25°C to 150°C to elucidate charge transport

mechanisms and thermal activation effects. The reported leakage current density (AVG J throughout the paper) and $\Delta V_{fb}$ represent the average value of five MOSCAP devices.

## Results and Discussions

When MOSCAPs on n-type 4H-SiC are biased in accumulation (at gate voltages higher than the flat band voltage ($V_{fb}$)), electrons from the SiC conduction band can be captured by interface traps or near-interface oxide traps at the $SiO_2$/SiC interface. In addition, carriers may tunnel through the gate dielectric and get trapped in bulk oxide traps within the dielectric layer [4, 17–19]. The capture of these negative charges perturbs the electric field distribution across the MOS structure, producing a positive $\Delta V_{fb}$, resulting in a shift of C-V characteristics. Such trapping is a critical reliability concern, as it can directly translate into threshold voltage instability in MOSFETs and degrade long-term device performance [8]. This trapped charge is often quasi-permanent due to a lack of minority charge carriers: the emission time constants of the responsible traps are much longer than the measurement timescale, strongly preventing detrapping during standard C–V sweeps [18, 20]. For thermally grown $SiO_2$ on 4H-SiC, the $\Delta V_{fb}$ magnitude is typically small ($\Delta V_{fb} \approx 0.8$ V in our measurements). Nevertheless, still quasi-permanent, as evidenced by subsequent sweeps reproducing the initial sweep's reverse branch (see Fig. 2). This behavior is consistent with deep electron traps possessing long emission time constants, e.g., with high emission activation energies, leading to incomplete detrapping within the experimental time window [17, 19, 21].

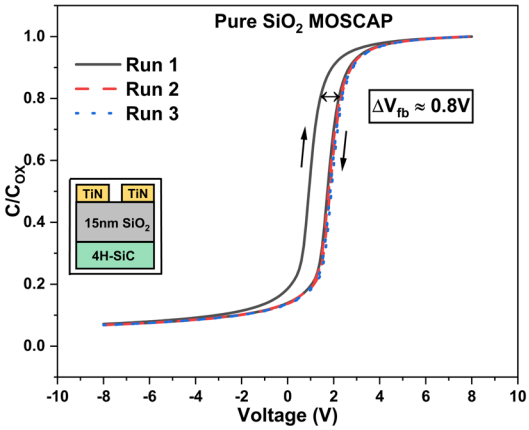


**Fig. 2.** Normalized capacitance-voltage characteristics of a 15 nm thick pure $SiO_2$ dielectric on 4H-SiC with a TiN top electrode, showing a 0.8 V positive $\Delta V_{fb}$ after three successive measurements. Arrows represent the direction of the sweep. Inset: schematic of the fabricated MOS capacitor test structure.

Incorporating a high-k dielectric such as $Al_2O_3$ can increase the observed $\Delta V_{fb}$ compared to pure $SiO_2$. The oxidant chemistry during ALD determines $V_{fb}$ stability among the other process parameters [10]. Our measurements for a fixed deposition temperature (Fig. 3) reveal that the leakage current density and the $\Delta V_{fb}$ vary significantly with the used oxidant. The $V_{fb}$ of the ideal MOSCAP is expected to be ~ 1 V due to the work function difference between the TiN electrode and the n-type 4H-SiC [22]. The difference in $V_{fb}$ observed during the initial upsweep between the MOSCAPs for different oxidants compared to the ideal expectation most likely arises from different amounts of fixed charges located at the interfaces or within the bulk of the $Al_2O_3$ layer [8, 14] (Fig. 3A). Oxidant C might act more aggressively on the interface since it causes the highest initial shift in the MOSCAPs. Furthermore, an additional offset in $V_{fb}$ can also stem from dipole formation at the high-k/$SiO_2$ interface, irrespective of the electrode material, as reported by Iwamoto *et al*. [22].
Furthermore, a much smaller $\Delta V_{fb}$ is observed in our MOSCAPs when oxidant A ($\Delta V_{fb} \sim 0.4$ V) is used compared to oxidants B and C ($\Delta V_{fb} > 2$ V) (Fig. 3A). The reduced $\Delta V_{fb}$ for oxidant A can be attributed to electron detrapping from bulk or near-interface traps and escaping to the top electrode during the measurement, reducing $\Delta V_{fb}$. This interpretation is based on observed higher leakage current characteristics for oxidant A compared to oxidants B and C (Fig. 3B), which indicate

enhanced pathways facilitating charge carrier transport in the $Al_2O_3$ film deposited using oxidant A. While no compromise seems evident for obtaining low $\Delta V_{fb}$ and low leakage current, a trade-off emerges: lowering the $\Delta V_{fb}$ can often lead to higher leakage current, and vice versa, solely by altering the oxidant chemistry [10]. For oxidants B and C, the influence of deposition temperature on the electrical performance of MOSCAPs is low (Fig. 4). In contrast, by using oxidant A, the MOSCAP exhibited a pronounced improvement in leakage characteristics and dielectric strength within the 200–250°C window, suggesting optimal film quality and reduced defect density in this regime. However, this temperature range did not coincide with the minimal $\Delta V_{fb}$ observed near 300°C (Fig. 4).

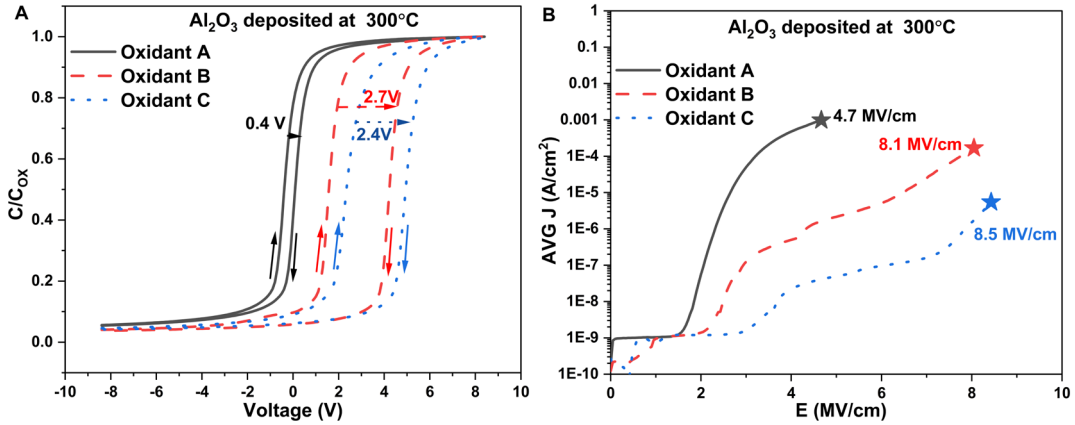


**Fig. 3.** A. Normalized capacitance–voltage characteristics of MOSCAPs with $Al_2O_3$, deposited with different oxidants (A, B, C). Numbers indicate the average $\Delta V_{fb}$ measured in the initial dual sweep (arrows indicate the sweep direction). B. Average leakage current density for $Al_2O_3$ films deposited with different oxidants (A, B, C) as a function of applied electric field. Stars and numbers denote the corresponding dielectric breakdown electric field strength ($E_{BD}$) of $Al_2O_3$ films for different oxidants.

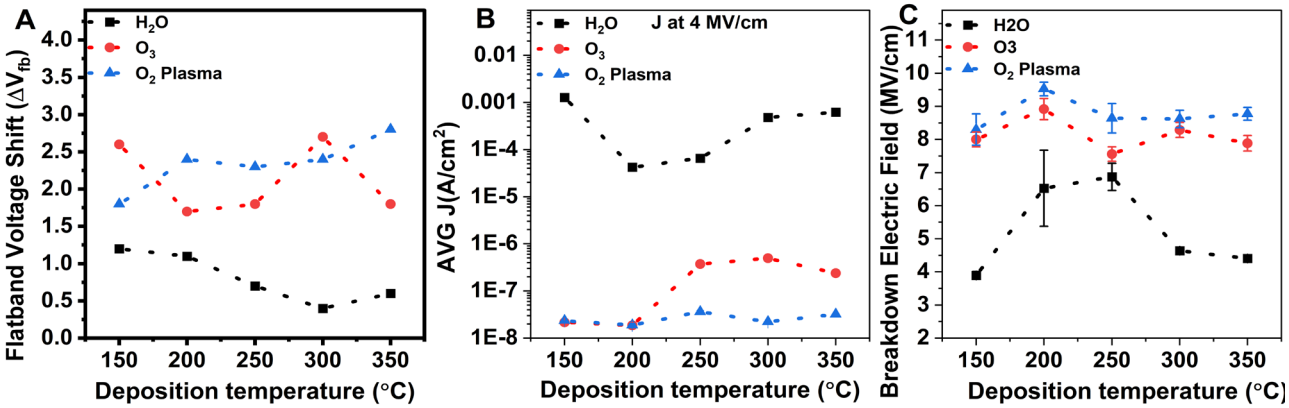


**Fig. 4.** A. Flat band voltage shift ($\Delta V_{fb}$), B. Average leakage current density at 4 MV/cm, and C. Breakdown electric field for $Al_2O_3$ films deposited using oxidants A, B, and C as a function of the deposition temperature in $Al_2O_3$ ALD deposition.

To further evaluate leakage behavior, temperature-dependent I–V measurements were performed on $Al_2O_3$ films deposited at 300°C using different oxidants (Fig. 5). Among the three, $Al_2O_3$ films deposited with oxidant A exhibited the highest leakage with minimal temperature dependence. In contrast, pronounced temperature sensitivity was observed when oxidants B and C were used, particularly beyond 5 MV/cm, where leakage current increased by nearly an order of magnitude between 25°C and 150°C. Simultaneously, the dielectric breakdown electric field decreased by approximately 3 MV/cm over the same temperature range. At low electric fields (< 2 MV/cm), the leakage current density approached the resolution limit of the parameter analyzer, preventing quantitative comparison. Notably, this low-leakage regime terminated at different electric field strengths for each oxidant, likely due to the initial $V_{fb}$ differences between the oxidants discussed previously. For example, in the case of oxidant C, the leakage onset occurred near 3 MV/cm (Fig. 5).

In the moderate electric field regime (2–5 MV/cm), leakage current exhibited a rather low temperature dependence. This suggests that thermally activated processes are less dominant in this range.

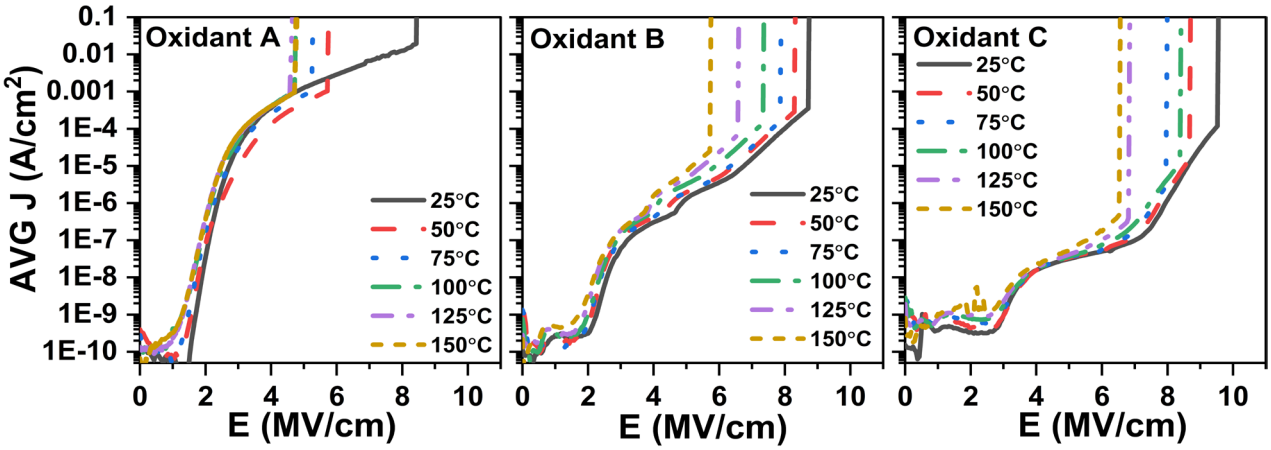


**Fig. 5.** Average leakage current density as a function of electric field for $Al_2O_3$ films deposited at 300°C using oxidants A, B, and C in ALD and measured at 25°C to 150°C.

To gain deeper insight into the underlying charge transport mechanism. We fitted the measured current using established conduction models with some free parameters to evaluate the conduction mechanism responsible for the observed leakage [13, 14, 23, 24]. The methodology for this calculation is detailed in [13]. This fitting procedure enabled the extraction of free model parameters. In the moderate electric field regime, the calculated current from the TAT model (analytical expression is mentioned in [23]) closely matched experimental data (see Fig. 6), confirming that TAT is the primary conduction mechanism under these conditions with the following argumentation. Since FN tunneling becomes significant only at high electric fields and PFE is highly temperature dependent, both mechanisms can be discounted as a major contributor. Electrode-limited SE can be ruled out as a major contributor due to the large conduction band offset between the $SiO_2$ interlayer and SiC. Moreover, since the electrode was the same in our experiments and using different oxidants during the deposition of $Al_2O_3$ produced distinct leakage current levels, SE can also be excluded as the primary mechanism in this electric field range [13, 24]. As a result, we attribute the leakage current in the moderate electric field regime mainly to TAT, which aligns with previous studies on high-k and $Al_2O_3$ gate stacks with $SiO_2$ interlayer [13, 14]. The extracted model parameters and calculated results for all three oxidants are shown in Fig. 6, offering quantitative insights into trap characteristics and how they depend on oxidant chemistry. According to the calculation results, the high leakage level for oxidant A is governed by the highest TAT trap density ($N_t$) for traps having an energy of 0.8 eV below the conduction band of the dielectric (Fig. 6A). The absolute $N_t$ values from our calculations might be underestimated by several orders of magnitude, as evidenced in the literature [23]. However, they indicate how the $N_t$ can vary by changing the oxidant chemistry during the ALD deposition.

At high electric fields exceeding 5 MV/cm, our MOSCAPs exhibit a pronounced increase in leakage current beyond a certain threshold at a given temperature when oxidants B and C are used, ultimately leading to dielectric breakdown as mentioned earlier. In this regime, none of the conventional conduction models in our simulations yielded physically reasonable parameter values across all tested mechanisms (SE, PFE, FN, TAT). Consequently, the applied models cannot meaningfully reproduce the leakage characteristics with their significant measurement temperature dependence. One plausible explanation is that most analytical formulations of conduction mechanisms are derived for single-layer dielectric systems. However, the gate stack in our experiments comprises a bilayer ($SiO_2/Al_2O_3$), where each dielectric has a different band offset relative to 4H-SiC. This structural complexity can significantly alter carrier transport, as carriers may experience sequential barriers and/or mixed conduction pathways not captured by single-layer models.

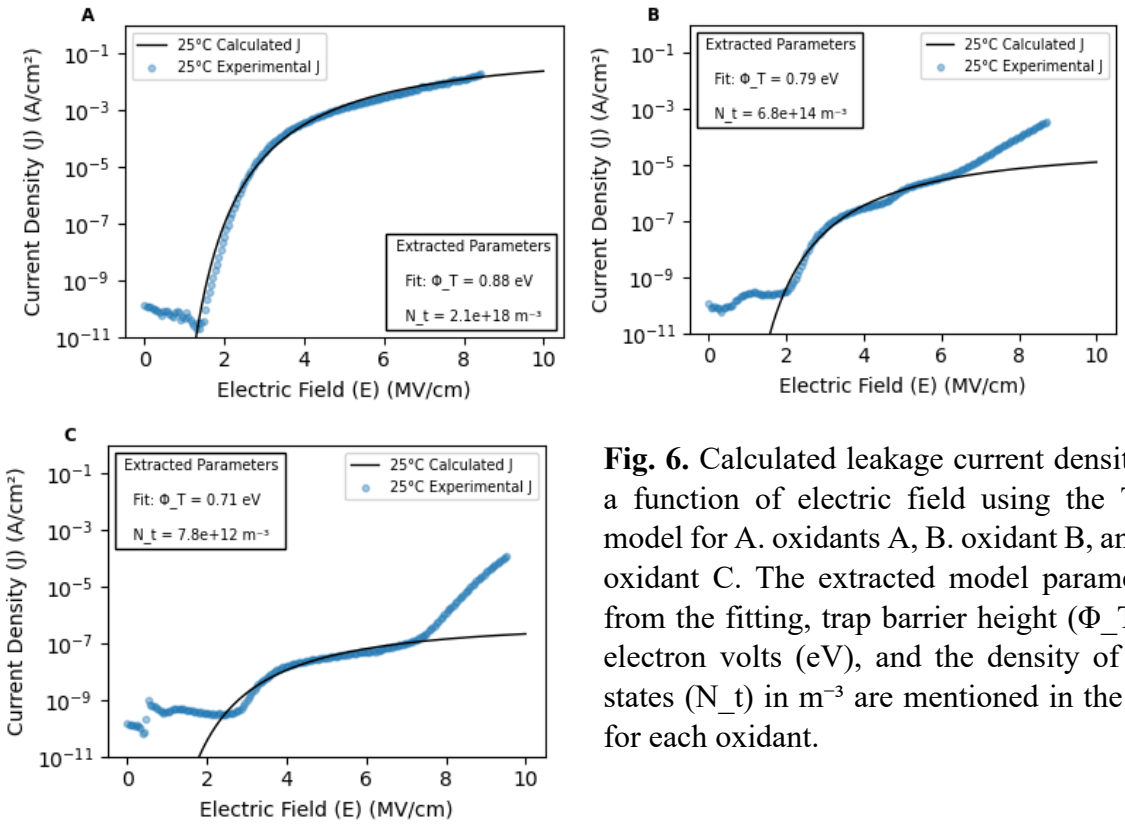


**Fig. 6.** Calculated leakage current density as a function of electric field using the TAT model for A. oxidants A, B. oxidant B, and C. oxidant C. The extracted model parameters from the fitting, trap barrier height (Φ_T) in electron volts (eV), and the density of trap states (N_t) in $m^{-3}$ are mentioned in the plot for each oxidant.

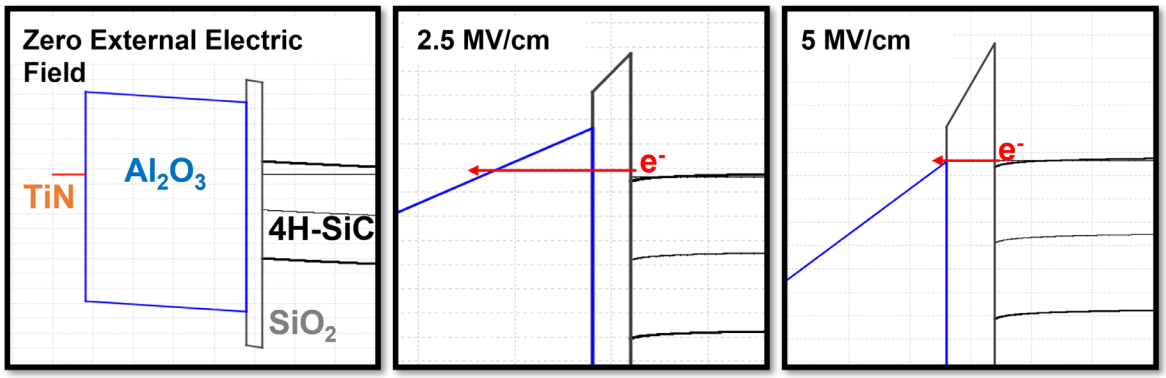


**Fig. 7.** Simulated energy-band diagrams of the $Al_2O_3/SiO_2$ bilayer dielectric stack on n-type 4H-SiC under zero external electric field and close-up at average electric fields of 2.5 and 5.0 MV/cm.

It is therefore plausible that the observed leakage might arise from a combination of bulk-limited and electrode-limited conduction processes, potentially involving multi-step tunneling or hopping conduction through defect states distributed across both layers [25]. Our band-diagram simulations (Fig. 7) show that at high electric fields (above ~5 MV/cm), the electric field-induced band bending becomes so pronounced that the $Al_2O_3$ barrier is almost completely suppressed, enabling enhanced carrier injection by direct tunneling through the 2nm $SiO_2$ layer. This could explain the increase in leakage after 5 MV/cm for oxidants B and C. However, our calculation approach was hindered by the lack of a simple analytical expression for direct tunneling through a trapezoidal barrier with a changing electric field. Furthermore, the observed significant temperature dependence of the leakage characteristic in the high electric field region for oxidants B and C may also indicate charge carrier transport through a combination of carrier injection and a bulk trap-related conduction mechanism with thermally activated processes.

**Summary**

This study investigates how oxidant chemistry and deposition temperature affect the electrical performance and leakage characteristics of $Al_2O_3/SiO_2$ bilayer gate stacks on n-type 4H-SiC MOS capacitors. Electrical tests with C–V and temperature-dependent I–V measurements show that oxidant chemistry greatly influences the $\Delta V_{fb}$ and leakage current density, with a trade-off between these factors. The impact of the deposition temperature was minimal. Trap-assisted tunneling is identified as the primary conduction process in the moderate electric field range, while Poole–Frenkel, Schottky emission, and Fowler-Nordheim tunneling are ruled out. At higher electric fields, simple single-layer dielectric models do not fully explain the leakage behavior, likely due to the complex band alignment of the bilayer system. Band diagram simulations reveal significantly high electric field barrier suppression in $Al_2O_3$, suggesting a combination of bulk- and electrode-limited conduction with thermally activated processes. These results emphasize the important role of oxidant chemistry in improving device reliability and highlight the need for modeling methods that consider multilayer dielectric stacks in SiC power electronics.

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