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Extraction of Trench Sidewall Capacitance by Linear Component Separation towards Wafer Level Evaluation

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Abstract. This work proposes a linear, area-based component separation method to extract an effective trench sidewall capacitance from C-V measurements of 4H-SiC UMOS capacitors. Devices were fabricated with two gate-oxide schemes LPCVD TEOS and low-temperature oxidation of LPCVD polysilicon and characterized by I-V and C-V measurements. Planar capacitors show breakdown strength above 9 MV/cm. Least-squares decomposition of layout-dependent capacitances enabled the separation of mesa, sidewall and bottom contributions. Additionally, this applying this approach revealed trench-pitch dependent depletion and larger wafer-level thickness variation for the polysilicon-oxidation flow. Reconstruction errors up to 20 % indicate that spacing-dependent depletion, corner curvature, fringe and field-oxide capacitances exceed the simple parallel-capacitor model.

Introduction

Reducing the on-state resistance ($R_{DS(on)}$) of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) remains a major driver for research and development. State-of-the-art SiC trench MOSFETs (UMOSFETs) reduce $R_{DS(on)}$ by increasing the channel width per unit area and lowering internal series resistance. Consequently, channel resistance becomes more dominant, and low channel mobility remains as a limiting factor for these devices. High channel resistance is mainly caused by the high density of interface traps (D_{it}) present at the SiO_2/SiC interface. Sophisticated optimization processes have been developed to reduce these interface traps. These include pre-oxidation etching in hydrogen atmosphere [1], high temperature oxidation, post-oxidation annealing in N_2 and NO [2,3], as well as the use of chemical vapor deposition (CVD) [1,2], low- pressure chemical vapor deposition (LPCVD) [3], and low-temperature oxidation of polycrystalline silicon [2]. Most of the processes have only been evaluated on planar MOS capacitors (MOSCaps) as the measurement and evaluation of D_{it} for the UMOS relevant trench sidewall is a challenge. Results from planar devices do not transfer to trench devices one-to-one due to different crystal orientations and the possibility of etch-induced interface modifications. In this work, we investigate the behavior of Trench MOSCaps (UMOSCaps) with gate oxides fabricated by LPCVD and low-temperature oxidation of undoped LPCVD polysilicon. We propose a method to extract an effective sidewall capacitance and an effective D_{it}, enabling qualitative comparison between gate-oxide fabrication methods. We also investigate the breakdown behavior of the gate oxides.

Device Fabrication

The MOSCap fabrication process Fig 1 (a) follows the processing of a SiC-UMOS closely [4]. The structure of the UMOSCaps is depicted in Fig. 1 b. To fabricate both samples an n-type epitaxy layer with a thickness of 12.79 ± 0.34 µm and a nitrogen concentration of $9.55*10^{15} \pm 0.34*10^{14}$ cm^{-3} suitable for 1.2 kV class UMOSFETs, was grown on commercial six inch 4H-SiC substrates. A 1.5 µm thick CVD SiO_2 hard mask was deposited and patterned by stepper lithography and structured

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by dry etching. Subsequently, SiC trenches with a target depth of 1.3 µm were etched using an ICP dry etching process described by Rusch et al. [5]. The trench depth was measured by structured illumination microscopy over the full wafer and was 1.23 ± 0.01 µm for sample 1 and 1.21 ± 0.01 µm for sample 2 (Fig. 1 (d)). A high-temperature H_2 reshape was applied to round the trench top and bottom corners, mitigating field crowding and premature gate-oxide breakdown [4]. Trench geometry was confirmed by focused-ion-beam (FIB) cross-section SEM measurement (Fig. 1 (c)). The measurement of 1.27 µm indicated that structured illumination microscopy underestimated the trench depth by approximately 50 nm. This difference between FIB-SEM and microscopy must be considered when using the optical measurement for further wafer level evaluation.

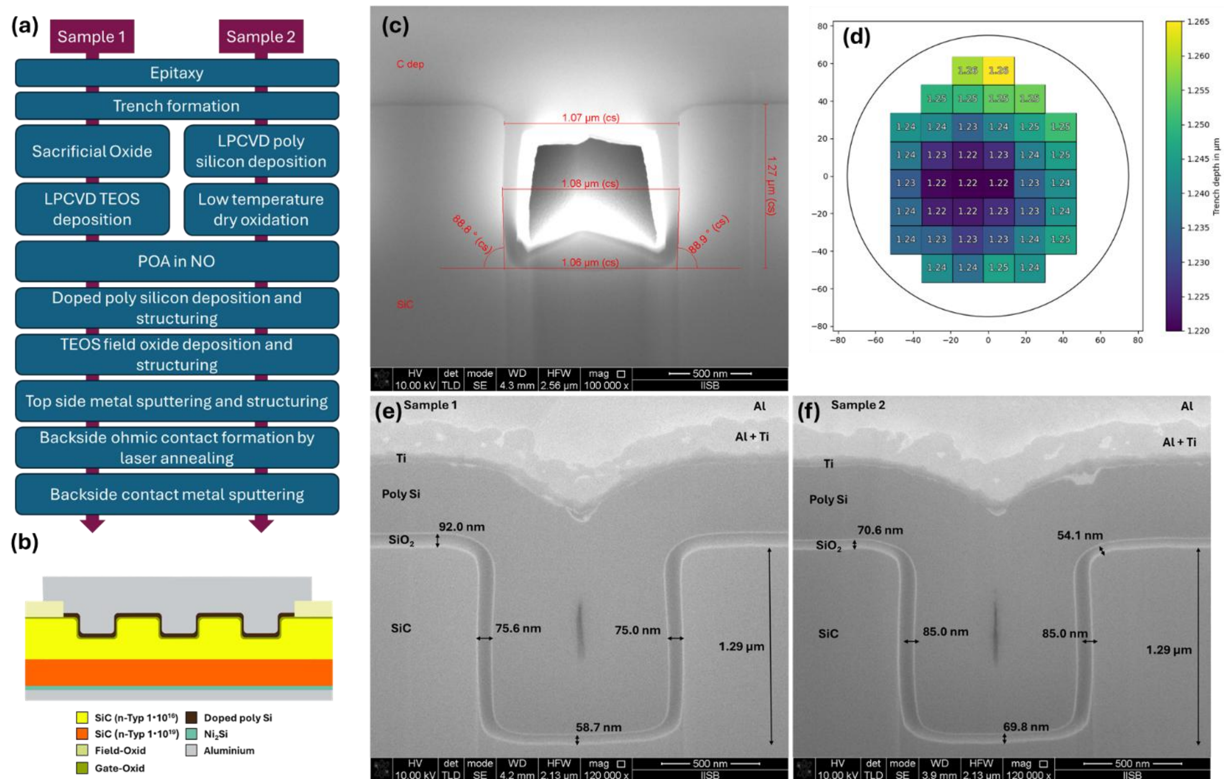

Fig. 1. a) Process flow for UMOSCaps. b) Schematic of fabricated devices. c) FIB-SEM cross-section of a 1 µm wide trench on sample 1 after trench reshape process. d) Wafer map of trench depth measured by structured illumination microscopy on sample 1. e) FIB-SEM cross-section of a final device on sample 1 (LPCVD TEOS oxide). f) FIB-SEM cross-section on a final device on sample 2 (oxidized LPCVD polysilicon).

Two approaches to form the gate oxide were used. For sample 1 a sacrificial oxide was grown after the trench reshape process and removed in buffered oxide etch. SiO_2 was then deposited by low pressure CVD at a temperature of 710 °C and a pressure of 0.133 mbar using TEOS as a precursor which was subsequently densified at 900 °C to form a layer with 87.7 ± 0.4 nm thickness [3]. For sample 2, undoped polysilicon with a thickness of 32.5 ± 0.4 nm was deposited and oxidized at 850 °C for 8 h in O_2 atmosphere. This process was based on a work reported by [2]. Both wafers underwent NO annealing at 1300 °C for 1 h; post-anneal oxide thicknesses were 94.5 ± 0.6 nm (sample 1 Fig. 1 (e)) and 66.6 ± 0.8 nm (sample 2 Fig. 1 (f)) measured by ellipsometry. In situ phosphorus-doped polysilicon was deposited by LPCVD as the gate electrode and patterned by dry etching to form pads of 1.0 mm^2, 0.5 mm^2, and 0.316 mm^2. A 600 nm TEOS oxide was deposited as a field oxide and contact windows were opened by dry etching. Frontside metallization consisted of 100 nm Ti and 3 µm Al sputtered onto the frontside and patterned. On the backside, a NiAl contact was sputtered and laser-annealed to form an ohmic contact to the SiC substrate, followed by Al backside metallization [6].

Results and Discussion

Breakdown Evaluation.

To evaluate the gate oxides, current voltage measurements (I-V) were done on 40 devices per design. The applied voltage was ramped from 0 V to 100 V and the measurement was stopped at a current compliance of 10 mA. Fig 2 (a) shows the averaged curves of the measurements. Because of the different gate oxide thicknesses of the two gate oxide processes and the variance in the oxide thickness on the trench sidewall, bottom and mesa (Fig. 1 (e) (f)) the current is plotted over the electric field on the trench mesa. To calculate this field the average oxide thickness on the wafer after NO annealing measured via ellipsometry is used (Sample 1 94.5 nm and Sample 2 66.6 nm). The planar designs show a high breakdown field of above 9 MV/cm for both gate oxides. Sample 2 shows an earlier onset of Fowler-Nordheim tunneling which might suggest a reduced oxide quality or additional thickness variation in the planar devices.

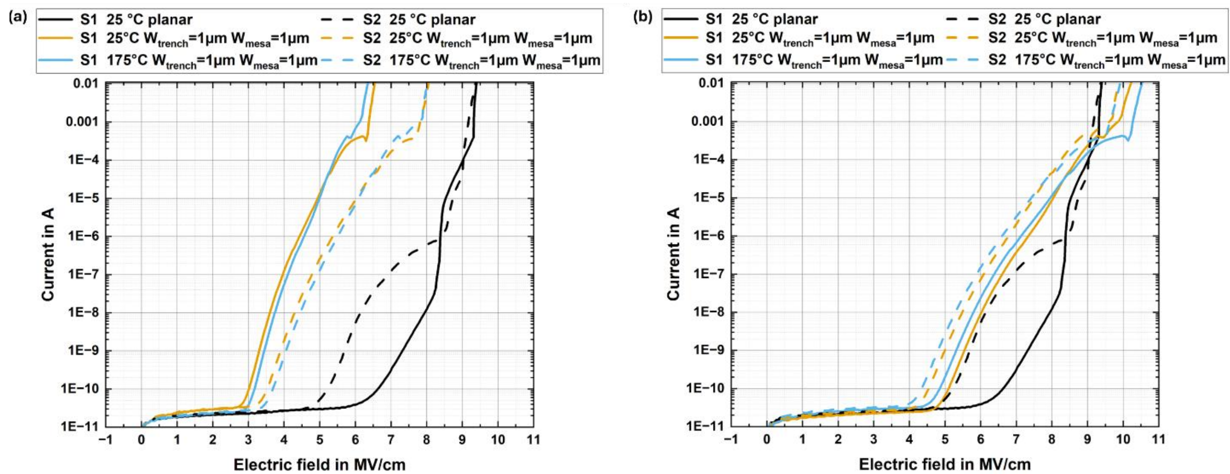

Fig. 2. Leakage current of planar and trenched devices at room temperature and for trenched devices at 175 °C. The electric field is calculated for a) the planar mesa top and b) for the planar devices in the mesa top and for the trenched devices in the smallest oxide thickness.

For the trench devices the breakdown electric field is significantly lower than for the planar devices. This is mainly caused by the difference in oxide thickness at the trench bottom and trench corners that can be observed for both sample 1 and sample 2. The electric field for the trench capacitors becomes closer to that of the planar devices when calculating with the lowest oxide thickness measured via FIB-SEM. For sample 1 this is the trench bottom with 58.7 nm and for sample 2 the top corner with 54.1 nm. However, the breakdown fields using this approach are slightly larger than for the planar devices which is not expected. This overestimation occurs because the simple calculation does not include field crowding effects that occur on the corners of the trench. Here, only one representative trench was measured by FIB-SEM meaning so it is also possible that even lower oxide thickness is present in the device. Moreover, for a given current value, the current density in the UMOSCap is lower than the current density in the planar MOSCap with identical metallization area.

Capacitance-Voltage measurements.

Full-wafer high-frequency capacitance measurements (C-V) at 100 kHz were performed at room temperature. Depicted in Fig. 3 (a) are the forward and backward capacitance curves for 40 devices on both samples for planar MOSCaps (Table 1, design 1) and UMOSCaps (Table 1, design 3), normalized with respect to the accumulation capacitance. No hysteresis can be observed regardless of design and oxide process. When comparing the absolute values of planar MOSCaps on sample 1 and sample 2, an increased spread of C_{ox} can be observed for the polysilicon oxidation process. Most likely this scheme yields a higher variation in layer thickness over the wafer than the TEOS process. For the planar devices the difference in flat-band voltage can be attributed to the different oxide thickness of both samples as well as different interface properties. For the trench devices, several

distinct slopes can be observed in depletion and weak inversion. This is particularly apparent for the devices on sample 2. The steeper slopes at approx. -6.2 V and -2.9 V are attributed to the different oxide thickness that occurs on the trench mesa, bottom and sidewall.

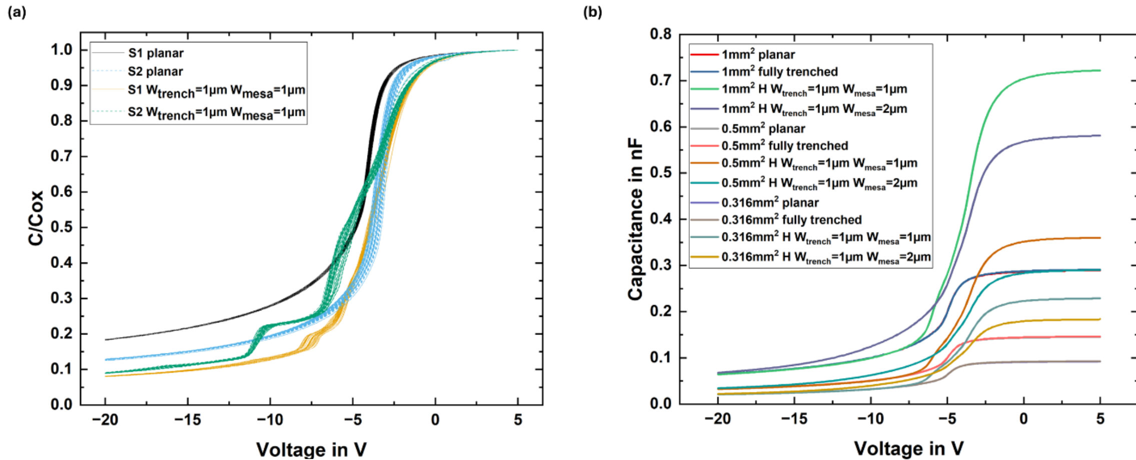

Fig. 3. a) Normalized capacitance-voltage measurements at 100 kHz for trenched and planar designs with 40 devices respectively and the two different gate oxide processes. b) Capacitance-voltage measurements at 100 kHz for all 12 different designs on one stepper field in the center of sample 1 (LPCVD TEOS oxide).

However, the steeper slopes at approx. -10.8 V (sample 2) and -7.7 V (sample 1) are caused by the extension of the space charge region into the trench sidewalls until the trench area is fully depleted and the space charge region starts to extend beyond the trench structure into the semiconductor [7]. This causes a change in effective capacitor surface area leading to in an abrupt reduction in capacitance. This effect is commonly used as the shielding effect in double UMOS transistors and is sensitive to the distance between two trenches [4]. Fig. 3 b) shows representative CV curves of the designs listed in table 1 on one stepper field in the center of sample 1.

Linear Component Separation.

In this work we expand on work reported by Lim [4], Banzhaf [7] and Guo et al. [8] which all investigated SiC UMOSCaps. The capacitance of a trench MOS capacitor is simplified to consist of three parallel capacitors: the capacitance on the top of the trench C_m, the trench sidewall C_s and the trench bottom C_b. The total capacitance C is the sum of these three contributions:

$$C(V) = A_m C_m(V) + A_s C_s(V) + A_b C_b(V). \qquad (1)$$

Here, A_m, A_s and A_b, represent the effective areas of the trench top, sidewall, and bottom, respectively. The knowledge about the effective areas allows for determination of the different capacitances by solving a linear system of equations. It is possible to extend this model by adding additional terms in case of significant corner rounding at the trench top and bottom, which has not been done in the scope of this work. A variation of the trench depth might be necessary to increase the accuracy of the method when trying to extract the influence of trench rounding. When no trench depth variation is included in the evaluated devices the influence of the rounding cannot be isolated from the trench sidewall because the area of the rounding is correlated to the trench sidewall area. It should also be mentioned that the behavior of a curved MOSCap is not equivalent to a planar structure and additional considerations to deal with the electrostatics (e.g. field crowding) of such a component must be considered when adding this to the model [9]. In addition to this, the real devices also include a fourth capacitance component which is caused by the field oxide depicted in Fig. 1 (b). Because of the low contribution to the overall capacitance (< 4 %) and insufficient variation of this parameter from design to design, this component is neglected in the investigation. Table 1 lists the different designs that are evaluated. Three different types of designs are used. Planar designs where no trench is etched, recess designs where one large continuous trench is etched, and trench designs were several trench stripes

with the same trench width and spacing (mesa width) are etched. The analytical calculation of the corresponding areas for the designs is described in literature [4,7]. For this calculation, the device areas are taken from the mask layout as drawn, the trench width is confirmed by focused-ion-beam (FIB) cross-section SEM measurements (Fig. 1 (c)), and wafer-level trench depth is measured by structured illumination microscopy (Fig. 1 (d)) which is verified by focused-ion-beam cross-section SEM measurements (Fig. 1 (c)). The area calculation is corrected by the top and bottom corner rounding measured by FIB-SEM. As described earlier, there is some measurement error for the wafer level measurements. For the following investigations, the trench depth measured by FIB-SEM on a device in the wafer center is used and it is assumed that the trench depth does not change from device to device as they are close together on the wafer. For future wafer level measurements, the accuracy of the optical trench depth measurement must be improved and a method to accurately determine the trench depth of each device such as optical critical dimension scatterometry should be considered to increase the accuracy of the method.

Table 1. Sizing of fabricated devices.

Design	Type	Area [mm^2]	Trench width [µm]	Mesa width [µm]	Effective area [10^3 μm^2]		
					Sidewall	Mesa	Bottom
1	Planar	1	0	1000	0	100	0
2	Recess	1	996	2	0.36	0.72	99.12
3	Trench	1	1	1	133.83	20.71	19.81
4	Trench	1	1	2	79.24	49.39	15.39
5	Planar	0.5	0	707	0	50	0
6	Recess	0.5	703	2	0.25	0.51	49.38
7	Trench	0.5	1	1	66.47	10.62	9.84
8	Trench	0.5	1	2	39.34	24.88	7.64
9	Planar	0.316	0	562	0	31.6	0
10	Recess	0.316	558	2	0.20	0.40	31.11
11	Trench	0.316	1	1	42.04	6.72	6.20
12	Trench	0.316	1	2	24.91	15.72	4.81

With the effective areas shown in Table 1 and equation 1 an overdetermined system of linear equations is formed which is then solved pointwise for every applied voltage. At least three different trench MOSCap designs with different area ratios are needed to solve the system of linear equations. Because of process variation, it is beneficial to increase the accuracy of the estimation by forming an overdetermined system of equations which is then solved by fitting a least-squares solution to the linear matrix equation. This yields an effective per-area capacitance for the trench mesa, trench sidewall, and trench, as bottom depicted in Fig. 4 for both, sample 1 and sample 2.

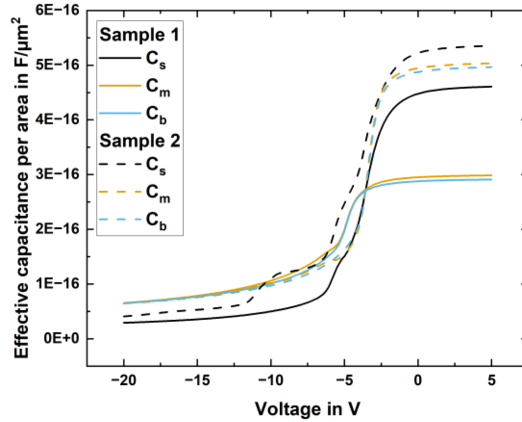

Fig. 4. Capacitance per area over voltage for trench mesa, bottom and sidewall calculated by linear component separation for the two different gate oxides.

For sample 1, the area-related oxide capacitance of the trench sidewall is larger than both the mesa and bottom capacitances. This suggests that the oxide thickness of the trench sidewall is lower than the oxide thickness of both the mesa and the bottom. As can be seen in Fig. 1 (e) this clearly is not the case. Sample 2 shows a similar effect even though here the oxide thickness of the sidewall is significantly larger than at the mesa and bottom. Some of this behavior can likely be attributed to the combination of trench sidewall and corner rounding to one capacitance. Previously, we suggested that the different slopes in the C-V curves are caused by the different oxide thicknesses. In the simple component separation, however, all curves show these different slopes. The curve for the mesa should not show this effect as no thickness variation caused by the trench geometries occurs. This leads to the conclusion that the three different components are not sufficiently separated. To verify the accuracy of the method the theoretical C-V curves for different designs are calculated using Eq. 1 (Fig. 5 (a) dashed lines) by multiplying the corresponding areas for sidewall, mesa and bottom listed in Table 1 with the calculated effective per area capacitance depicted in Fig. 4. When comparing them to the actual measurements (Fig. 5 (a) solid lines), good alignment can only be seen for the fully trench recessed devices (designs 2, 6 and 10). Fig. 5 (b) shows the relative error between the measurements and modelled capacitance of all 12 designs. It can be observed that the different design types (planar, recess, 1 µm trench/1 µm mesa and 1 µm trench/2 µm mesa) show characteristic error curves.

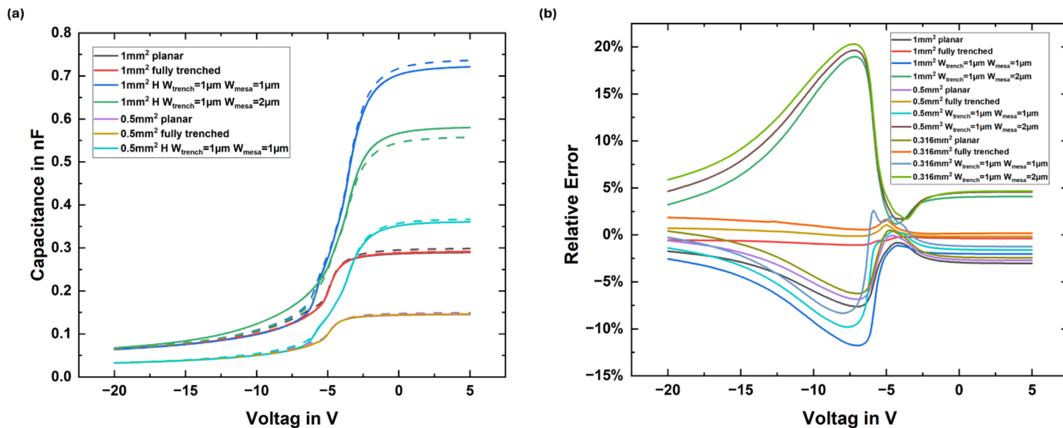

Fig. 5. a) Measured capacitance–voltage characteristics at 100 kHz (solid lines) for all 12 designs on one stepper field in the center of sample 1 (LPCVD TEOS oxide), compared with the corresponding curves reconstructed from the linearly separated mesa, sidewall, and bottom capacitances (dashed lines, using Eq. (1) and the areas in Table 1). b) Relative error between reconstructed and measured capacitances as a function of gate voltage for all designs, illustrating the systematic, design-dependent deviation of the simple parallel-capacitor model.

The largest error is observed for the devices with 1 µm trench and 2 µm mesa widths at -7.2 V where the curve calculated via linear component separation underestimates the actual capacitance of the devices by up to 20 %. Close to the voltage the error curves of the designs with 1 µm trench width and 1 µm mesa width show a minimum. This leads to the conclusion that there is another effect which the linear component separation assigns to the trench sidewall but is caused by the difference in mesa width. This effect is the previously described extension of the space charge region into the trench sidewalls. Because this effect does not only depend on the area of the different capacitance components but on the spacing of the trenches the simple linear combination of parallel capacitors cannot model this behavior and therefore ascribes the corresponding capacitance to the trench sidewall. A more refined compact model could represent the lateral extension of the depletion region between neighboring trenches by an additional series capacitance that depends on trench pitch and doping, while keeping the oxide-related contributions as parallel capacitors. Corner and field-oxide effects could likewise be represented by separate capacitance elements. However, introducing these additional components would substantially increase the number of unknown parameters. A calibrated TCAD simulations model might allow for a robust extraction of the depletion capacitance. In addition to this the influence of the corner rounding could also be more accurately be described through TCAD simulations.

Density of interface states.

For the evaluation of the density of interface states manual high and low frequency measurements (quasistatic and 1 MHz) and manual measurements at 100 kHz for the Terman D_{it} determination method equivalent to the full wafer C-V measurements on four devices per wafer were done. Fig. 6 (a) shows the density of interface states for design 1 (planar) and design 3 (1 µm trench/1 µm mesa) on sample 1. The measured values are in good agreement with previously reported results for planar MOSCaps using LPCVD TEOS oxides annealed in NO [3]. The differences between the high-low method and the Terman method are well reported [9]. However, because of measurement time and setup requirements of the low frequency measurement for the high-low method, it is not suitable for wafer level measurements. When applying the high low-method to the trench devices and assuming a constant surface potential and no variation of the oxide thickness the difference between the planar structures and the trench devices is not too large [10]. The Terman method shows an increased deviation between the trench and planar designs.

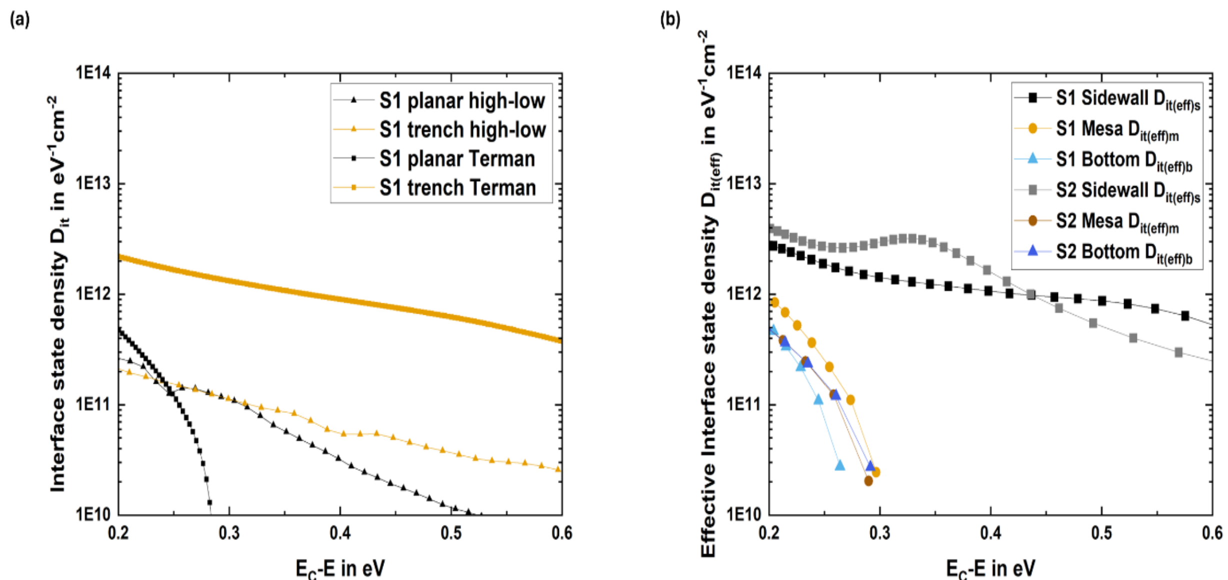

Fig. 6. a) Average interface state density determined by the high-low and Terman methods for four devices per design for planar and trench MOSCaps on sample 1. b) Calculated effective D_{it} for the trench sidewall, mesa and bottom with the Terman method.

An effective D_{it} for the three calculated capacitance components for design 3 is evaluated for sample 1 and sample 2. Overall, these values are not quantitatively accurate as many influences that were previously described are not included in this model. The extracted quantities should therefore be regarded as effective D_{it} values, which also contain these parasitic effects. The behavior of the mesa top and trench bottom follows the Terman evaluation for the planar devices, while the trench sidewall follows the trenched devices. Sample 1 shows a lower effective D_{it} for the trench sidewall leading to the conclusion that between the two compared oxide processes the LPCVD TEOS oxide is better suited for fabricating UMOSFETs. However, because of the different SiO_2 thickness distributions and the model errors of up to 20 %, this apparent difference cannot be interpreted as a rigorous quantitative statement about the physical D_{it} at the trench sidewall.

Summary and Outlook

In this work, we demonstrate a linear component separation approach to extract effective sidewall capacitances from 4H-SiC UMOSCaps fabricated with LPCVD TEOS and polysilicon oxidation. While planar MOSCaps exhibit good breakdown performance trench devices show reduced breakdown strength attributed to non-uniform oxide thickness and corner field crowding.

It was possible to separate the capacitance-voltage measurement with the proposed linear component separation. However, significant systematic deviations between measured and reconstructed capacitances indicate that the simple parallel capacitor model inadequately captures the complex electrostatic behavior of trench structures. The observed errors correlate with design geometry, suggesting that mesa spacing-dependent depletion, field oxide contributions, and trench corner effects cannot be neglected. Future improvements should incorporate physics-based models for lateral depletion behavior and an expansion from point wise solving the linear matrix equation to form a linear system of functions and solving for these functions. Integration with TCAD simulations could provide deeper insights into the underlying physics and enable development of more accurate analytical models.

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