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Characterization of Al-Gate MOS Capacitor on Thermally Oxidized 3C/4H Hybrid Polytype-Heterostructure Si-Face SiC(0001) Wafer Fabricated by Simultaneous Lateral Epitaxy (SLE) Method

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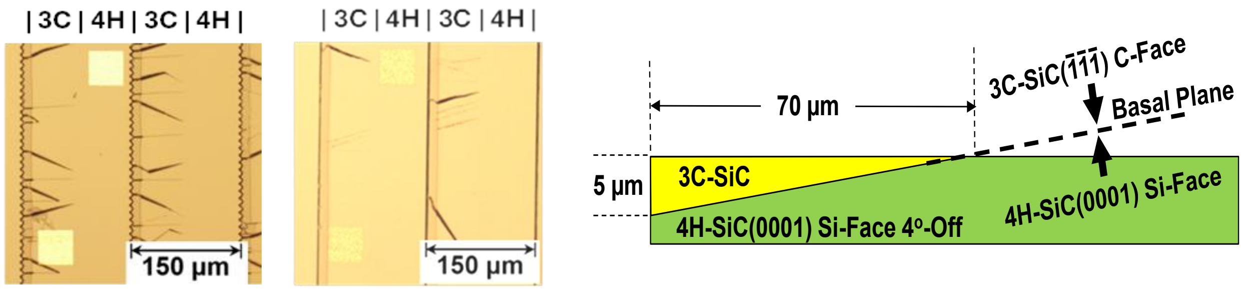
Abstract. 3C-SiC with a moderate band gap and a large electron affinity is expected to have superior long-term stability against performance degradation. We have fabricated Al-gate MOS diodes in 3C-on-4H-SiC and 4H-SiC regions on a simultaneous lateral epitaxy (SLE) wafer. Here, evaluation results of their high-frequency differential capacitance-voltage (C-V) characteristics are reported and, from suggested band diagrams, carrier transport involved in the phenomena are considered. In the case of n^--type 3C-on-4H-SiC MOS diode, increase in capacitance due to fast modulation in the inversion layer charge (hole) concentration can be confirmed in the negative bias below −5 V. 2-dimensional hole gas (2DHG) is considered at the Si-face 3C/4H heterointerface negatively charged by spontaneous polarization and is expected to be an effective supply source of holes. Especially in the case of *p*-type 3C-on-4H-SiC MOS diode, it is considered that injection of holes from neutral *p*-type region into the heterointerface induces compensation of the fixed charges and lowering of the electron barrier at conduction band, and then, electron injection through the barrier causes the fast response of inversion-layer modulation. Appearance of the larger frequency dependence can be understood by inclusion of the larger-activation-energy phenomena, such as “a deep acceptor level” and “2DHG confined by fixed charges”. These findings are believed to contribute to building new production platforms of high-performance power semiconductor devices utilizing the polytype heterostructure of SiC.

Introduction

Metal-oxide-semiconductor (MOS) transistors using 3C-SiC, which have moderate band gap (2.4 eV) and large electron affinity compared to that of 4H-SiC, are expected to have superior long-term stability against performance degradation due to leakage current in the gate insulator in addition to high blocking voltage, low interface trap density and higher *n*-channel mobility than 300 $cm^2/(V\text{-}s)$



(a) (b) (c)

Fig. 1. Optical micrographs of (a) n^--type and (b) p-type Al-gate MOS diodes using the SLE wafer, (c) schematic cross-sections for a stripe between periodically arranged trenches. SLE trench interval, widths for 3C-SiC stripe, 4H-SiC stripe and length of Al gate square are 150 µm, 70 µm, 80 µm and 50 µm, respectively.

at 25 °C [1-3]. Recently, a simultaneous lateral epitaxy (SLE) method has been developed in which 3C-SiC and 4H-SiC are simultaneously epitaxially grown along the basal plane and produced 3C-on-4H polytype heterostructure SiC wafers (SLE wafers) [4-6]. In this presentation, we will report on the fabrication of Al-gate MOS diodes in 3C-on-4H-SiC and 4H-SiC regions on a single SLE wafer (**Fig. 1**) and the evaluation results of their high-frequency differential capacitance-voltage (C-V) characteristics.

Experimental

One piece cut out from a SLE wafer produced from Si-face 4H-SiC(0001) wafer with off angle of 4° along [11$\bar{2}$0] (Fig. 1) was used as an n^--type SLE wafer (carrier concentration of about 10^{16} cm^{-3}), and the other was used as an SLE wafer with a *pn* junction after high-temperature ion implantation (500 °C, Al ions) and heat treatment (1700 °C, 5 min, Ar atmosphere) to make a 500 nm-thick surface p-type layer (carrier concentration of about 2×10^{17} cm^{-3}). Here, a 24-30 nm-thick thermal oxide (SiO_2) film was formed by H_2-O_2 pyrogenic wet oxidation (1050 °C, 4 h). Subsequently, about 100 nm-thick Al film was deposited on the surface, and resist patterns were formed on each area of 3C-SiC and 4H-SiC by photolithography using direct laser drawing exposure method, and Al gate electrodes were formed by wet etching. Finally, about 100 nm-thick Al film was deposited on the back surface and H_2 sintering was performed at 400 °C (95% N_2 + 5% H_2, atmospheric pressure). C-V characteristics of the MOS diodes were measured at room temperature and 50-400 kHz for the small amplitude signal superimposed on the gate voltage sweep.

Results and Discussion

The evaluation results of their C-V characteristics are shown in **Fig. 2** and, from suggested band diagrams shown in **Figs. 3-6**, carrier transport involved in the phenomena are considered. Here, following the advanced research on 3C/4H-SiC polytype heterostructure with spontaneous polarization [7-11], discontinuity at conduction band and negative fixed charges at the 3C/4H heterointerface have been included in the band diagrams. In Figs. 4-6, we are assuming situations in which a depletion layer exists inside far away from the MOS interface in relation to heterointerface and/or the *pn* junction, and stretching/shrinking of the width of the depletion layer are causing charging/discharging of the depletion layer capacitance (C_D). Therefore, we added C_D in the inset pictures of equivalent circuit.

n^--type 4H-SiC Region.

In the case of n^--type 4H-SiC MOS diode (Fig. 2 (a)), the C-V curve indicates that free electrons accumulate at the SiO_2/4H-SiC interface in the positive bias (Fig. 3 (b)), while the capacitance decreases monotonically in the negative bias, suggesting the expansion of the depletion layer (Fig. 3 (a)). Here, the depletion is observed near 0 volts, and the flat band voltage is estimated to be about +3V.

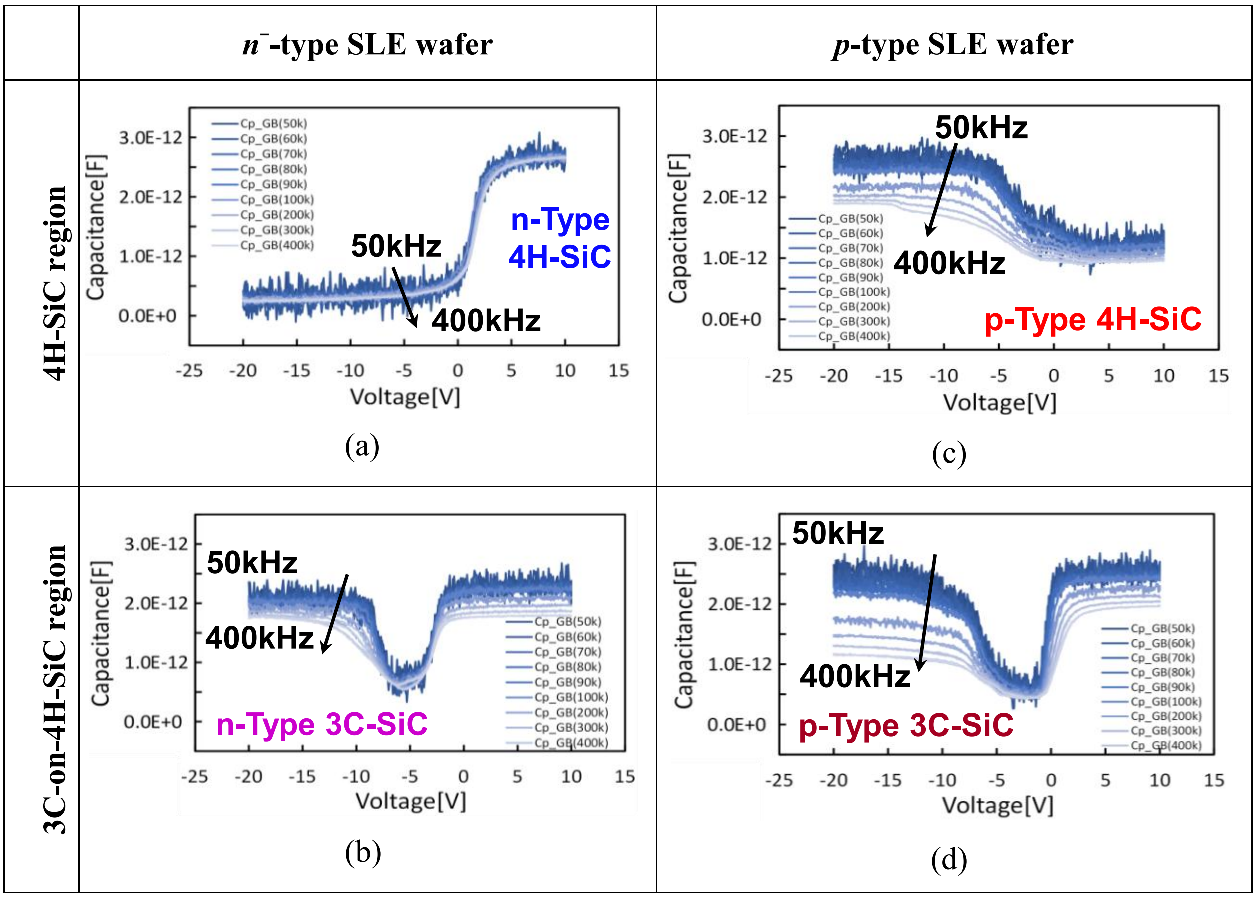


Fig. 2. C-V characteristics of the MOS diodes at room temperature and 50-400 kHz for the small amplitude signal superimposed on the gate voltage.

n^--type 3C-on-4H-SiC Region.

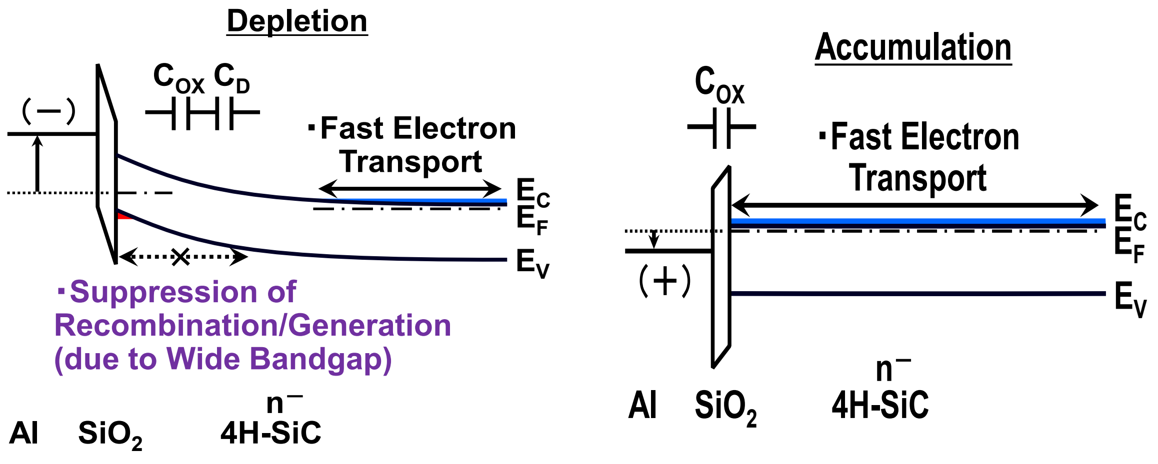
In the case of n^--type 3C-on-4H-SiC MOS diode (Fig. 2 (b)), free electrons accumulate at the SiO_2/3C-SiC interface at around 0 V and in the positive bias, while increase in the capacitance due to fast change in the inversion layer charge (hole) concentration can be confirmed in the negative bias below -5 V. The latter indicates a fast response of minority carrier (hole) concentration at the SiO_2/3C-SiC interface, although 3C-SiC has a sufficiently wide band gap to suppress carrier generation at room temperature. It has been reported that 2-dimensional hole gas (2DHG) is formed at the Si-face 3C/4H heterointerface negatively charged by a spontaneous polarization [7-8] (Fig. 4). Therefore, it is considered that 2DHG can act as an effective supply source of holes. In contrast, on the C-face 3C/4H-SiC heterointerface, formation of a 2-dimensional electron gas (2DEG) with channel mobility as high as 780 $cm^2/(V\text{-}s)$ has been observed [9-11].

p-type 4H-SiC Region.

In the case of p-type 4H-SiC MOS diode (Fig. 2 (c)), holes are considered to accumulate at the SiO_2/4H-SiC interface in the negative bias (Fig. 5 (a)), while a monotonic decrease in the capacitance can be confirmed in the positive bias, suggesting the expansion of the depletion layer (Fig. 5 (b)). In addition, since no increase in capacitance is observed in the positive bias, it is believed that conversion from n^--type to *p*-type by Al ion implantation is successful, and a high-quality *pn* junction (*pn* isolation structure) is formed.

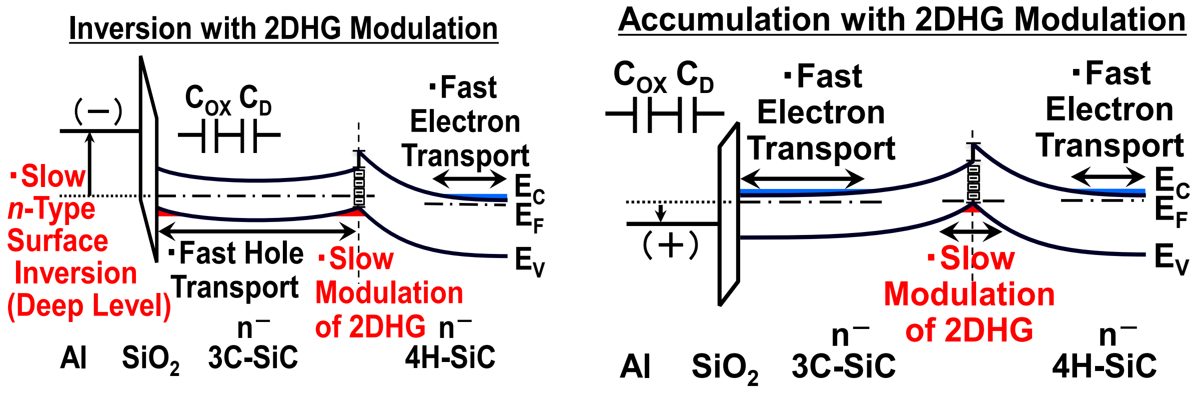
***p*-type 3C-SiC Region.**

In the case of *p*-type 3C-SiC MOS diode (Fig. 2 (d)), a drastic increase in the capacitance in the positive bias is clearly observed, indicating not only fast response of the minority carrier (free electron) concentration at the SiO_2/3C-SiC interface but also the drastic change of band alignment. From the suggested band diagram shown in Fig. 6 (b), it is considered that (1) holes are injected from the *p*-type 3C-SiC, (2) the injected holes neutralize the fixed negative charges at the Si-face 3C/4H heterointerface [7- 8] and causes (3) barrier lowering to enhance free electron transport from the n^--type 4H-SiC (similarly to "parasitic bipolar effect"). When we assume that most of holes in the p-type 3C-SiC layer are injected into the 2DHG, the sheet density is estimated as high as about 1×10^{13} cm^{-2} from the implanted *p*-type dopant dose. Additionally, reported sheet hole density of 2DHG induced by spontaneous polarization (9.7×10^{12} cm^{-2} [7]) is almost the same order. Therefore, neutralization by compensation can be considered to occur effectively at the heterointerface. Here, it can be suggested that a structure of n^--type 4H-SiC/2DHG/n^--type 3C-SiC acts as an *npn* heterojunction bipolar transistor with high current gain due to a wider-gap emitter and a narrower-



(a) (b)

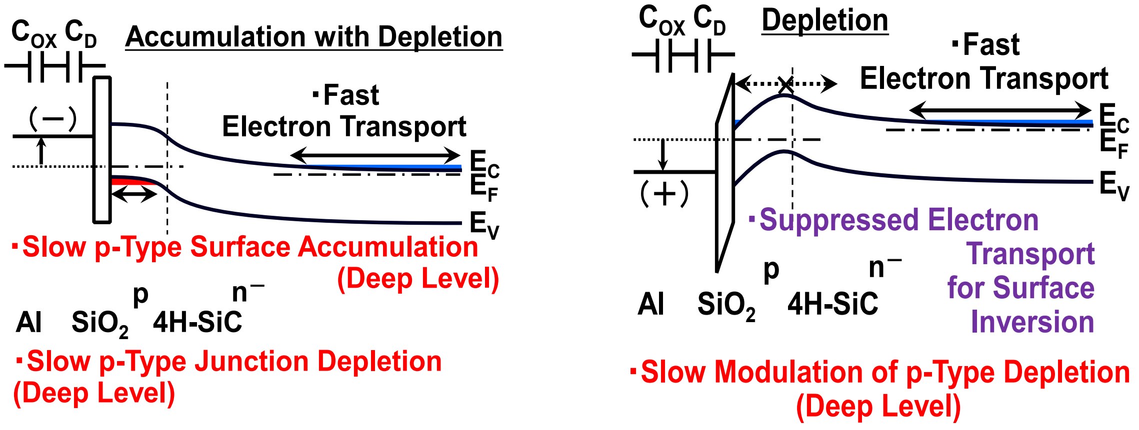
Fig. 3. Suggested band diagram of the MOS diode on n^--type 4H-SiC region of SLE wafer under (a) negative and (b) positive bias.



(a) (b)

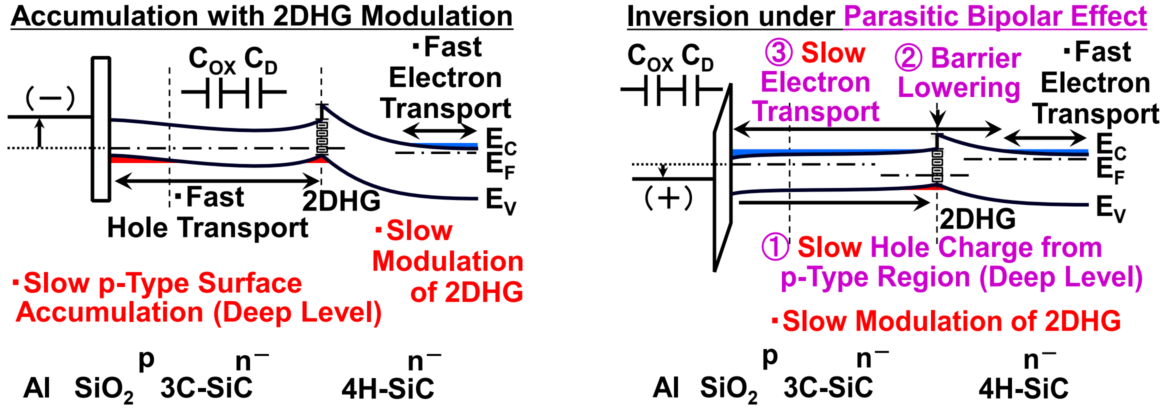
Fig. 4. Suggested band diagram of the MOS diode on n^--type 3C-SiC region of SLE wafer under (a) negative and (b) positive bias.

gap base, in which holes are supplied from *p*-type 3C-SiC through the depleted *n*⁻-type 3C-SiC to 2DHG. On the other hand, in a negative bias of −5 V or less, holes accumulate at the SiO_2/3C-SiC interface as shown in Fig. 6 (a), and the flat band voltage is estimated to be about −7 V. It is considered that the conversion from *n*⁻-type to *p*-type by ion implantation is successful in 3C-SiC as well as 4H-SiC. For example, the holes in 2DHG below the gate electrode are considered to move away out of the electrode area (50 μm^2) due to horizontal electric field caused by applying positive gate voltage. Based on such phenomenology, the holes in 2DHG should move because the band bending changes. Here, we assume that "slow modulation of 2DHG" (shown in Figs. 4 and 6) includes two phenomena such as "wide-range horizontal movement of holes during entering/exiting the electrode area along the 2DHG" and "capture/release in the deeply-confined state at the 2DHG". Because the phenomena seemed to be not so quick due to wide range and deepness, it is considered that the modulation might be slow and induce the frequency dependence.



(a) (b)

Fig. 5. Suggested band diagram of the MOS diode on *p*-type 4H-SiC region of SLE wafer under (a) negative and (b) positive bias.



(a) (b)

Fig. 6. Suggested band diagram of the MOS diode on *p*-type 3C-SiC region of SLE wafer

Frequency Dependence of Capacitance

From overview of all the C-V curves, frequency dependence of capacitance is found especially in Fig. 2 (b-d). As such frequence dependence can be seen generally in trap and release process of carrier at specific state, it can be imagined that the larger activation energy results in the slower response. In our case, acceptor level of Al atom doped in 4H-SiC and 3C-SiC is reported to have relatively large activation energy such as 0.25-0.26 eV [12-13], while donor level of N atom doped in 4H-SiC and 3C-SiC has as low activation energy as 0.0653 eV and 0.124 eV in 4H-SiC and 0.018-0.047 eV in 3C-SiC [14-15]. Therefore, appearance of the larger frequency dependence can be understood by inclusion of the larger-activation-energy phenomena, such as "a deep acceptor level" and "2DHG confined by fixed charges". Here, during modulation of depletion layer thickness by small-amplitude signal at high frequency for capacitance measurement, holes in the trap and release process at deep acceptor level especially at edge of the depletion layer will contribute to frequency dependence. Additionally, because similar relation can be also imagined between holes and the negative fixed charges at Si-face 3C/4H heterointerface, "2DHG confined by fixed charges" will also contribute to frequency dependence in supplying/receiving holes (Figs. 4 and 6). In another typical case of n^--type 4H-SiC region (Fig. 2. (a)), due to shallow donor level without heterointerface, frequency dependence is considered to become small. Thus, it is suggested that frequency dispersion of capacitance is large in Fig. 2 (b-d) and significant especially at negative bias in Fig. 2 (d) with coexisting effect of the Al doped region and 3C/4H heterointerface. For the detailed contribution of each process, further research is needed. "Additionally, it should also be noted that frequency dependence in both the accumulation and inversion capacitance of C-V characteristics can be observed if the series resistance is high [16]. Therefore, concerning the actual effect of series resistance as well as contribution of interface traps at the SiO_2/SiC, further investigations are necessary."

Summary

By fabrication of Al-gate MOS diodes in 3C-on-4H-SiC and 4H-SiC regions on an SLE wafer, evaluation results of their high-frequency C-V characteristics are reported and, from suggested band diagrams, carrier transport involved in the phenomena are considered. In the case of n^--type 3C-on-4H-SiC MOS diode, increase in capacitance due to fast modulation in the inversion layer charge (hole) concentration can be confirmed in the negative bias below −5 V. 2-dimensional hole gas (2DHG) is considered at the Si-face 3C/4H heterointerface negatively charged by spontaneous polarization and is expected to be an effective supply source of holes. Especially in the case of *p*-type 3C-on-4H-SiC MOS diode, it is considered that injection of holes from neutral p-type region into the heterointerface induces compensation of the fixed charges and lowering of the electron barrier at conduction band, and then, electron injection through the barrier causes the fast response of inversion-layer modulation. Appearance of the larger frequency dependence can be understood by inclusion of the larger-activation-energy phenomena, such as "a deep acceptor level" and "2DHG confined by fixed charges". These phenomena can be useful sometimes, but they can also be a hindrance if they are used improperly. Strategy of elimination or utilization for such phenomena will be important for breakthroughs in the novel semiconductor device development. These findings are believed to contribute to building new production platforms of high-performance power semiconductor devices utilizing the polytype heterostructure of SiC.

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