Materials Science Forum
ISSN: 1662-9752, Vol. 1192, pp 47-52
doi:10.4028/p-8XxBpT
© 2026 The Author(s). Published by Trans Tech Publications Ltd, Switzerland.
Submitted: 2025-09-16
Revised: 2025-12-16
Accepted: 2026-02-26
Online: 2026-05-20

Enhanced Mobility in SiC (0001) MOSFETs Using a Decoupled Plasma Nitridation (DPN) Process and Oxide Deposition

Koushik Ramadoss[1,a*], Joshua Holt[2,b], Lucien Date[3,c], Safdar Muhammad[4,d], Jesse Kalliomaki[4,e], Fernanda Albrechtvechietti[4,f], William Charles[5,g], Athena Pang[2,h], Shubhendra Jain[5,i], Benjamin Briggs[5,j], Ludovico Megalini[2,k], Michael Chudzik[2,l], Dallas Morisette[1,m] and James Cooper[1,n]

[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA

[2]Applied Materials, 3325 Scott Bldv., Santa Clara, CA 95054, USA

[3]Applied Materials, Kapeldreef 75, Leuven, BEL 3001, Belgium

[4]Applied Materials, Masalantie 365, 02430, Masala, Finland

[5]Applied Materials, 1 Broadway, Cambridge, MA 02142, USA

[a*]kramado@purdue.edu, [b]Joshua_Holt@amat.com, [c]lucien_date@amat.com, [d]safdar_muhammad@amat.com, [e]jesse_kalliomaki@amat.com, [f]fernanda_albrechtvechietti@amat.com, [g]william_charles@amat.com, [h]Athena_Pang@amat.com, [i]Shubhendra_Jain@amat.com, [j]benjamin_briggs@amat.com, [k]ludovico_megalini@amat.com, [l]michael_chudzik@amat.com, [m]morisett@purdue.edu, [n]cooperj@purdue.edu

Keywords: atomic layer deposition, decoupled plasma nitridation, MOSFET, H_2 etching.

Abstract. In this work, we demonstrate a novel oxidation-free gate oxide process consisting of a two-step surface preparation treatment, followed by atomic layer deposition of SiO_2 and a post-deposition anneal in nitrogen. The surface treatment includes a 1300°C anneal in hydrogen and dilute silane, followed by decoupled plasma nitridation (DPN). Long channel MOSFETs fabricated with this process show a 1.5X improvement in peak field effect mobility compared with devices utilizing a standard thermal oxide and NO anneal. The MOSFETs had a positive threshold voltage, low gate leakage, and a breakdown field above 8 MV/cm.

Introduction

Silicon carbide (SiC) is a wide gap semiconductor that is being rapidly adopted in power electronic applications due to its high critical electric field, high thermal conductivity, the availability of high-quality large area substrates, and maturing fabrication technology. However, SiC MOSFETs exhibit poor performance due to a high density of interface states, leading to low channel mobility (<5% of bulk mobility). To mitigate this, various studies have been conducted using deposited gate oxide processes to avoid thermal decomposition of the substrate. These processes include atomic layer deposition (ALD) [1], plasma enhanced CVD [2] [3], and a process we call “poly-ox”, wherein a thin film of Si is deposited by chemical vapor deposition (CVD), followed by oxidation of the Si film at a sufficiently low temperature to avoid oxidation of the underlying SiC [4] [5]. Alternatively, other nitridation techniques including nitrogen plasma [6] [7] [8], N_2O [9] and high temperature nitrogen anneals [4] have been explored as an alternative to the NO anneal to maximize the nitrogen coverage and improve interface properties. But these methods have negative side-effects such as the incorporation of nitrogen throughout the bulk of the oxide [4], or lead to only marginal improvements in interface properties. In this study, we use an Applied Materials™ Centura™ DPN (decoupled plasma nitridation) process in conjunction with an Applied Materials™ Picosun™ P300B ALD tool to form an oxidation-free SiO_2 gate oxide. Decoupled plasma nitridation is a remote plasma process, capable of directly nitriding the SiC surface within a few tens of seconds, and is therefore particularly suitable for high-volume manufacturing [10] [11] [12] [13] [14]. Optimization of the DPN parameters allows the introduction of a tunable concentration of nitrogen as high as ~$1.5x10^{21}/cm^3$ in a sharply

This article is an open access article under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0)

defined peak at the SiC/SiO_2 interface, making the traditionally hours-long and expensive NO or N_2O post-deposition nitridation process unnecessary. When combined with a hydrogen + dilute silane surface pretreatment process as described previously [5] [2] [15] , MOSFETs formed by this process show a 1.5X enhancement in peak channel mobility compared to standard MOSFETs prepared by thermal oxidation and NO annealing, as well as a positive threshold voltage, low gate leakage, and a breakdown field greater than 8 MV/cm.

Device Fabrication

Our oxidation-free gate dielectric process was demonstrated using long-channel MOSFET templates consisting of an n-type 4H-SiC substrate with a 9.0×10^{15} cm^{-3} n-type epilayer and ion implanted p-body regions having a surface aluminum concentration of 1.6×10^{16} cm^{-3}, confirmed by SIMS analysis. The source and drain regions consist of highly doped n^+ regions implanted with nitrogen. The DPN-based process flow used to form the gate oxide is shown in Fig. 1. Before forming the gate oxide, the substrates were first RCA cleaned and subjected to H_2 etching in a hot walled CVD furnace (1300°C, 900 mbar, 10 slm H_2) for 6 min. During the final 3 minutes of this anneal, a 5% SiH_4/H_2 mixture was added at a flow rate of 100 sccm, for a silane concentration of 0.05%. This last silane step is critical to minimize and passivate interface defects [5] [2] [15]. Subsequently the samples were subjected to the DPN process with a remote plasma to incorporate nitrogen into the SiC surface, similar to that formed by a post-deposition anneal in NO. A 48 nm thin film of silicon dioxide was then deposited using an Applied Materials Picosun P300B ALD system, and densified by annealing in a N_2 ambient at 1200°C for 30 min. The final MOSFETs were formed with n-type polysilicon gates doped by 800°C, 60 s diffusion from a Filmtronics P509 spin-on phosphorus source, Ni source and drain ohmic contacts formed by rapid thermal annealing at 800°C for 120 s, and Al top metal pads were deposited and patterned for electrical contacts. The gate poly was also encapsulated by a 300 nm thick PECVD SiO_2 prior to the formation of ohmic contacts. The channel length and width are 140 μm and 110 μm respectively. In our experiments, a control sample was prepared by thermal oxidation of SiC in dry O_2 followed by NO annealing at 1175°C for 2 hrs. to give about 50 nm of SiO_2 for comparison.

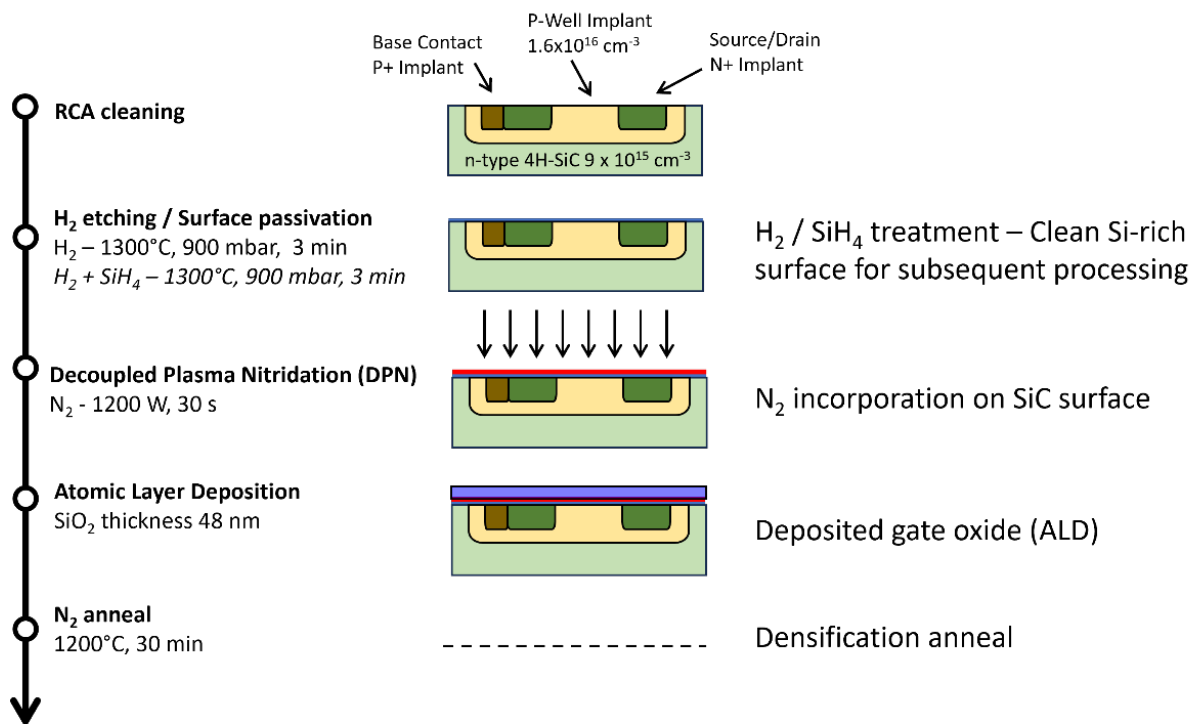

Fig. 1. Process flow diagram for DPN based gate oxide process.

Results and Discussion

The transfer characteristics of a typical MOSFET fabricated in this manner are shown in Fig 2a.

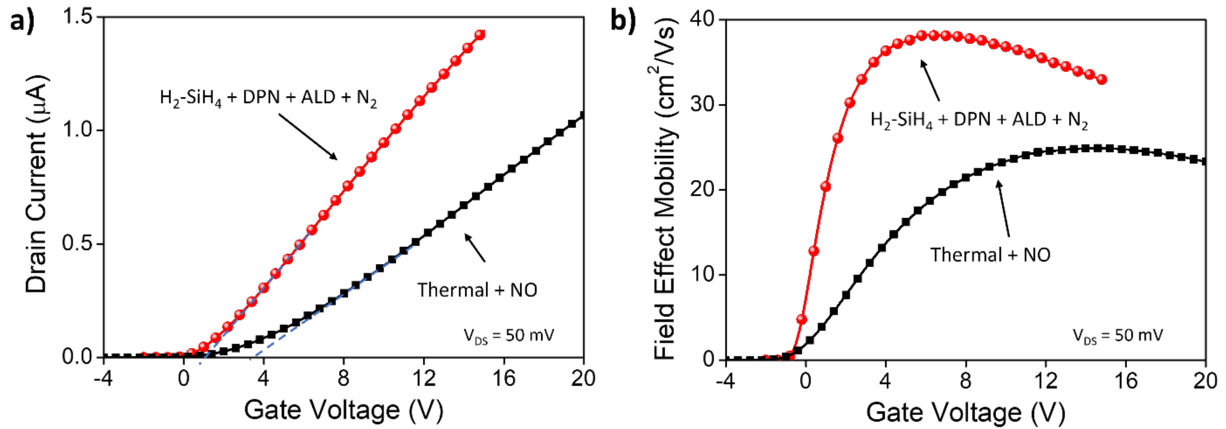

Fig. 2. Transfer characteristics (a) and field-effect mobility (b) as a function of gate voltage for MOSFETs formed by the DPN process in comparison with a standard thermal + NO process.

The device shows a sharper increase in drain current with a positive but somewhat reduced threshold voltage (V_{th} ~ 1 V) in comparison to the control sample with a 50 nm thick thermally grown gate oxide and NO anneal. The field effect mobility (Fig. 2b) of a DPN treated device shows a significant 1.5X improvement (~38 cm^2/Vs) as compared to the control sample (~25 cm^2/Vs). This increased mobility, reduced threshold voltage, and a sharper turn-on characteristic are all consistent with a significant reduction in the interface state density. It is important to note that these measurements were done on an ion implanted channel with $N_A = 1.6 \times 10^{16}$ cm^{-3}. While this p-type doping concentration may be insufficient for practical power devices, it still allows a direct comparison of parameters for the MOSFETs fabricated with the two different gate oxide methods.

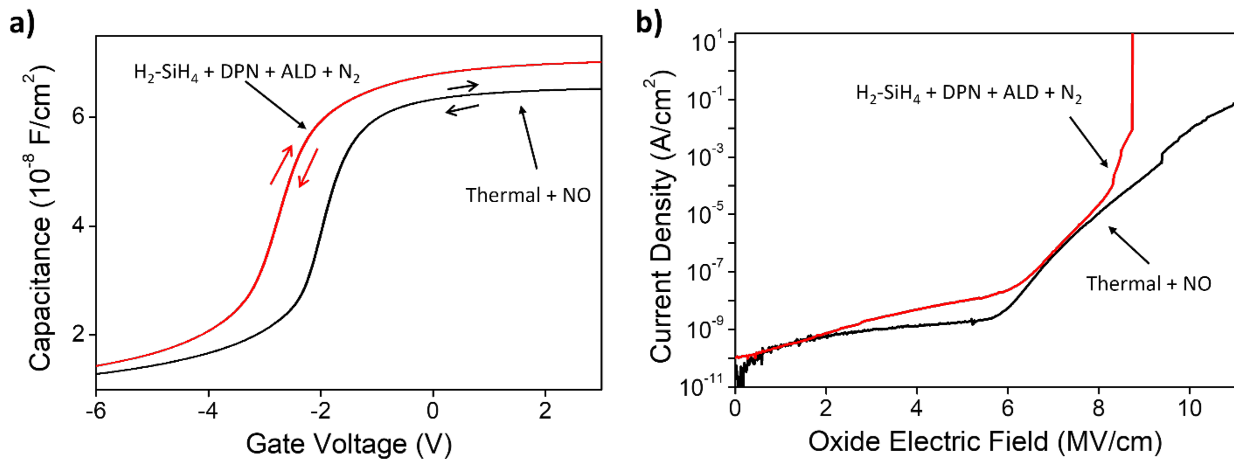

Fig. 3. a) Normalized CV characteristics of DPN treated circular MOSCAP device (diameter = 225 µm) compared with Thermal + NO control. b) Comparison of leakage current and oxide breakdown fields for DPN treated device and Thermal + NO control.

The high frequency CV characteristics (at 100 kHz in dark conditions) are shown for the DPN treated MOSCAPs (Fig 3a). The normalized CV data shows minimal hysteresis, and a -0.8 V shift in the CV curve compared to the control sample. This shift is consistent with that of a reduction in negative interface charges (interface + fixed charge) of $q*3.45 \times 10^{11}$ C/cm^2 and is also consistent with the higher mobility shown in Fig 2b. The DPN treated MOSCAPs also exhibit low leakage current and a high breakdown field (> 8 MV/cm) (Fig. 3b), although somewhat lower breakdown field than the thermal+NO control sample. While nearly ideal breakdown fields have been observed in ALD deposited SiO_2 films [16], it is not uncommon for such films to have somewhat lower

breakdown fields than thermal oxides. Further optimization of our process is required to achieve an oxide breakdown field comparable to traditional thermal+NO oxides. Fig. 4 shows a transmission electron microscopy (TEM) cross-section image and electron energy loss spectroscopy (EELS) map across the interface. The image indicates that the N_2 is preferentially incorporated at the interface during the DPN treatment with small distribution into the oxide bulk.

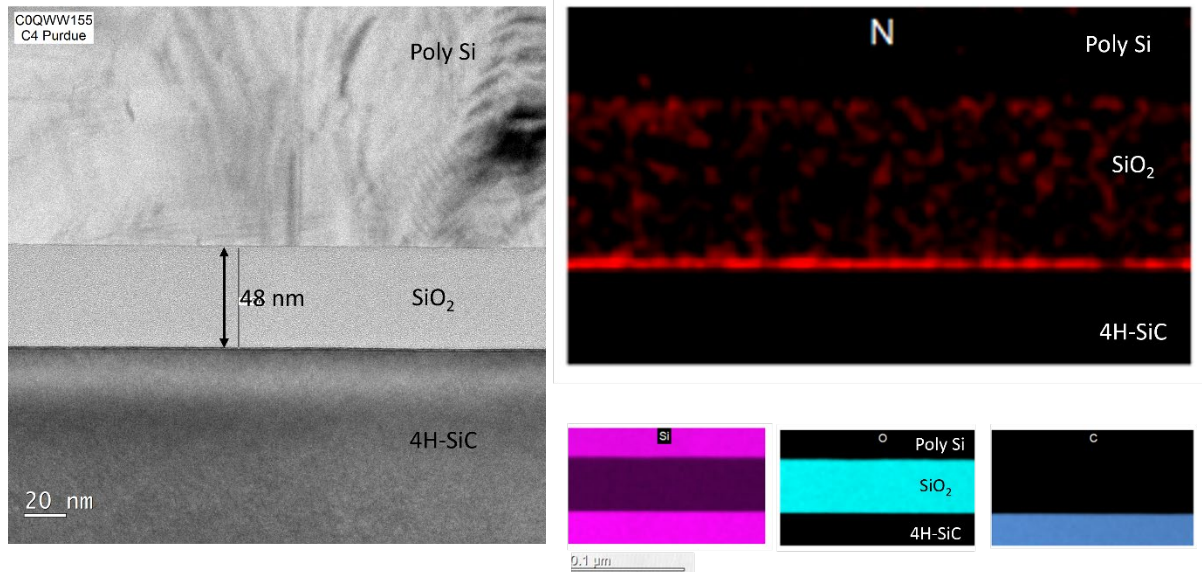

Fig. 4. TEM micrograph of DPN treated device showing SiO_2 thickness of 48 nm. The EELS map of various elements (Nitrogen, Silicon, Oxygen, Carbon) across the device cross section is also shown.

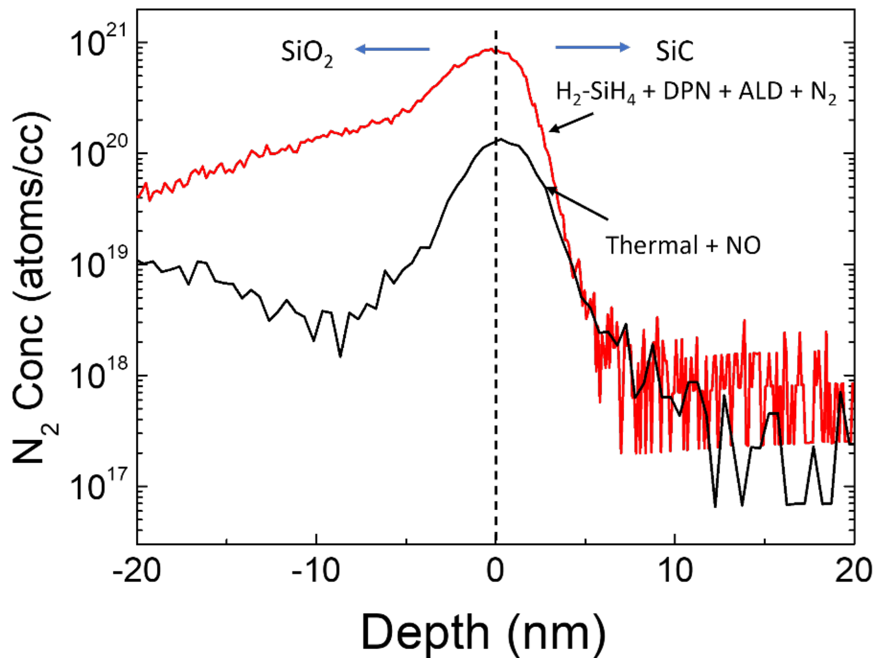

Fig. 5. Depth profiles of nitrogen atom concentration near SiC-SiO_2 interface and in the bulk SiO_2. The peak concentration at the interface is slightly higher than Thermal + NO control.

To quantify the concentration of N_2 near the interface and in the bulk oxide, depth profiling was performed using SIMS as shown in Fig. 5. The results indicate high concentration of N_2 near the interface for DPN treated samples with small amount of N_2 present in the bulk of the oxide as well. Further experiments are required to optimize the conditions of DPN treatment and post ALD deposition anneal to further improve the device performance.

Conclusion

In summary, we have demonstrated a gate oxide process that reduces the interface defect density to yield a 1.5X improvement in peak channel mobility while maintaining a small positive threshold voltage. The effectiveness of the DPN process in nitriding the SiC surface in a very short time enables a high-throughput fabrication process and is therefore particularly suitable for high-volume manufacturing of SiC devices.

Acknowledgement

The authors would like to thank the support from the Margot A. and Carl J. Johnson Foundation for financial support. This work was done in part at the Birck Nanotechnology Center, Purdue University. We also acknowledge the assistance from Clas-SiC Wafer Fab.

References

[1] R. P. Ramamurthy, D. T. Morisette, V. Amarasinghe and L. C. Feldman, "Thermal-oxidation-free dielectrics for SiC power devices," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017.

[2] K. Tachiki, M. Kaneko and a. T. Kimoto, "Mobility improvement of 4H-SiC (0001) MOSFETs by a three-step process of H2 etching, SiO2 deposition, and interface nitridation," *Applied Physics Express,* vol. 14, p. 031001, 2021.

[3] M. Yakut, A. Roy, F. Arith, A. Whitworth, A. Alexander, J. Gryglewicz, J. Sheriff, S. Olsen, K. Vasilevskiy and a. A. O'Neill, "Increasing Mobility in 4H-SiC MOSFETs with Deposited Oxide by In-Situ Nitridation of SiC Surface," *Solid State Phenomena,* vol. 359, pp. 157-162, 2024.

[4] T. Kobayashi, T. Okuda, K. Tachiki, K. Ito, Y.-i. Matsushita and a. T. Kimoto, "Design and formation of SiC (0001)/SiO2 interfaces via Si deposition followed by low-temperature oxidation and high-temperature nitridation," *Applied Physics Express,* vol. 13, p. 091003, 2020.

[5] K. Ramadoss, A. Samal, D. T. Morisette and a. J. A. Cooper, "High Mobility SiC MOSFETs Using an Oxidation-Minimizing Process," in *Poster presented at 21st International Conference on Silicon Carbide and Related Materials*, 2024.

[6] X. Zhu, A. C. Ahyi, M. Li, Z. Chen, J. Rozen, L. C. Feldman and a. J. R. Williams, "The effect of nitrogen plasma anneals on interface trap density and channel mobility for 4H–SiC MOS devices," *Solid-State Electronics,* vol. 57, no. 1, pp. 76-79, 2011.

[7] Modic, Y. Sharma, Y. Xu, G. Liu, A. Ahyi, J. Williams, L. Feldman and a. S. Dhar, "Nitrogen Plasma Processing of SiO2/4H-SiC Interfaces," *Journal of Electronic Materials,* vol. 43, p. 857–862, 2014.

[8] D.-K. Kim, Y.-S. Kang, K.-S. Jeong, H.-K. Kang, S. W. Cho, K.-B. Chung, H. Kim and a. M.-H. Cho, "Effects of spontaneous nitrogen incorporation by a 4H-SiC(0001) surface caused by plasma nitridation," *Journal of Materials Chemistry C,* vol. 3, pp. 5078-5088, 2015.

[9] T. Kimoto, H. Kawano, M. Noborio, J. Suda and a. H. Matsunami, "Improved Dielectric and Interface Properties of 4H-SiC MOS Structures Processed by Oxide Deposition and N2O Annealing," *Materials Science Forum ,* Vols. 527-529, pp. 987-990, 2006.

[10] H. N. Al-Shareef, A. Karamcheti, T. Y. Luo, G. Bersuker, G. A. Brown, R. W. Murto, M. D. Jackson, H. R. Huff, P. Kraus, D. Lopes, C. Olsen and G. Miner, "Device performance of in situ steam generated gate dielectric nitrided by remote plasma nitridation," *Applied Physics Letters,* vol. 78, pp. 3875-3877, 2001.

[11] Materials, "TSMC Qualifies Applied Materials' Gate Stack System for Its Leading-Edge 65nm Transistor Processes," Applied Materials, Inc, 5 May 2005. [Online]. Available: https://ir.appliedmaterials.com/news-releases/news-release-details/tsmc-qualifies-applied-materials-gate-stack-system-its-leading/.

[12] S. W. Lim, T.-Y. Luo and a. J. Jiang, "Mechanism of Silicon Dioxide Decoupled Plasma Nitridation," *Japanese Journal of Applied Physics,* vol. 45, p. L413, 2006.

[13] M. Tian, K. Chen, C. Wang, T. Guan, Q. Sun and a. D. W. Zhang, "Decoupled Plasma Nitridation (DPN) and Postnitridation Annealing (PNA) Treatment for Metal Boundary Effect Reduction," *IEEE Transactions on Electron Devices ,* vol. 71, no. 3, pp. 2233 - 2237, 2024.

[14] P. Fiorenza, G. Lorito, L. Vigo, L. Date, J. Holt, M. Vivona, G. Cautiero, A. Cockburn, L. Megalini, M. Chudzik and a. F. Roccaforte, "Decoupled Plasma Nitridation of SiC surface for Interface States Density reduction in 4H-SiC MOS Capacitors," in *Poster presented at 22nd International Conference on Silicon Carbide and Related Materials*, 2025.

[15] T. Kimoto, T. Kobayashi and a. K. Tachiki, "SiC semiconductor device manufacturing method and SiC semiconductor device". United States Patent Application No. 2023/0307503 A1, 28 Sep 2023.

[16] X. Yang, B. Lee and V. Misra, "Electrical Characteristics of SiO2 Deposited by Atomic Layer Deposition on 4H–SiC After Nitrous Oxide Anneal," *IEEE Transactions on Electron Devices,* vol. 63, p. 2826, 2016.