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Characterizations of 4H-SiC/SiO_2 Interface by High-Temperature N_2/H_2 Pretreatment

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Abstract. In this work, we present a process flow to optimize the SiC/SiO_2 gate interface quality for SiC power MOSFETs. The process incorporates high-temperature N_2/H_2 pretreatment, followed by LPCVD SiO_2 deposition and NO post-deposition annealing (PDA). By tailoring the pretreatment conditions, a substantially improved SiC/SiO_2 interface with reduced interface trap density (D_{it}) can be achieved. Furthermore, the gate oxide quality is also characterized by measuring the leakage current and time-dependent dielectric breakdown (TDDB). The results indicate a noticeable improvement in the average breakdown field (E_{ox}), thanks to the enhanced SiC surface condition achieved by the N_2/H_2 pretreatment.

Introduction

Despite the on-going commercialization, the 4H-SiC power MOSFET still suffers from the trap-rich SiC/SiO_2 MOS gate interface, which affects the field-effect MOS channel mobility, threshold voltage stability, and device lifetime. Attempts to improve the SiC/SiO_2 MOS gate interface should continue for improved device performance and reliability. Carbon-related defects (i.e., the carbon clusters) generated during the thermal oxidation process of SiC are identified as a predominant contributor to the high D_{it} level [1].

Preventing the thermal oxidation of SiC surface during which the high oxidation temperature (~1,200 ºC) could lead to carbon accumulation at the interface, e.g., replacing thermal oxide with deposited oxide (at lower temperature), has been experimented to eliminate the carbon-related defects, thereby improving the quality of SiC/SiO_2 interface [2-3]. Nevertheless, carbon-related defects can still form during sacrificial oxidation process. Therefore, an appropriate pretreatment prior to the gate oxide deposition is needed to remove the existing carbon-related defects, thereby obtaining a high-quality SiC surface for the subsequent gate oxide deposition process.

In this work, we present a process flow that integrates high temperature N_2/H_2 pretreatment, LPCVD SiO_2 deposition, and NO post deposition annealing (PDA) to optimize the quality of SiC/SiO_2 interface. The hydrogen-containing pretreatment enables effective removal of the carbon-related defects through a layer-by-layer etching process of the defective layers at the SiC surface, preparing a high-quality SiC surface [4]. The LPCVD deposition at 420 ºC effectively avoids the thermal oxidation of SiC and the associated carbon clusters, and the subsequent NO PDA further passivates the interface states, pursuing a high-quality SiC/SiO_2 gate interface for improved device performance.

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Experiment

SiC/SiO_2 MOS capacitors were fabricated on an n-type 4H-SiC (0001) epilayer (donor density: 1×10^{16} cm^{-3}) grown on a n-type substrate [Fig. 1]. The fabrication process starts with a surface pretreatment in a furnace under a gas atmosphere of 95% N_2 and 5% H_2 at atmospheric pressure. Compared with the pretreatment etching by pure H_2 [2-3], such N_2/H_2 gas composition is compatible with standard industrial furnace with high level of safety. Subsequently, a gate oxide layer of ~ 55 nm was deposited by LPCVD at 420 °C. Afterwards, NO PDA was performed at 1250 °C for 70 min for interface passivation. Finally, circular Al front electrode (diameter: 400 μm) and Al back contact were deposited and sintered. Following device fabrication, electrical measurements (*C–V* and *I–V)* and material characterization were performed to evaluate the impact of the proposed process and gain insights into the underlying physical mechanisms.

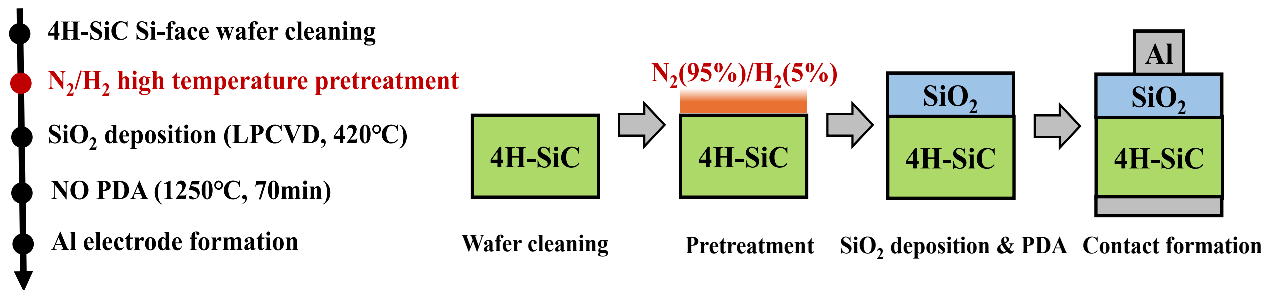

Fig. 1. Procedure and schematic of the proposed fabrication process of MOS capacitors.

Results and Discussion

To evaluate the quality of SiC/SiO_2 interface, D_{it} near the conduction band edge (E_c) is extracted from the C-V results by using high (100 kHz)-low (quasi-static) method. Fig. 2 (a) shows the D_{it} distribution profiles of samples pretreated in N_2/H_2 mixture gas at 1350 °C for different treatment time duration. The lowest D_{it} level is obtained in the 30-min sample. Further prolonging the pretreatment time to 40 min leads to a noticeable increase of D_{it}, especially in shallow levels close to E_c. The results could be attributed to the layer-by-layer etching process of the SiC defective surface layers by H_2. With 30-min pretreatment, a clean Si-rich layer is exposed with the lowest level of D_{it}, but further extending the pretreatment time to 40 min exposes the underlying C-rich layer that inherently leads to higher density of D_{it}. In addition, two Nitrogen-based treatments, i.e., the N_2/H_2 pretreatment and the NO PDA, could both introduce Nitrogen atoms to passivate the SiC/SiO_2 interface and improve its quality. The XPS C 1s spectra of samples without pretreatment and with a 30-min pretreatment were analyzed and compared. The C–C/C–Si ratio decreases from 0.038 to 0.026 after pretreatment, indicating an effective reduction of carbon clusters on the SiC surface due to the N_2/H_2 pretreatment.

The temperature dependence of the D_{it} level during the 30-min N_2/H_2 pretreatment is also investigated [Fig. 2 (b)]. Samples pretreated at 1350 °C exhibits the lowest D_{it} level. At higher temperature (1350 °C), the accelerated etching and passivation reactions outweigh the trap generation from Si–C bond breaking, so the trap removal and passivation process dominants.

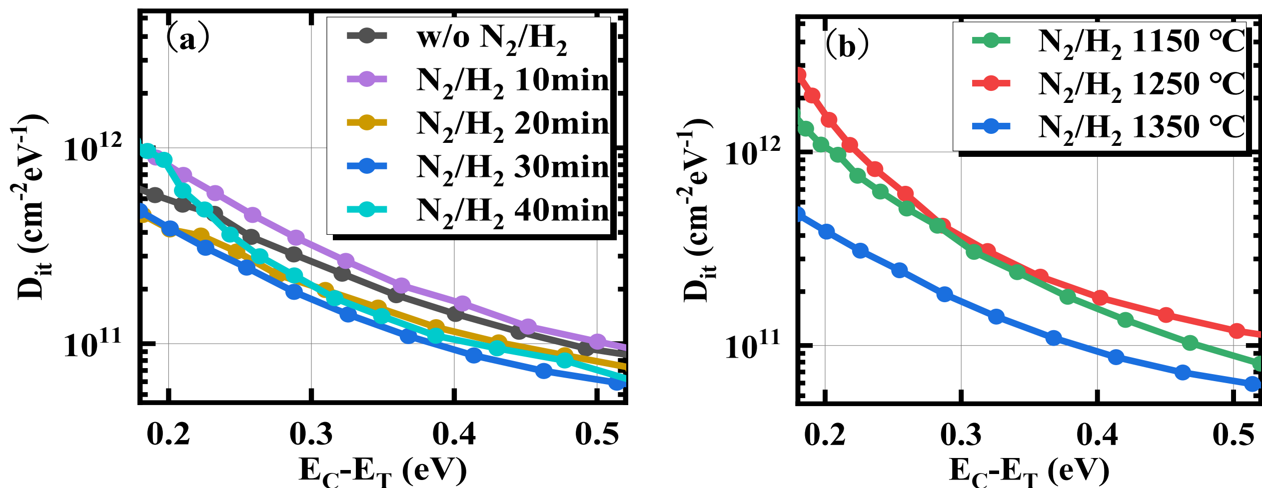

Fig. 2. Energy distribution of D_{it} extracted from samples with different pretreatment (a) time duration and (b) temperature.

The layer-by-layer etching process of H_2 is verified by the AFM image of the SiC surface selective region pretreatment experiment [Fig. 3]. A layer of SiO_2 is deposited and patterned to expose a selected SiC surface region to the N_2/H_2 pretreatment. After the 30-min N_2/H_2 pretreatment at 1350 °C, a Si-C bilayer of ~ 0.5 nm is removed from the SiC surface, exposing the Si-rich surface to improve the quality of SiC/SiO_2 interface.

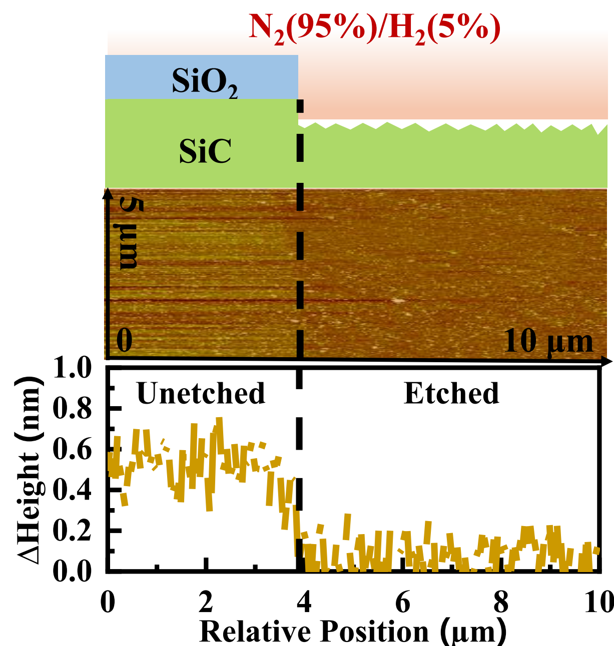

Fig. 3. AFM image after selective region N_2/H_2 pretreatment.

Any performance benefit introduced by optimizing the fabrication process should come without a penalty in the gate oxide reliability. Most reliability-relevant characteristics including the leakage current and time-dependent dielectric breakdown of the gate oxide from samples with and without the pretreatment (1350 °C for 30 min) were compared. Both the leakage current and the breakdown electric field indicate the N_2/H_2 pretreatment does not negatively affect the gate oxide quality [Fig. 4 (a)]. Based on the statistical distribution of oxide breakdown electric field in Fig. 4 (b), the devices with N_2/H_2 pretreatment show a noticeable increase in the average E_{ox}, indicating a better SiC surface was prepared for gate oxide deposition. The relatively large dispersion in the E_{ox} distribution under both conditions is primarily attributed to intrinsic process-induced variations in oxide quality.

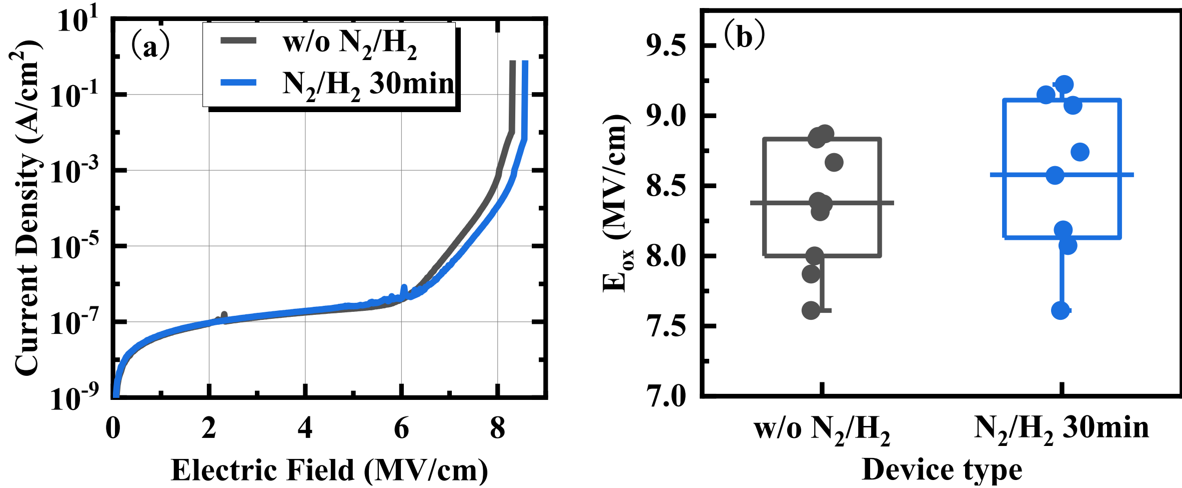

Fig. 4. (a) Insulating properties of MOS capacitors with and without the pretreatment. (b) Statistical chart of E_{ox} for the two samples.

TDDB test was further performed at room temperature to evaluate the reliability of the gate oxide pretreated at 1350 °C for 30 min [Fig.5 (a)]. The stress electric field is 8 MV/cm, 8.25 MV/cm, and 8.5 MV/cm, with the corresponding Weibull slope (β) value of 0.98, 1.16, and 0.94. This value is relatively low in comparison to that of thermal oxide [5], which is attributed to the compromised quality of the LTO. To project the lifetime of the fabricated MOS capacitors, $t_{63\%}$ is plotted against the applied gate electric field, as shown in Fig. 5 (b). From the projection, the lifetime of these devices can reach 10 years at room temperature with a maximum operating electric field of 6.74 MV/cm.

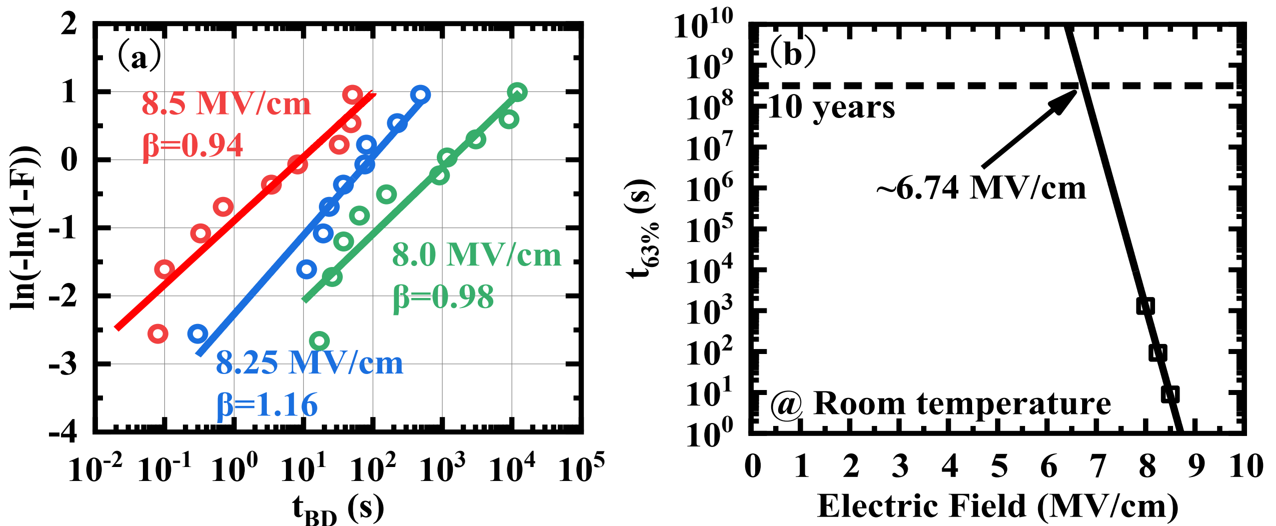

Fig. 5. (a) Weibull distributions of devices failures at various electric fields; (b) Ten-year lifetime predictions by choosing 63% failure rate.

Summary

To conclude, the discussed process that integrates N_2/H_2 pretreatment, gate oxide deposition, and NO post deposition annealing demonstrated effective improvement of the SiC/SiO_2 interface by removing the thermal-oxidation-related carbon clusters and the associated D_{it}. Meanwhile, the quality of the gate oxide is not compromised by the pretreatment process, which could be further improved by optimizing the deposition method and conditions.

Acknowledgement

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References

[1] Z. Wang, Z. Zhang, S. Liu, C. Shao, J. Robertson, and Y. Guo, Impact of carbon–carbon defects at the SiO_2/4H-SiC (0001) interface: a first-principles calculation, Journal of Physics D: Applied Physics 55.2 (2021): 025109.

[2] K. Tachiki, M. Kaneko, and T. Kimoto, Mobility improvement of 4H-SiC (0001) MOSFETs by a three-step process of H_2 etching, SiO_2 deposition, and interface nitridation, Applied physics express 14.3 (2021): 031001.

[3] K. Tachiki, M. Kaneko, T. Kobayashi, and T. Kimoto, Formation of high-quality SiC (0001)/SiO_2 structures by excluding oxidation process with H_2 etching before SiO_2 deposition and high-temperature N_2 annealing, Applied physics express 13.12 (2020): 121002.

[4] S. Glass, F. Reis, M. Bauernfeind, J. Aulbach, M. R. Scholz, F. Adler, L. Dudy, G. Li, R. Claessen, and J. Schäfer, Atomic-Scale Mapping of Layer-by-Layer Hydrogen Etching and Passivation of SiC (0001) Substrates, The Journal of Physical Chemistry C 120.19 (2016): 10361-10367.

[5] B. Tsui, Y. Huang, T. Wu, and C. Chien, Time-dependent dielectric breakdown of gate oxide on 4H-SiC with different oxidation processes, Microelectronics Reliability 123 (2021): 114186.