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Preliminary Study into Ferroelectric Properties of ALD Al-Doped HfO_2/SiO_2/4H-SiC MOS Capacitors for Improved Short Circuit Reliability

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Abstract. We investigate the physical and electrical characteristics of the Al-doped or undoped HfO_2/SiO_2 gate stacks on 4H-SiC by testing MOSCAP chips fabricated in house. A clear reduction in accumulation capacitance (C_{ox}) with increasing chuck temperature from room temperature up to 523 K is observed, with Al-doping playing a key role and aligning with temperature-dependent Landau ferroelectric theory. Chips annealed at 1100℃ in N_2 ambient show the highest C_{ox} decrease rates while maintaining functional MOS interfaces with acceptable flatband voltage, hysteresis, and D_{it} profiles. TCAD simulations on a double trench MOSFET model, based on the extracted data indicate improved electro-thermal performance, demonstrating that Al-doped HfO_2/SiO_2 gate stacks are a promising approach for enhancing 4H-SiC power devices.

Introduction

Silicon Carbide (SiC) has several material advantages over silicon (Si) in power electronics applications, such as its wider bandgap, higher breakdown voltage, and higher operating temperatures of SiC devices. Hence, they could be used for making more efficient power-dense 4H-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) with lower on-resistances (R_{on}). Problems surrounding reliability under harsh conditions are still a challenge in 4H-SiC technology in this field. Short-circuit (SC) withstand time has been one of the challenges extensively researched, as the withstand times in 1.2kV 4H-SiC MOSFETs have been low compared to their lower-rated 650V counterparts [1]. Through Landau's theory of the temperature dependence of the dielectric constant and accumulation capacitance (C_{ox}) in ferroelectric materials [2], the solution proposed was the integration of a ferroelectric hafnium oxide (HfO_2)/ silicon dioxide (SiO_2) gate-stack as the gate dielectric, which led to decreased peak current leakage and peak device temperature, resulting in improved electro-thermal behaviour of the device [3, 4]. This is based on the ferroelectric/paraelectric capacitance model from Landau's theory, where the dielectric permittivity increases up to when the operation temperature (T) reaches the Curie-Weiss temperature (T_{CW}), but then decreases when T is above the T_{CW} [2]. Research in ferroelectricity of HfO_2 has shown that doping the HfO_2 layer with different dopants, such as Si or aluminium (Al) could enhance the ferroelectric property of HfO_2 [5, 6]. Therefore, the investigation will involve doped-HfO_2/SiO_2/4H-SiC MOS capacitor (MOSCAPs) chips.

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In this study, the electrical performance and structural properties of the atomic layer deposited (ALD) Al-doped HfO_2/SiO_2/4H-SiC will be investigated. The focus will be on the C_{ox} change rate at increasing chuck temperatures against room temperature (RT) for the validity of Landau's theory. Flatband voltage (V_{FB}), hysteresis and density interface traps (D_{it}) at RT are also investigated for studying the electrical reliability and integrity of the MOS interface.

Methodology

For the fabrication of the MOSCAP chips in this investigation, seven 1 cm × 1 cm chips have been cleaved from a 10 µm thick wafer consisting of an epitaxially grown light nitrogen-doped (1×10^{16} cm^{-3}) drift layer on top of a heavy nitrogen-doped (>1 x 10^{20} cm^{-3}) 4H-SiC substrate. The cleaved chips then underwent standard RCA cleaning with an: HF(10%)/ RCA1/ HF(10%)/ RCA2/ HF(10%), cleaning cycle. For the deposition of the HfO_2/SiO_2 gate-stack, 6 nm of SiO_2 was deposited followed by 30 nm of doped/undoped HfO_2 on top. Oxygen plasma is the oxidant of choice along with bis(diethylamido)silane (BDEAS) and tetrakis(dimethylamido)hafnium (TDMAHf) as Si and Hf precursors. This is all done by plasma-enhanced ALD (PE-ALD) at 200°C with the Ultratech Fiji G2 PE-ALD system. For Al-doped HfO_2 layers ALD cycles ratios of 1:19 and 1:29 of the Al_2O_3:HfO_2 have been used to produce the Al-HfO_2/SiO_2/4H-SiC MOSCAP chips. Post deposition annealing (PDA) was done on the chips in nitrogen (N_2) ambient for one hour leading to a following list of MOSCAP chips produced:

1. **Undoped HfO_2**/SiO_2/4H-SiC MOSCAP chips annealed in a quartz furnace at 900°C, 1000°C, or 1100°C.
2. **Al-doped:HfO_2**/SiO_2/4H-SiC MOSCAP chips annealed at 900°C, 1000°C, or 1100°C.

500 nm thick aluminium contacts were deposited on the top and bottom of the chips by means of metal sputtering to complete the fabrication of the devices. The top contacts were circular with a surface area of 1.26×10^{-3} cm^2. The bottom surface of the chip was dry etched for the formation of the ohmic contact, before the bottom contact was deposited.

High-low frequency variant ±10V capacitance-voltage (C-V) sweeps were conducted on at least 15 MOSCAP devices on each chip, with the average V_{FB}, hysteresis and D_{it} were extracted at room temperature (RT) (293K). D_{it} profiles of each MOSCAP device are extracted by the high-low frequency method with 100 Hz being the lowest frequency and 1 MHz being the highest frequency, using an Agilent E4980A LCR meter. High frequency C-V sweeps at varying probe station chuck temperature points (between 293K – lowest and 523K – highest) were performed on the MOSCAP chips; V_{FB}, hysteresis and C_{ox} (at +10V) measurements were obtained at those various temperature points. A previously characterised ALD-SiO_2/4H-SiC MOSCAP served as a reference for comparative electrical benchmarking. Grazing-incidence X-ray diffraction (GIXRD) measurements are conducted on the HfO_2 surface for determining the crystal phase of the HfO_2 film after a PDA; further structural analysis and the layer thicknesses have been verified by scanning transmission electron microscopy (STEM).

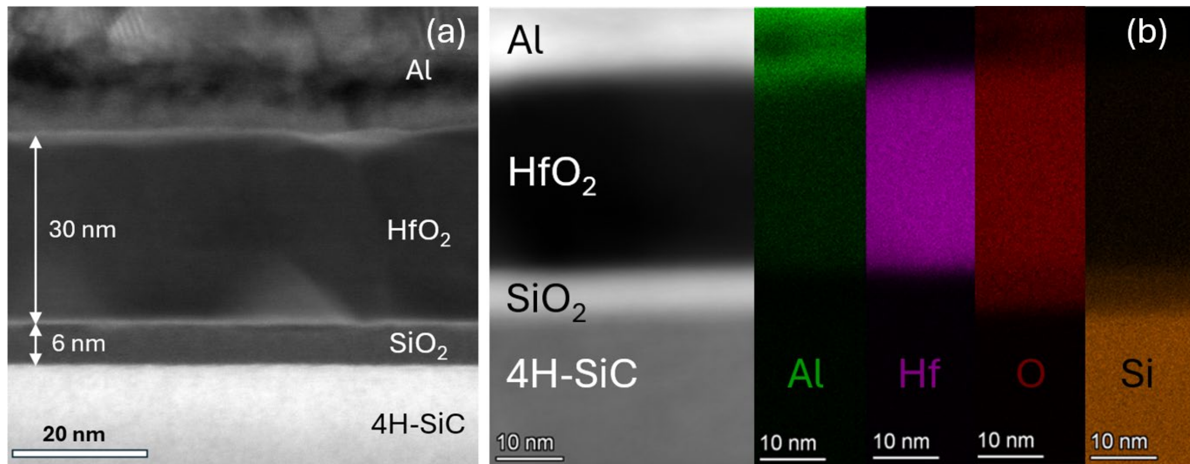

Fig. 1. A TEM scan verifying the thickness of (a) deposited stacked dielectric as well the (b) element composition.

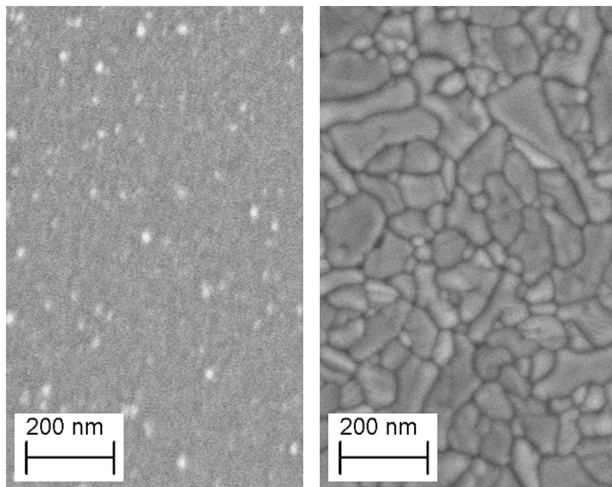

Fig. 2. SEM images of a unannealed (left) and N2 1100°C annealed (right) MOS structure.

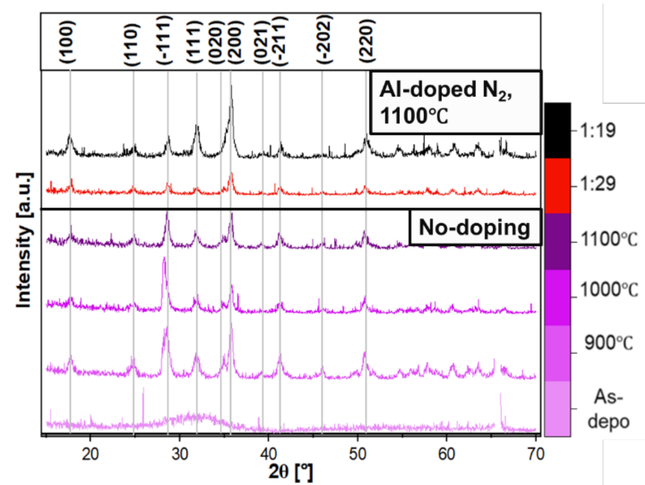

Fig. 3. GIXRD measurements of the undoped/doped HfO_2 films on SiO_2/4H-SiC.

Physical Characterisation

The STEM analysis of the N_2 1100°C annealed gate-stack MOS interface cross-section, shown in fig. 1, has confirmed the thicknesses of each insulator in the gate stack. Some crystallinity could be observed in the HfO_2 layer from the STEM analysis. This detected crystallinity is like the crystallinity detected on HfO_2 layers annealed on Si [9]. Comparative SEM conducted on an as-deposited layer of

HfO_2 and then a N_2 1100°C annealed (both on separate chips of SiO_2/4H-SiC), have been done as shown in fig. 2. Fig. 2 depicts the grains of the annealed HfO_2 to be greater than that of the as-deposited HfO_2. Similar trends have also been seen on as-deposited or 700°C annealed 500nm thick HfO_2 films on Si, where the method of deposition was by electron beam evaporation [10]. GIXRD results of fig. 3, show that for all the chips that underwent a high temperature PDA, a monoclinic crystal phase has been detected on the HfO_2 film, which is synonymous with paraelectric properties of HfO_2 [5]. Thus, links with the paraelectric phase of the ferroelectric theory could be established, especially the C_{ox} decrease at higher chuck temperatures.

Electrical Results

Fig. 4 shows normalised high-frequency C-V sweep results of a MOSCAP device taken from a 1:19 Al-doped HfO_2/SiO_2/4H-SiC chip annealed at 1100°C in N_2 at varying chuck temperatures. All recorded capacitance values have been referenced to the C_{ox} at RT. A C_{ox} (at +10V) decreased by 15%

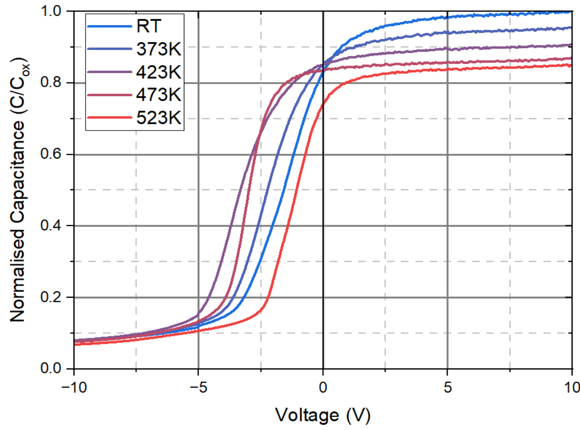

Fig. 4. Normalised Capacitance-Voltage sweep of a device on an Al_2O_3:HfO_2 1:19 Al-doped MOSCAP chip.

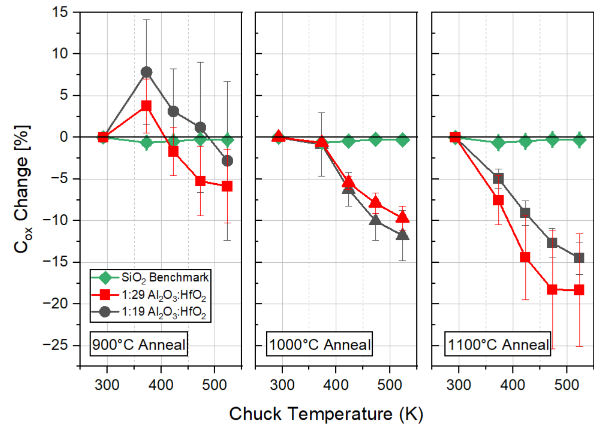

Fig. 5. C_{ox} change vs chuck temperature results for all the PDA Al-doped HfO_2/SiO_2 gate-stack and SiO_2 benchmark MOSCAP chips.

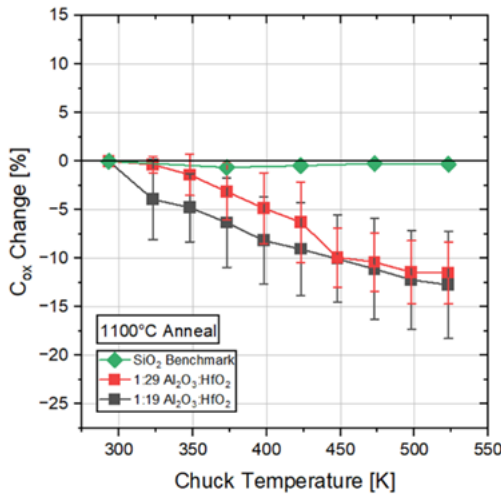

Fig. 6. C_{ox} change vs Chuck Temperature on retested MOSCAP devices.

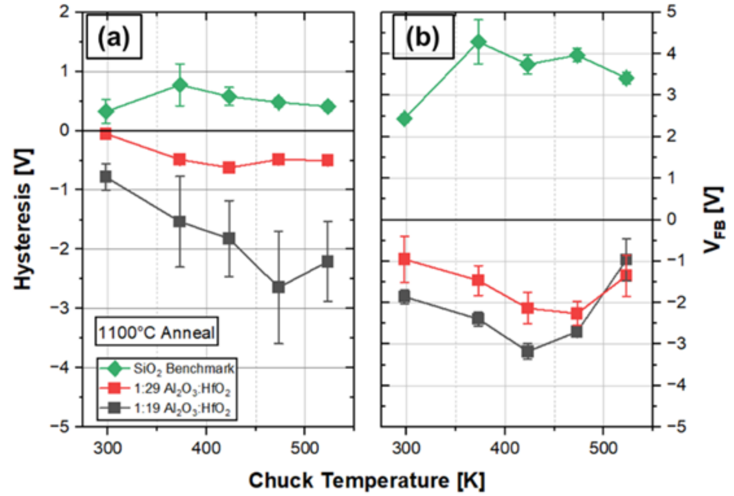

Fig. 7. (a) Hysteresis and (b) V_{FB} results at varying chuck temperatures.

has been recorded as the chuck temperature rose from RT to 523K. This result partially supports Landau's theory of temperature dependence on C_{ox} in ferroelectric materials, especially in the paraelectric phase [2]. Fig. 5 shows the average C_{ox} change rate for all Al-doped gate stack MOSCAP chips in comparison to the ALD-SiO_2 benchmark chip [7] at rising chuck temperatures (in 50K increments). These results show that, regardless of the deposition cycles for the Al-doped HfO_2, the PDA temperature of 1100°C leads to the most favourable trends in C_{ox} reduction rate with rising chuck temperatures; Hence, the doped MOSCAP chips annealed at 1100°C have been taken further for further study. Cox change rate for the benchmark MOSCAP chip has been close to zero regardless of chuck temperature level. Moreover, high-frequency C-V sweeps, even with smaller chuck temperature increments of 25K, have been conducted on a new set of MOSCAP devices on chips annealed at 1100 °C (fig. 6), further confirming the decreasing Cox trend (Fig. 5). This experimentally confirms a similar trend, also observed in silicon-on-insulator MOSFET devices [8].

Fig. 7a and 7b show the average hysteresis and VFB results at varying chuck temperature points for the MOSCAP chips. At all chuck temperature levels, the V_{FB} is shown to be closer to the ideal V_{FB} of Φ_{MS} than that of the ALD-SiO_2 benchmark. The hysteresis for the MOS interfaces is calculated using Eq. (1); therefore, a positive value indicates that negative charge is trapped in the MOS interface, but a negative value indicates that positive charge is trapped. Fig. 4b shows that positive

charges are trapped in the interface for the Al-doped gate stacks at all chuck temperature points, whereas negative charges are trapped for the ALD-SiO_2 benchmark interface.

$$Hysteresis = V_{FB\ (Acc.\rightarrow Inv.)} - V_{FB\ (Inv.\rightarrow Acc.)} \quad (1)$$

Fig. 8 shows the RT D_{it} profile results of the Al-doped/undoped gate stacks and the ALD-SiO_2 benchmark. The D_{it} profile results are lower than 10^{12} $eV^{-1}cm^{-2}$ even when at 0.2 eV. Such results confirm that Al-doped gate-stacks can also make functional 4H-MOS interfaces.

TCAD Simulations Based on Experimental Results

SC TCAD simulations have been conducted on a double trench MOSFET [11] employing similar methods for temperature-dependent dielectric constant (ε) curve fitting of the N_2, 1100℃ annealed 1:19 (Al_2O_3:HfO_2)/SiO_2 gate-stack and SC testing parameters, as of [3]. Fig. 9 shows the curve results of the curve fitting for the ε vs chuck temperature based on the electrical characterisation results. Given that no changes have been made on the design dimensions of the double trench MOSFET device, except for the gate insulator, it shows that there is improved electro-thermal performance when the temperature-dependent gate-stack has been adopted over the SiO_2 gate insulator. Fig. 10 shows the responses of the MOSFET drain current (I_D) and the maximum lattice temperature (T_{MAX}) when under SC stress. Besides the lower peak I_D and T_{MAX} for the MOSFET that adopted the temperature-dependent ε gate-stack, the SC withstand time (SCWT) also increased by 2 µs.

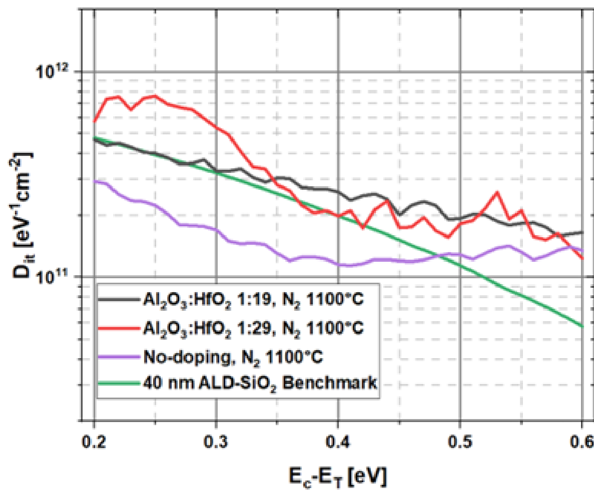

Fig. 8. D_{it} profile results of the MOS interfaces of different gate insulator options.

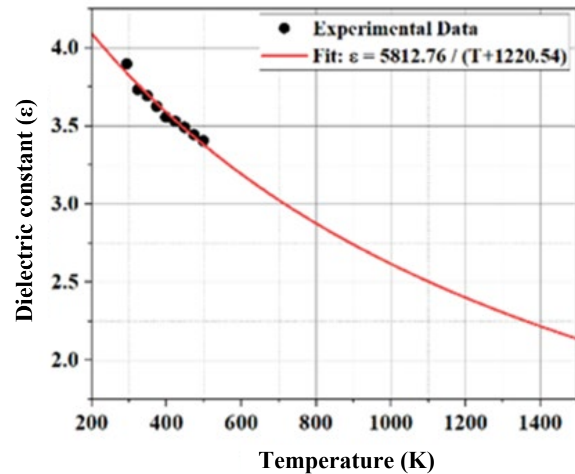

Fig. 9. Dielectric constant (ε) vs Chuck temperature curve fit.

A comparative T_{MAX} in the TCAD MOSFET lattice model switching from the SiO_2 (fig. 11a) to the doped gate-stack (fig. 11b) have recorded a decrease in lattice temperature from 1286K to 1229K.

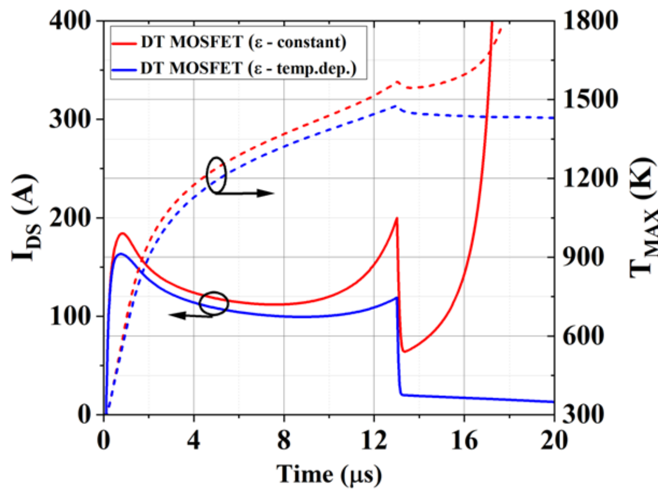

Fig. 10. Simulated SC I_D and T_{MAX} for the DT MOSFET with constant SiO_2 (red) and temperature dependent HfO_2/SiO_2 gate-stack gate insulator (blue).

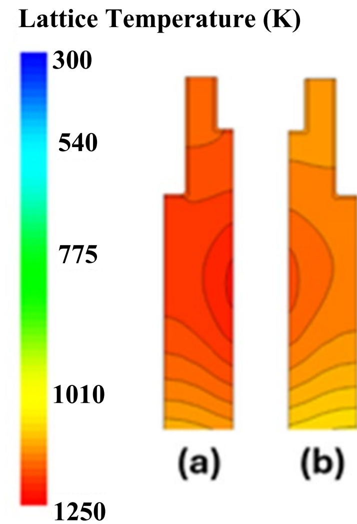

Fig. 11. Lattice temperature distribution in the simulated TCAD double trench MOSFET model with (a) constant SiO_2 or (b) temperature dependent HfO_2/SiO_2 gate stack.

Conclusion

Ferroelectric/Paraelectric properties of HfO_2 on SiO_2/4H-SiC have been investigated for the first time both physically and electrically on various materials/electrical characterisation methods. The physical characterisation through GIXRD and SEM reveals that the doped/undoped HfO_2 layers that underwent a high-temperature PDA all exhibit a monoclinic (P21/c) crystal phase, which may justify the C_{ox} decrease against the rising chuck temperature. Chips that underwent a PDA of 1100℃ in N_2 ambient led to the highest rates of C_{ox} decreases between -13% and -18% from RT to 523K. Furthermore, the V_{FB}/hysteresis vs chuck temperature, and RT D_{it} profile results, all show that the gate-stack could still lead to functional and efficient MOS interfaces for 4H-SiC power MOS devices. Simulation results on a TCAD double trench MOSFET model, based on experimental data of this study, show improved electro-thermal performance when utilising the gate-stack as an alternative.

This study demonstrated that Al-doped HfO_2/SiO_2 gate-stacks could be a viable gate insulator option in SiC power devices. Further investigations into the stability of pure-ferroelectric property of HfO_2 should be conducted in the future, with some changes to be made to the HfO_2 doping ratios and the PDA process step thermal budget during the fabrication process of future gate-stack MOSCAP chips. The suitability of those gate stacks for MOSFET device integration will also encompass D_{it} (for channel mobility) and voltage breakdown (for gate leakage) parameters, as the polycrystalline nature of high temperature PDA HfO_2 could sometimes lead to current leakage through the HfO_2 layer [12].

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