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High-Temperature H_2- and N_2-Containing Surface Conditioning for SiO_2/4H-SiC Interface Optimization

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Abstract. In this paper, we study high-temperature H_2, N_2, and H_2/N_2 surface conditioning processes prior to the SiO_2 deposition as a promising approach for SiO_2/4H-SiC interface preparation in metal-oxide-semiconductor field-effect transistors (MOSFET). A thorough electrical analysis is presented, consisting of temperature-dependent transfer characteristics as well as reliability studies regarding bias temperature instabilities (BTI) and dielectric breakdown behavior. Especially N_2-containing surface pretreatments were found to greatly suppress electron traps, whereas hole trapping is enhanced. Finally, X-ray photoelectron spectroscopy (XPS) was utilized to elucidate the elemental surface composition after the different annealing procedures. The obtained results are in good agreement with the electrical characterization and complement already published results regarding the formation of surface reconstructions on 4H-SiC through H_2 and H_2/N_2 annealings.

Introduction

Within the recent years, the SiC power MOSFET market has been massively grown. The wide bandgap of the 4H-SiC material comes along with a high breakdown field strength, offering the possibility of shrinking the drift zone thickness and ultimately its resistance contribution. Together with other superior physical properties like a high thermal conductivity, 4H-SiC is expected to continuously replace Si-based devices in high-voltage, energy-efficient power electronics application. A fundamental building block of every MOSFET device is the oxide-semiconductor interface. Despite the ongoing efforts to improve the SiO_2/4H-SiC interfacial quality, the resulting channel mobility remains below expectation. Hence, metal-oxide-semiconductor (MOS) channel engineering is still a highly interesting matter of applied research.

With progressing scientific achievements in the field of SiO_2/4H-SiC interface improvement, it is nowadays common knowledge, that thermal oxidation of 4H-SiC creates various defect states, located at different energetic levels. Exchanging a thermally grown by a deposited SiO_2 gate oxide, however, turned out to yield a more abrupt material transition, if combined with an appropriate post-deposition annealing (PDA) process [1]. Hence, low pressure chemical vapor deposition (LPCVD) became the method of choice for high-quality gate oxide formation in 4H-SiC MOSFETs. Along with the transition to deposited gate oxides, the investigation of appropriate surface pretreatment processes prior to the dielectric deposition gained growing scientific interest. In this regard, especially H_2-based, high-temperature surface conditioning in combination with a deposited SiO_2 gate oxide was recently shown to offer a substantial increase in the channel mobility [2,3]. Even if the physical origin of the remarkable performance improvement is not yet fully understood, it is speculated, that mobility-limiting defects are heavily reduced by H_2 conditioning together with avoiding substrate oxidation.

The surface configuration of H_2-annealed Si-face (0001) 4H-SiC is a matter of scientific interest since decades. Within the published studies, several hints to explain the recently shown mobility improvement can be found. Typically, upon H_2 annealing, highly ordered silicate adlayers have been

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observed, which provide an atomically sharp, epitaxial material transition to the underlying 4H-SiC [4]. Such silicate layers are expected to provide a well-suited seed layer for subsequent SiO_2 deposition. However, it was found out, that the resulting surface reconstruction leaves behind an unsaturated bond per unit cell, which forms a mid-gap interface state. In this regard, researchers discovered an even more promising surface structure by adding a N_2 annealing subsequent to the H_2 treatment [5]. Such a combined H_2/N_2 surface treatment was proven to form an epitaxial silicon oxynitride (SiON) adlayer in a self-limiting manner, which potentially serves as an ideal insulator/4H-SiC transition due to the absence of dangling bonds. Even if first attempts to transfer those theoretical predictions to simple MOS capacitor devices have been published by Rozen *et al.* [6], to the best of our knowledge, there exists no successful demonstration on 4H-SiC MOSFET devices. In this work, we close this gap by investigating the effect of high-temperature H_2, N_2 and H_2/N_2 surface conditioning processes on the electrical performance of lateral 4H-SiC MOSFETs. Besides a thorough evaluation of the resulting transfer characteristics, reliability aspects of the processed gate oxides are discussed. Finally, the electrical results are correlated with XPS analysis.

Experimental

To study the effect of different high-temperature surface conditioning processes, we fabricated lateral, long channel MOSFET devices on epitaxial n-type layers, grown on conventional 4°-off axis (0001) 4H-SiC 6” substrates. A schematic cross section of the MOSFET devices is shown in Fig. 1 together with the detailed process chain of the investigated gate formation procedures. To prepare the wafers for the variation in high-temperature surface conditioning, three subsequent ion implantation steps were conducted. In a first step, Al was implanted as a p-type dopant to create the channel region. Subsequently, a surrounding p-type border was implanted with a higher Al dose, which later serves as ohmic contact, connecting the channel region to ground potential during electrical characterization. Finally, highly doped n-type source and drain regions were formed by implanting ionized N atoms. Except the ion implantation steps, device fabrication took place in the corporate research cleanroom of the Robert Bosch GmbH. Following the implantation block, dopant activation was conducted by the state-of-the-art process of high-temperature annealing with the wafer surface being covered by a C capping.

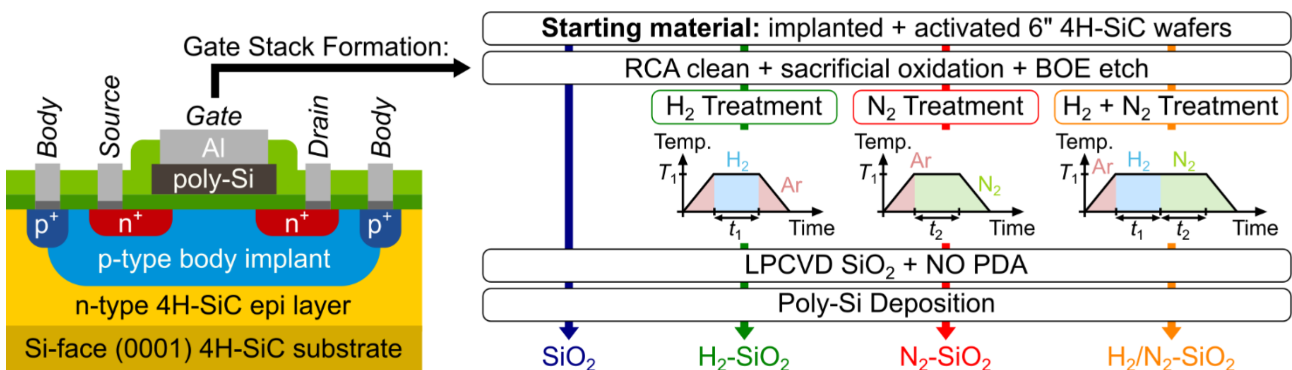

Fig. 1. Schematic cross section of the fabricated long channel MOSFET devices. Process chain and details regarding the gate stack formation including the surface conditioning procedures are given on the right side together with the respective sample nomenclature.

Prior to the surface conditioning processes, the wafers were cleaned to subsequently grow a sacrificial oxide layer, which is removed in a wet buffered oxide etch (BOE) solution. Right after, the wafers were processed according to the fabrication scheme, shown in Fig. 1. As a baseline for comparing the electrical results, a reference sample without additional surface treatment, denoted as “SiO_2”, was fabricated. All other samples underwent a dedicated high-temperature surface conditioning process, namely H_2, N_2 and a combination thereof. The respective processing conditions in terms of temperature profile over time and gas ambient are schematically provided in Fig. 1. All pretreatment processes were performed ex-situ to the subsequent LPCVD SiO_2 formation. However,

the anticipated surface passivation layers upon H_2 and H_2/N_2 annealing are published to be very stable against air exposure [4,5]. After the surface conditioning processes, all wafers were put together and processed nominally the same. SiO_2 gate dielectrics were deposited by means of LPCVD and annealed in NO ambient at moderate temperatures to avoid reoxidation of interfacial layers. An in-situ P doped LPCVD poly-Si layer was subsequently deposited as gate electrode material. Following a dry etching step to structure the poly-Si, a thick SiO_2 insulation layer was formed to encapsulate the MOS stack, again via a LPCVD process. Afterwards, electrical contacts to the source, drain, gate and bulk regions had to be defined. Starting with the ohmic contacts to the 4H-SiC, the insulation layer was selectively etched in dedicated areas, followed by NiSi formation via sputtering and rapid thermal annealing (RTA) at elevated temperatures. Finally, to ensure a reliable needle contact to the MOSFET terminals during electrical characterization, thick Al contact pads were formed.

The fabricated MOSFET devices were electrically characterized in a Cascade Microtech probe station. A Keithley 2636 sourcemeter was connected to the probe station to record transfer characteristics and perform BTI, time-zero dielectric breakdown (TZDB) and constant voltage time-dependent dielectric breakdown (TDDB) analysis. For analyzing the atomic surface configuration, XPS characterization was carried out in a PHI Quantera II equipment. Si2p, C1s, O1s and N1s core level spectra were acquired by using a monochromatic Al K_α x-ray source with a take-off angle of 45°. The resulting diameter of the analyzed area is roughly 200 µm.

Results and Discussion

Fig. 2 a)-c) present the transfer characteristics of our devices. In Fig. 2 a), the linear drain current I_D curve traces of one exemplary device per wafer are shown. The gate voltage V_G was swept in 0.1 V steps from -5 V to +25 V and vice versa. The drain voltage V_D was set to 0.3 V. To better compare the turn-on characteristics of the differently processed MOSFETs, a logarithmic illustration of I_D in the voltage range 0 V < V_G < 4 V is given in Fig. 2 b). Out of the results in Fig. 2 a) and b), the peak field-effect mobility μ_{FE}, threshold voltage V_{th} and sub-threshold hysteresis $\Delta V_{sub\text{-}th}$ are extracted and shown as box plots in Fig. 2 c) for a statistics of 16 devices per wafer.

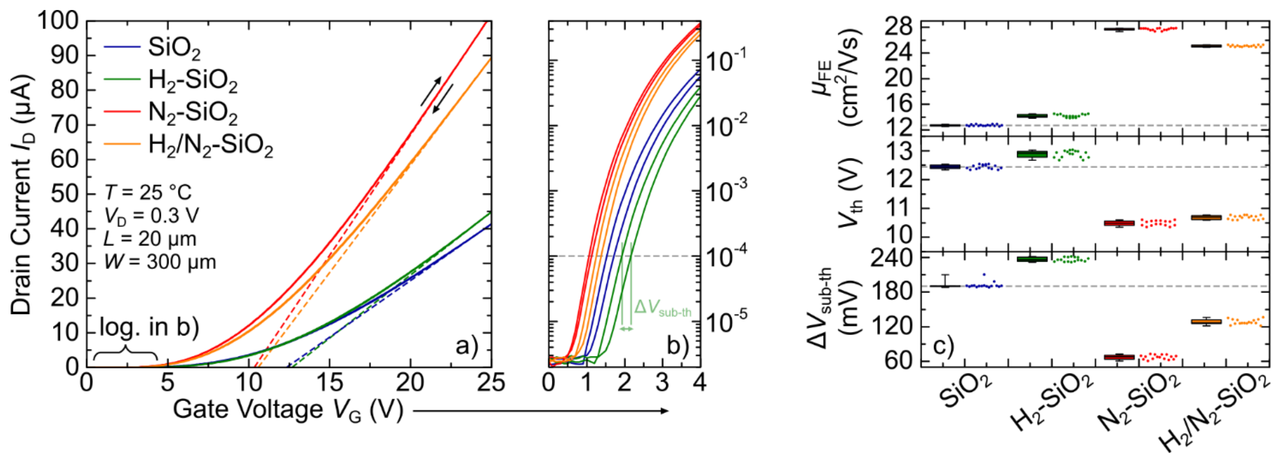

Fig. 2. a) Linear transfer characteristics of one exemplary MOSFET device per wafer with a channel length L = 20 µm and width W = 300 µm. The measurements were done at room temperature. An extrapolation in the linear curve regime is sketched by dashed lines to indicate the V_{th} extraction. The I_D-V_G turn-on behavior is shown in b) in logarithmic scale. The current level to extract $\Delta V_{sub\text{-}th}$ between up- and down-sweep direction is illustrated by the dashed line. The characteristic MOSFET parameters μ_{FE}, V_{th} and $\Delta V_{sub\text{-}th}$ are derived for 16 devices per sample and shown as box plots in c). The dashed lines indicate the reference level of the SiO_2 wafer.

Comparing all wafers, a substantial μ_{FE} improvement of up to 2.2 times the reference value as well as a reduced $\Delta V_{sub\text{-}th}$ value is observed for both wafers, which have been processed with N_2-containing surface conditioning. Furthermore, the N_2-SiO_2 and H_2/N_2-SiO_2 devices turn on with a significantly steeper I_D-V_G slope, as shown in Fig. 2 b). Those aspects clearly reveal a superior SiO_2/4H-SiC

interface quality after N_2-containing surface pretreatment. Comparing the N_2-SiO_2 to the H_2/N_2-SiO_2 sample, the N_2-alone process seems to be even more effective to boost the MOSFET's performance. Interestingly, in contrast to the published results [2,3], the H_2 surface conditioning process just marginally improves μ_{FE}, while energetically deeper interface states are even slightly increased, as $\Delta V_{sub\text{-}th}$ is enlarged and the onset of I_D increase is delayed, as compared to the SiO_2 reference wafer.

To get further insights regarding the SiO_2/4H-SiC interface quality upon the investigated pretreatment processes, the temperature dependence of V_{th} and μ_{FE} was evaluated by measuring the transfer curves between 25 °C and 175 °C in 25 °C steps. The corresponding results are elucidated in Fig. 3 a) and b), respectively.

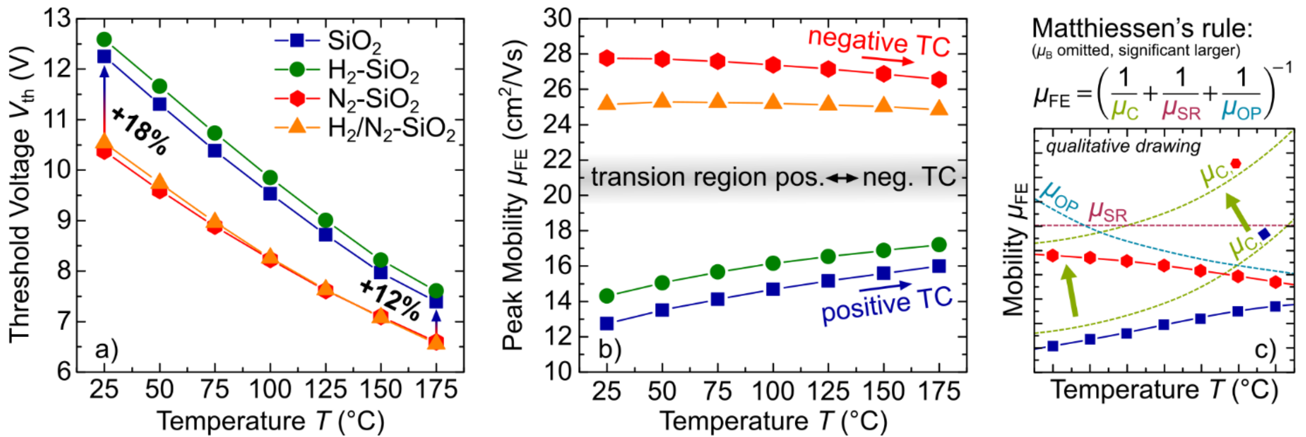

Fig. 3. a) Temperature-dependent V_{th} for one exemplary device per sample. b) The corresponding μ_{FE} values show a different TC, which can be explained by considering the temperature dependence of μ_C, μ_{SR} and μ_{OP}. A qualitative drawing of the scattering contributions is given in c). While μ_{SR} and μ_{OP} are assumed to be comparable between the wafers, especially μ_C strongly depends on the interface preparation and is therefore significantly improved for the N_2-SiO_2 sample.

Regarding V_{th}, a distinct difference between the devices with N_2-containing pretreatment and the SiO_2 sample is observed in Fig. 3 a). Already at room temperature, the N_2-SiO_2 and H_2/N_2-SiO_2 samples show a lower V_{th} value, which can be explained by the steeper I_D-V_G turn-on behavior as a result of a reduced interface trap density around the conduction band edge. The V_{th} gap, however, decreases with increasing temperature. The more stable V_{th} temperature behavior of the N_2-SiO_2 and H_2/N_2-SiO_2 samples is another indication for the improved interface characteristics. The superior interfacial quality additionally shows up in the μ_{FE} trend in Fig. 3 b). Whereas the samples with lower μ_{FE} exhibit a positive temperature coefficient (TC) of μ_{FE}, the behavior clearly reverses for the wafers, which were processed with N_2-containing surface conditioning. A qualitative explanation for this observation is given in Fig. 3 c), where the temperature dependence of the dominant scattering mechanisms, namely Coulomb scattering μ_C, surface roughness scattering μ_{SR} and optical phonon scattering μ_{OP}, is sketched [7]. The bulk mobility μ_C is omitted as it is known to be significantly larger than the other contributions. According to Matthiessen's rule, the lowest value dominates the overall μ_{FE} behavior. In the case of the SiO_2 and H_2-SiO_2 sample, Coulomb scattering, which has a positive TC, limits μ_{FE}. As the interface quality gets remarkably improved by N_2-containing pretreatment, the contribution of μ_C decreases, such that the overall μ_{FE} takes over the negative TC from μ_{OP}. Similar behavior is typically only reported on non-polar surfaces like (11-20) or (0-33-8), where the SiO_2/4H-SiC interface quality is inherently much better [3,8].

During long-term operation of a MOSFET, the stability of important parameters like V_{th} is crucial. To compare the devices' V_{th} stability with differently processed gate oxides, high-temperature gate bias (HTGB) analysis was performed at 175 °C and a gate bias of +20 V and -11 V, respectively. Prior to each V_{th} readout, a preconditioning pulse according to Fig. 4 a) was applied to reduce the contribution of fully reversible trap charging/discharging on the shift in V_{th}. The resulting ΔV_{th} drift signal is shown in Fig. 4 b) and c) for positive BTI (PBTI) and negative BTI (NBTI) stress. For each

sample and stress bias, six devices were analyzed. The respective measurement data is given together with the averaged values per sample and accumulated stress time t.

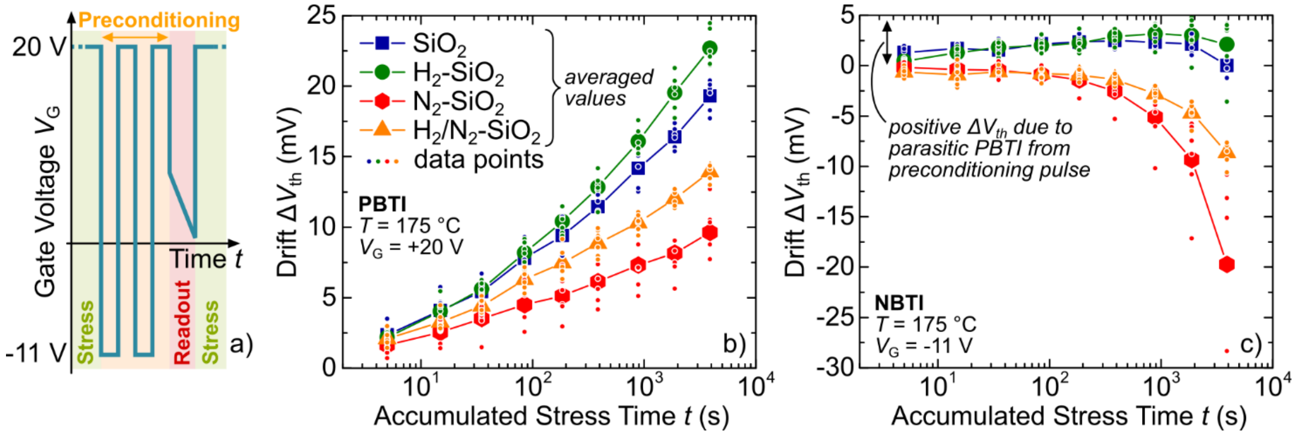

Fig. 4. a) Schematic explanation of the HTGB measurement procedure. Prior to every V_{th} readout, a preconditioning pulse is applied to reduce the ΔV_{th} drift contribution of fully reversible trap charging/discharging. Note that even if the preconditioning pulse plateau phases are short (~ 0.1 s), they can add up a parasitic BTI stress. ΔV_{th} drift signals are shown in b) for PBTI and c) for NBTI stress at 175 °C. The measurement data points of six devices per wafer and stress bias are shown together with the averaged values.

In terms of PBTI in Fig. 4 b), a significantly lower ΔV_{th} drift is observed for the samples with N_2-containing pretreatment. Hence, we speculate, that at least a part of the mobility-limiting interface traps, which are remarkably reduced for the N_2-SiO_2 and H_2/N_2-SiO_2 samples, can also trap electrons (quasi-) permanently. In contrast, however, interface nitridation prior to the gate oxide deposition seems to contribute to enhanced hole trapping during NBTI stress, as shown in Fig. 4 c). Such behavior is similarly observed for heavily nitrided SiO_2/4H-SiC interfaces upon prolonged NO PDA at high temperatures [9]. The SiO_2 as well as the H_2-SiO_2 sample, on the other hand, show negligible ΔV_{th} drift during NBTI stress. Even a small positive ΔV_{th} is observed until $t \approx 10^3$ s, which is assumed to be caused by the parasitic PBTI stress contribution originating from the preconditioning pulse.

Besides the stability of V_{th}, securing a reliable gate oxide operation over lifetime is indispensable. First evaluations in this regard were done by means of TZDB and constant voltage TDDB analysis. The corresponding results are shown in Fig. 5 a)-c). In Fig. 5 a) the gate leakage current normalized to the device area was recorded by increasing V_G with a constant ramp of 0.5 V/s until dielectric breakdown occurred. Per Wafer, ten MOS capacitor devices, built on the n-type doped epi surface, are shown together with a fitted curve, assuming an ideal Fowler-Nordheim (FN) gate leakage behavior. For the calculation of the electric field E, the resulting oxide thicknesses after device processing were considered by performing capacitance-voltage (C-V) measurements. The oxide's dielectric constant was assumed to be $\varepsilon_r = 3.9$ for all samples. Compared to the SiO_2 reference sample, all pretreatment processes contribute to a narrower distribution of the breakdown field strength E_{BD}. The highest E_{BD} around 11 MV/cm is reached for the H_2-SiO_2 sample, while especially the N_2-SiO_2 and H_2/N_2-SiO_2 samples show a distinct shift of the gate leakage curves, attributed to a lower energetic FN tunneling barrier Φ_B. The shown Φ_B values were calculated by considering an effective electron mass of $m^* = 0.42\ m_0$ [10]. Similar lowering of Φ_B was already reported for prolonged interface nitridation via NO PDA [10]. Additionally, at high gate oxide fields, a more pronounced deviation from the ideal FN curve shape is observed for both samples with N_2-containing surface conditioning. While at moderate E-fields in the oxide, the leakage current is predominantly governed by FN tunneling, at higher fields, electrons have sufficient energy to generate holes by anode hole injection from the poly-Si electrode and/or impact ionization in the oxide near the anode. The generated holes drift towards the SiO_2/4H-SiC interface, get trapped and hence, enhance the electric field, which further reduces the FN tunneling barrier for electrons [11]. In logical consequence, electron and hole injection amplify each other, leading to a deviation from the ideal FN current

behavior in the high E-field regime. The gap between the measured and fitted current is more pronounced for the N_2-SiO_2 and H_2/N_2-SiO_2 samples. As the bulk SiO_2 is assumed to have comparable quality for all samples, the current enhancement at higher fields is expected to originate from increased hole trapping near the SiO_2/4H-SiC interface. This conclusion is supported by the observations from NBTI stress analysis, where N_2-containing pretreatment was shown to create interfacial defect states, that capture holes during NBTI as well as high-field TZDB characterization.

To investigate a potential impact of the differences in Φ_B and hole trap density on the TDDB characteristics, MOS capacitor devices from the SiO_2 and N_2-SiO_2 samples were stressed at three different E-fields at a temperature of 140 °C. For each stress field and sample, eight devices were analyzed. Fig. 5 b) shows the respective leakage current evolution over time, while c) illustrates the time-to-breakdown t_{BD} data together with the $t_{63\%}$ values, which we extracted by assuming a Weibull distribution. Interestingly, at least in the investigated E-field range, the resulting t_{BD} values are nearly the same for both samples, even if the initial gate leakage current is significantly higher for the N_2-SiO_2 devices due to lower Φ_B and stronger leakage current enhancement. However, as can be seen by the humps in Fig. 5 b), the chosen E-field values are still in a range, where significant hole injection occurs, which can lead to an overestimation of the gate oxide lifetime. Hence, additional TDDB analysis at lower stress fields would need to be performed to reliably exclude a detrimental effect of N_2 pretreatment on the gate oxide lifetime at typical operation conditions.

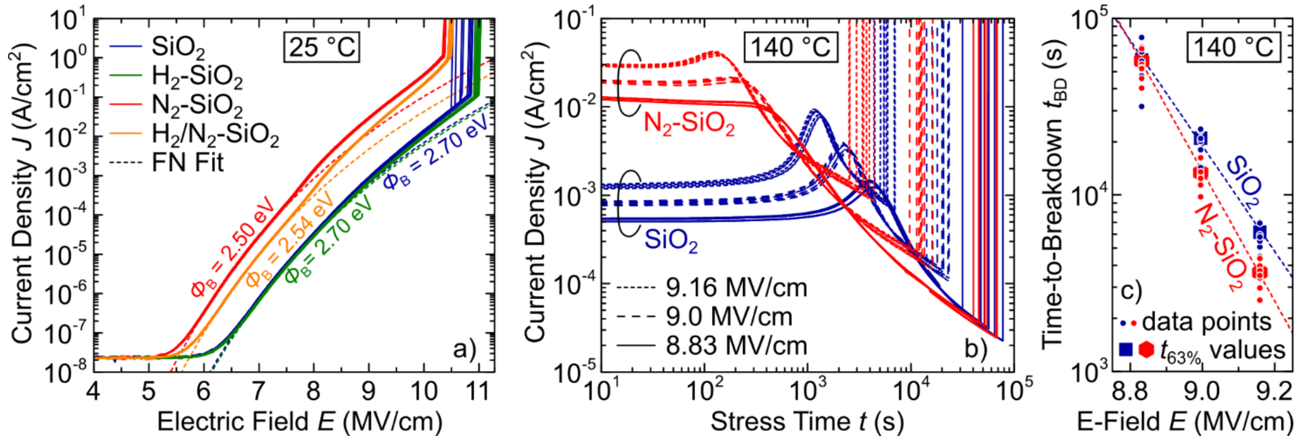

Fig. 5. a) TZDB measurements of ten MOS capacitor devices per sample at room temperature. At moderate E-fields, the measurement curves are reproduced by assuming FN-governed electron tunneling through the SiO_2. The calculated Φ_B values, extracted from the fit, are given. b) Constant voltage TDDB measurements of eight MOS capacitor devices per sample and stress field at 140 °C. The stress time t_{BD}, when dielectric breakdown occurs, is detected and plotted in c) over the E-field. The $t_{63\%}$ values are calculated by assuming a Weibull distribution.

In the attempt to correlate the electrical results with compositional surface characterization, we performed XPS analysis. Additional samples were prepared by annealing epitaxial n-type wafers with the same H_2, N_2 and H_2/N_2 processes as utilized for the electrical MOSFET devices. A bare 4H-SiC epi wafer was added as reference. The XPS core level spectra were acquired ex-situ to the annealing processes. The corresponding results are presented in Fig. 6 a)-f). In Fig. 6 a), the elemental surface composition is evaluated by weighting the integrated signal intensity of the Si2p, C1s, O1s and N1s core level peaks. For all elemental components, three different measurement spots were analyzed. Even if this simple integration method contains some uncertainties regarding the exact compositional values, Fig. 6 a) clearly reveals the formation of O- and N-containing adlayers after all high-temperature surface treatments. While the O-content in the Ref. sample stems from a thin, native oxide layer as well as potential adsorbates from air exposure, the fraction of O and N atoms at the surface remarkably increases for all annealed surfaces by substituting C atoms in the uppermost atomic layers. Regarding the interfacial N coverage, it is often reported, that a higher N amount enhances the μ_{FE} of a MOSFET, while especially the device's reliability has to be taken with caution [9]. Interestingly, in terms of μ_{FE} and PBTI drift, the N_2-SiO_2 sample reveals the best electrical

performance, even if its interfacial N density seems to be reduced, compared to the H_2/N_2-SiO_2 sample. Note that the elemental surface composition could be also affected by further MOS stack and device fabrication and might be slightly different in a fully processed MOSFET device. However, also the N binding configuration might have an impact on the defect passivation. As aforementioned in the introductory section, especially for H_2 [4] and H_2/N_2 [5] treatment of 4H-SiC surfaces, the formation of epitaxial surface reconstructions is reported. The published structures are shown in Fig. 6 e) and f) for H_2 and H_2/N_2, respectively. Both structures consist of an uppermost SiO layer, which is either directly bonded to the 4H-SiC surface or connected via a bridging SiN interlayer. In case of the H_2 treatment, one dangling bond per unit cell is left behind, while the H_2/N_2 treatment ideally passivates the surface.

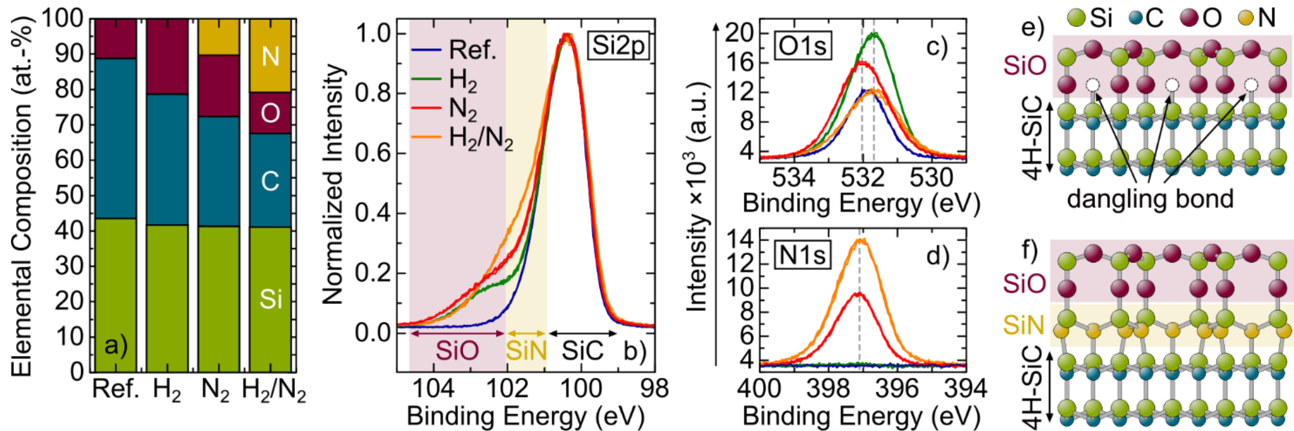

Fig. 6. a) Elemental surface composition for the investigated samples was calculated by weighting the integrated Si2p, C1s, O1s and N1s signal intensities. The corresponding core level spectra are shown in b) for Si2p, c) for O1s and d) for N1s for three measurement spots per sample. Energetic positions of the peaks are indicated by dashed lines. The published surface configurations after e) H_2 [4] and f) H_2/N_2 [5] treatments of 4H-SiC are schematically drawn.

To discuss the potential formation of such surface reconstructions in our experiments, the detailed XPS core level spectra of Si2p, O1s and N1s are given in Fig. 6 b)-d). All spectra were corrected to the theoretical binding energy of the Si2p peak in an ideal 4H-SiC crystal. As compared to the reference sample, Fig. 6 b) shows a pronounced shoulder of different shape for the samples with high-temperature surface conditioning. SiO surface components are typically observed towards higher binding energies, whereas SiN bonds are known to energetically lie between the SiO and SiC component [5]. Those considerations are in line with our measurements, where an increased intensity in the SiN region is observed especially for the N_2 and H_2/N_2 surface treatment. Interestingly, the intensity increase of the Si2p spectra for the H_2 and H_2/N_2 sample towards higher binding energy nearly perfectly overlap. This observation is in agreement to the energetical position of the O1s peak in Fig. 6 c), which is identical for both samples. Hence, it is speculated, that the O atoms are similarly bound in both configurations. The H_2/N_2 sample, however, contains an additional, N-related contribution in Fig. 6 b). Those observations promote the hypothesis, that similar surface adlayers, as shown in Fig. 6 e) and f), are created by the H_2 and H_2/N_2 annealings in our experiment. In contrast, the N_2 treatment seems to form a slightly different adlayer, as compared to the H_2/N_2 treatment. The O1s peak for the N_2 sample is slightly shifted, pointing towards a different Si-O binding configuration. The N1s peak, however, seems to have a similar binding energy.

Summarizing the XPS analysis, our observations are in good agreement with published considerations and our electrical data. The N_2-containg pretreatments were shown to efficiently suppress mobility-limiting traps by passivating the surface. H_2 treatment, in contrast, leaves behind one dangling bond per unit cell, which could be a potential explanation for the less pronounced μ_{FE} improvement after this annealing. However, the reliability of SiO_2 gate dielectrics upon N_2-containing surface conditioning has to be taken with caution, as the resulting surface configurations, even if they slightly differ from each other, were shown to be prone to hole trapping.

Summary

In this work, we investigated the impact of high-temperature H_2, N_2, and H_2/N_2 surface conditioning processes on the electrical performance of lateral SiO_2/4H-SiC MOSFETs and correlated the results with compositional XPS surface analysis. Especially N_2-containing surface treatments were shown to greatly suppress electron trapping states around the conduction band edge, leading to a remarkably improved conductivity of the gate-controlled 4H-SiC/SiO_2 interface. However, similarly to heavily NO-nitrided SiO_2/4H-SiC interfaces, hole traps arise, which could have a detrimental effect on the device's reliability during long-term operation. In contrast to recently published results regarding H_2 treatments, its beneficial effect on μ_{FE} could not be reproduced to the same extent.

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