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Threshold Voltage Control in 4H-SiC MOS Devices by Atomic Layer Deposited Al_2O_3/SiO_2 Interface Dipole Engineering

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Abstract. This study investigates the electric dipole effect at Al_2O_3/SiO_2 interfaces deposited by Atomic Layer Deposition (ALD) on 4H-silicon carbide (SiC) substrates for threshold voltage (V_T) modulation. By incorporating an ultrathin 3nm Al_2O_3 layer onto ALD-deposited 30nm SiO_2, they created an electric dipole that produces a 0.65±0.15V positive shift in threshold voltage after N_2O post-deposition annealing. The dipole-induced voltage shift was validated through both MOS capacitor measurements and lateral MOSFET characterization. Importantly, the threshold voltage enhancement occurred without degradation in field-effect mobility, demonstrating that the dipole effect does not introduce additional scattering centers. This technique offers an effective approach for threshold voltage tuning in alternative semiconductor devices where thermal SiO_2 growth is not feasible, addressing critical challenges in SiC power electronics that require high threshold voltages (>3V) for reliable operation.

Introduction

Electric dipole effects at high-permittivity dielectric (high-k)/SiO_2 interfaces have been reported for various dielectrics, including HfO_2, Al_2O_3, LaO_x, and Y_2O_3 on Silicon as well as Silicon Carbide substrates [1-4]. For example, a dipole-induced voltage shift of up to 0.57 V has been observed for Al_2O_3 on thermally grown SiO_2 on Si [2]. Such dipole effects can lead to either positive or negative flatband or threshold voltage shifts, depending on the properties of the high-k dielectric within the stack. Consequently, dipole engineering provides a means to modulate the threshold voltage of metal–oxide–semiconductor field-effect transistors (MOSFETs) [2]. Traditionally, dipole effects of high-k dielectrics have been investigated on thermally grown SiO_2 on silicon. However, it is particularly interesting to explore these effects on alternative substrates where threshold voltage control remains challenging, such as in silicon carbide (SiC) MOSFETs. In SiC devices, enhancing channel mobility via nitrogen-based post-oxidation annealing often forces a trade-off between mobility and threshold voltage. For reliable power electronics applications, a sufficiently high threshold voltage (>3 V) is typically required. In this work, we report a V_T enhancement method based on the dipole effect of Al_2O_3/SiO_2 stacks deposited by atomic layer deposition (ALD) on 4H-SiC. ALD dielectrics are particularly attractive as gate dielectrics due to their excellent film quality, uniformity, precise thickness control, and low-temperature processing [5]. Here, we demonstrate for the first time the dipole effect in Al_2O_3/SiO_2 stacks deposited entirely by ALD on 4H-SiC.

The origin of the dipole effect is generally attributed to energy band bending at the high-k/SiO_2 interface. This effect can arise from either (i) the electronegativity difference between the cations in the two oxides or (ii) differences in oxygen areal density across the interface [3,4]. As a result, the threshold voltage/flatband voltage (V_T/V_{FB}) shift induced by the dipole effect does not introduce additional interface states or Fermi-level pinning [3,4]. Importantly, unlike charge-induced V_T/V_{FB} shifts, the dipole-induced shift does not generate new scattering centers, and its magnitude is independent of both the SiO_2 and high-k dielectric thicknesses. Thus, the dipole effect can be modeled as an intrinsic band bending at the high-k/SiO_2 interface, which produces a constant flatband shift for a given dielectric stack. Accordingly, the expression for the MOS capacitor flatband voltage must be modified under the assumption that any anomalous V_T/V_{FB} shift is caused by the dipole effect. The general expression for the flatband voltage of a MOS capacitor is given as:

$$V_{FB} = \Phi_{ms} - \frac{q}{\varepsilon_{ox}} \int_0^{EOT} x\rho(x)dx + dipole \tag{1}$$

In this framework, $\boldsymbol{\Phi_{ms}}$ represents the work function difference between the gate and the substrate, $\boldsymbol{\varepsilon_{ox}}$ is the relative permittivity of SiO_2, $\boldsymbol{x}$ denotes the distance from the gate, $\boldsymbol{EOT}$ is the effective oxide thickness of the dielectric stack, and $\boldsymbol{\rho(x)}$ corresponds to the fixed charge density within the dielectric layers or at the interfaces [6]. In the calculation, only fixed charges are considered; these may be located at the SiO_2/SiC interface, within the bulk of the SiO_2, at the high-k/SiO_2 interface, within the bulk of the high-k dielectric, or at the gate/high-k interface. For high-quality SiO_2, the bulk charge density can typically be neglected. Any charge or dipole at the dielectric/gate interface can be accounted for by using an experimentally determined effective gate work function. Therefore, in all subsequent equations, Φ_{ms} should be regarded as the effective work function difference between the gate and the substrate. For a Al_2O_3/SiO_2 dual-layer stack, the flatband voltage equation can be modified as follows:

$$V_{FB} = \Phi_{ms} - \frac{q}{\varepsilon_{ox}} (Q_{SiO2}\, EOT + Q_{Al2O3}\, EOT_{Al2O3} + \rho_{Al2O3} EOT_{Al2O3}^2) + dipole \tag{2}$$

Here, Q_{SiO2} and Q_{Al2O3} represent the fixed charge densities at the SiO_2/SiC interface and the Al_2O_3/SiO_2 interface, respectively. In the derivation, the bulk charge density within the high-k layer is assumed to be uniform. From Equation (2), it follows that, in the absence of any bulk charge, the flatband voltage should exhibit a linear dependence on EOT. Our experimental results indicate that high-k Al_2O_3 contains a negligible amount of bulk charge; therefore, the bulk charge term in Equation (2) can be ignored in the following discussion. To verify the presence of a dipole effect, the charge densities Q_{SiO2} and Q_{Al2O3} must be extracted. When the Al_2O_3 thickness is fixed, Equation (2) can be simplified and written as:

$$V_{FB} = \Phi_{ms} - \frac{q}{\varepsilon_{ox}} (Q_{SiO2}\, EOT + Q_{Al2O3}\, EOT_{Al2O3}) + dipole \tag{3}$$

With Equation (3), the fixed charge density at the ALD SiO_2/SiC interface can be extracted by varying SiO_2 thickness while the Al_2O_3 thickness is fixed.

$$V_{FB} = \Phi_{ms} - \frac{q}{\varepsilon_{ox}} (Q_{SiO2} + Q_{Al2O3}) EOT + \frac{q}{\varepsilon_{ox}} Q_{Al2O3} EOT_{SiO2} + dipole \tag{4}$$

Similarly, using another set of capacitors with varying Al_2O_3 thickness, the fixed charge density at the ALD Al_2O_3/SiO_2 interface can be extracted using Equation (4).

Experiments

MOS capacitors were fabricated on n-type, Si-face (0001) 4H-SiC substrates with a nitrogen doping concentration of $N_D = 6\times10^{15}/cm^3$. Following surface cleaning in solvents and diluted hydrofluoric (HF) acid, the samples were immediately transferred to an ALD system for SiO_2 deposition at 150 °C. Variation in SiO_2 thickness across the MOS capacitors was achieved by wet etching in diluted HF. For the dual-layer capacitors, an ALD Al_2O_3 layer was subsequently deposited at 200 °C after the SiO_2 etching step. Post-deposition annealing (PDA) was carried out in a rapid thermal anneal (RTA) system at 900 °C in pure N_2O ambient. The gate electrode was formed by RF sputtering of tantalum nitride (TaN) capped with tungsten (W). A post-metallization anneal (PMA) in N_2 ambient was then performed to mitigate sputter-induced damage. The capacitance–voltage (C–V) characteristics were measured using an HP 4284A precision LCR meter. Flatband voltage and effective oxide thickness (EOT) were extracted from the 1 MHz C–V curves with the CVC program, using 4H-SiC material parameters [7]. Lateral MOSFETs were fabricated on Al-doped ($N_A = 5\times10^{15}/cm^3$ Si-face (0001) 4H-SiC substrates. Source and drain regions were formed by phosphorus implantation followed by activation annealing. After field oxide deposition and patterning, the samples underwent the same surface cleaning, ALD dielectric deposition, PDA, and TaN/W gate electrode deposition and patterning steps used for the capacitors. Contact holes were etched in HF solution prior to the N_2O PDA. The source/drain ohmic contacts were formed by nickel silicide after the gate stack fabrication. Finally, MOSFET characteristics were measured using a Keithley 4200 semiconductor parameter analyzer.

Results and Discussion

The C–V characteristics of MOS with ALD SiO_2 and Al_2O_3/SiO_2 dielectrics are shown in Fig. 1 (a). The C-V curves measured at different frequencies exhibit minimal frequency dispersion. The flatband voltage and effective oxide thickness of the MOS capacitors were extracted to evaluate the dependence of V_{FB} on oxide thickness. The effective work function of TaN gate electrode on Al_2O_3 and SiO_2 dielectrics was individually extracted from measured capacitor C–V data of MOS capacitors with single-layer Al_2O_3 and SiO_2. The effective work function of TaN on ALD SiO_2 and ALD Al_2O_3 is 4.47±0.01 eV and 4.56±0.04 eV, respectively. As shown in Fig. 1 (b), V_{FB} values of capacitors with only ALD SiO_2 and those with dual-layer stacks both show a linear dependence on oxide thickness, indicating a negligible amount of bulk fixed charge in the oxide. The linear fitting line of the dual-layer devices shows a significantly higher y-intercept than that of the ALD SiO_2 samples, suggesting the existence of a dipole. The positive slopes of the linear fits indicate negative effective fixed charges, consistent with prior observations in ALD SiO_2 dielectrics [8]. Table 1 summarizes the extracted charge density and interface state density. Based on calculations, the dipole-induced V_{FB} shift is estimated to be 0.65±0.15 V. The addition of Al_2O_3 reduces the gate leakage due to the incorporation of a high-k layer in the oxide stack.

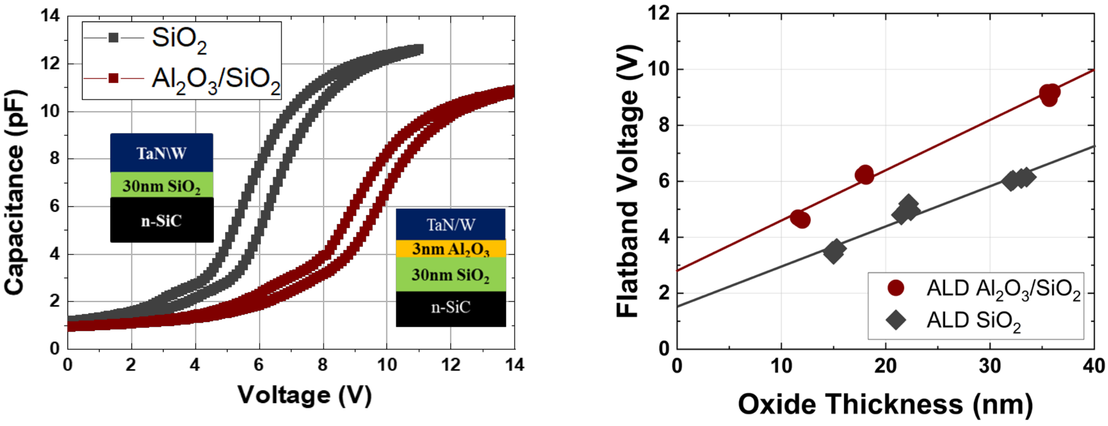

Fig. 1. (a) C-V characteristics of MOS Capacitors and (b) Flatband voltage vs. oxide thickness of MOS Capacitors with 30nm ALD SiO_2 and ALD Al_2O_3/SiO_2 after 900°C N_2O PDA. Both sets of samples contain ALD SiO_2 with various thicknesses.

Figure 2 (a) shows the average flatband voltage for ALD SiO_2 and Al_2O_3/SiO_2 dielectrics after post-deposition annealing (PDA) at 900°C and 1000°C. The Al_2O_3/SiO_2 stack maintains a higher flatband voltage compared to SiO_2 indicating the persistence of the interface dipole between Al_2O_3 and SiO_2. Figure 2 (b) presents the gate leakage characteristics, where the incorporation of an Al_2O_3 layer effectively suppresses gate leakage in the low- and moderate-field regions. These results confirm that the Al_2O_3/SiO_2 dielectric stack provides superior electrical performance, offering both enhanced flatband voltage stability and reduced leakage current relative to a single SiO_2 dielectric.

Table I. Extracted parameters from MOS capacitor with ALD SiO_2 and Al_2O_3/SiO_2 after 900 °C PDA.

Dielectric	Parameters	
	Charge Density (cm^{-2})	D_{IT} at E_c-E_T =0.2eV
SiO_2	$-3.19\times10^{12}\pm4.3\times10^{11}$	2.0×10^{12}
Al_2O_3/SiO_2	$-3.71\times10^{12}\pm1.5\times10^{11}$	2.0×10^{12}

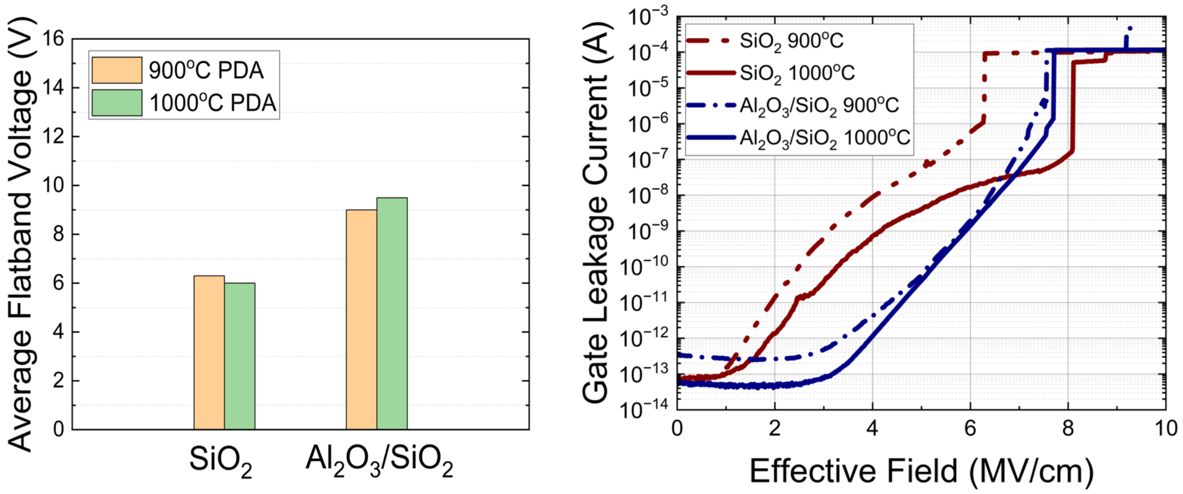

Fig. 2. (a) Average flatband voltage after two different PDA temperatures and (b) Gate leakage characteristics of MOS capacitors with single SiO_2 and dual Al_2O_3/SiO_2 dielectrics.

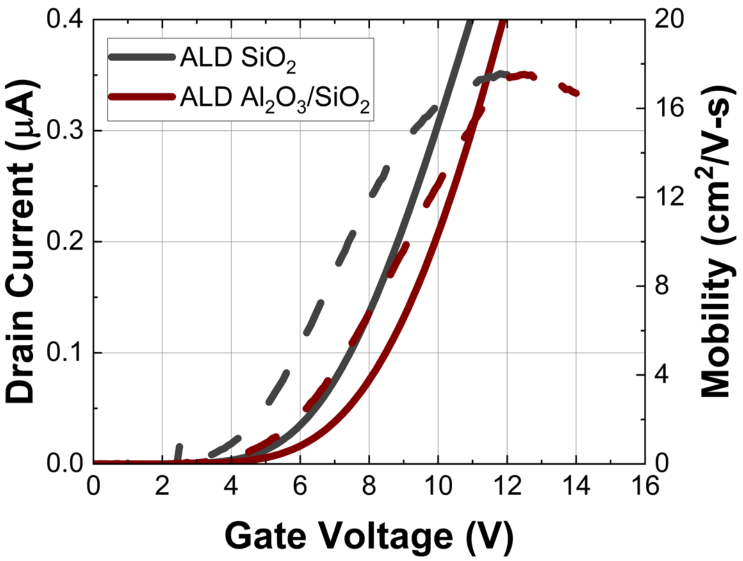

Fig. 3. I_{DS}-V_{GS} curves and mobility of MOSFETs with ALD SiO_2 and Al_2O_3/SiO_2.

Lateral MOSFETs were fabricated to validate the MOS capacitor results. As shown in Fig. 3, the lateral MOSFET with an ALD Al_2O_3/SiO_2 dual-layer gate dielectric exhibits a threshold voltage that is 1.24 V higher than that of the device without Al_2O_3, accompanied by an increase of 1.5 nm in effective oxide thickness (EOT) due to the additional Al_2O_3 layer. Considering the effect of the negative fixed charge, the increase in EOT from the Al_2O_3 layer accounts for approximately 0.6 V of the observed V_T shift. The remaining increase in V_T is therefore attributed to the dipole effect.

Importantly, no degradation in field-effect mobility or subthreshold swing was observed. These results demonstrate that the ALD Al_2O_3/SiO_2 dual-layer stack is an effective approach to increase the threshold voltage of SiO_2-based devices without compromising device performance. Furthermore, the findings confirm that the dipole does not introduce additional scattering centers at the SiC/dielectric interface compared to devices with only ALD SiO_2. In addition, the ALD-deposited dual-layer stack can be extended to other alternative semiconductor substrates to induce a positive threshold voltage shift.

Summary

We have demonstrated the existence of an electric dipole at the Al_2O_3/SiO_2 dual-layer stack deposited by ALD on 4H-SiC substrates. After N_2O post-deposition annealing, the dual-layer stack exhibits a dipole-induced voltage of 0.65 ±0.15 V. Lateral MOSFET results further confirm that the incorporation of Al_2O_3 induces a positive threshold voltage shift of 1.24V, accompanied by suppressed gate leakage and without degradation in mobility or subthreshold swing. These results highlight that Al_2O_3/SiO_2 stacks not only enable threshold voltage tuning but also improve dielectric properties. This approach provides an effective pathway to achieve a positive threshold voltage in 4H-SiC MOSFETs and can be extended to other wide bandgap semiconductor devices where thermal oxidation of SiO_2 is not feasible.

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