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Feasibility Study of SiC Wafer Reutilization Process through Laser Splitting and Bonding Techniques

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Abstract. We propose a novel SiC wafer recycling process that employs the laser splitting and wafer bonding techniques. The process allows us to attain the recycled SiC wafers suitable for conventional device processes, leading to the reduction of SiC device costs and environmental burdens. Preliminary evaluations were conducted on the key technologies of the process: surface activated bonding and laser splitting for SiC wafers. The bonding interface was confirmed to withstand the stresses encountered during device manufacturing thanks to the recrystallization of the interface layer. The electrical characteristics of MOSFETs thinned using laser splitting showed no significant difference compared to those thinned by conventional grinding. These results demonstrate that the proposed process is a feasible technique that offers a cost-effective and eco-friendly solution for SiC power device production.

Introduction

The high cost of SiC wafers is one of the major issues in further promoting the adoption of SiC devices. SiC wafers are frequently thinned through grinding to reduce on-resistance and mitigate thermal stress caused by differences in thermal expansion coefficients within power modules. Reducing the amount of discarded SiC material and, ideally, reusing it in device fabrication is highly desirable. This approach not only helps reduce costs but also minimizes environmental impact. Several potential technologies for reducing wafer costs have been reported [1, 2], but there are still challenges to tackle from both technical and cost perspectives.

We propose a novel SiC wafer reutilization process that employs laser splitting and bonding techniques. The laser splitting technology is progressing markedly today and well-suited for this process. Preliminary experiments have been conducted on wafer bonding and laser splitting, which are key technologies for the proposed wafer reutilization process. In this paper we present the findings and examine the feasibility of the proposed approach.

Proposal of Novel SiC Wafer Reutilization Process

A novel SiC wafer reutilization process for device fabrication is proposed. Fig. 1 illustrates the rough sequence of the SiC wafer reutilization process. In this process, a wafer is split into two wafers at a certain thickness after fabricating device structures on its top surface. The wafer with the device structures undergoes usually used wafer processing. Meanwhile, the surface of the split wafer without device structures is polished, cleaned, and then bonded with another split wafer. This results in a recycled wafer with a thickness suitable for device fabrication. After forming device structures on the

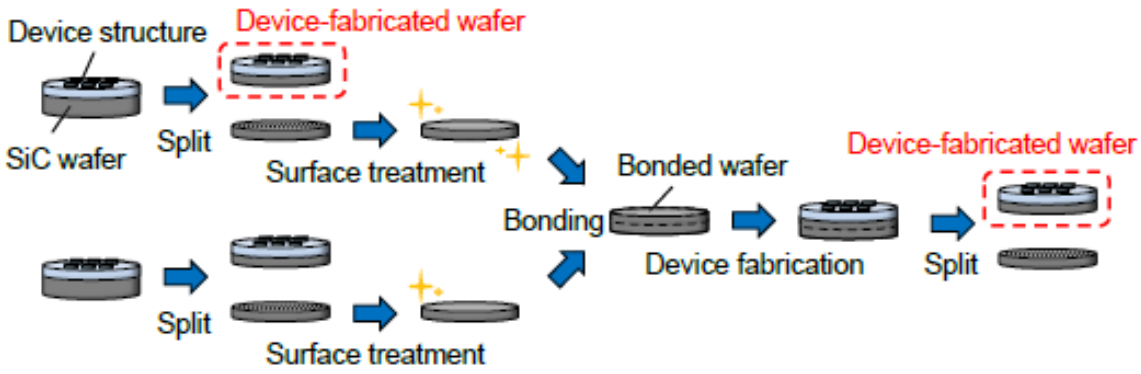

Fig. 1. Schematic of Novel SiC Wafer Reutilization Process using laser splitting and bonding techniques.

bonded wafer, it is split again into two wafers: one with devices and one without devices. The split wafer without devices then repeats the above-mentioned process, and thereby the recycled wafer is fabricated again.

The proposed process is expected to attain several advantages. Firstly, it leads to reduction in costs and material loss, which is crucial for SiC device manufacturing. Specifically, this process increases the chip yield (in this case referring to the number of chips) per initial wafer, thereby drastically reducing the chip cost. Secondly, it eliminates the need for externally procured heterogeneous support wafers, such as poly-SiC wafers, and the recycled wafers are formed entirely from 4H-SiC material. This not only reduces costs but also enhances compatibility with conventional device production processes. Furthermore, it is possible for the sprit wafer with devices to exclude the junction interface, ensuring that there are no negative effects on device characteristics resulting from including the bonding interface such as increase in resistance.

The wafer bonding technique and the laser splitting technique are key technologies in this wafer reutilization process. To verify the feasibility of this wafer reutilization process, preliminary experiments were conducted on these two techniques.

Investigation of Wafer Bonding Technique

We investigated the bonding technique for split SiC wafers and the feasibility to split the bonded wafer at a designed thickness. The SiC wafer bonding method is schematically shown in Fig. 2. Two 6-inch 4° off 4H-SiC wafers were thinned to 150 µm by grinding, and their surfaces for bonding (both C- and Si-face) were flattened using a CMP method. Subsequently, the two wafers were bonded at room temperature using the surface activated bonding method [3].

The bonded wafer fabricated using above method were implanted with Al ions at a doping concentration of 2 x 10^{15} cm^{-2} across the entire wafer surface and subsequently annealed at 1750℃ to electrically activate the Al. Additionally, another bonded wafer was divided again by the laser

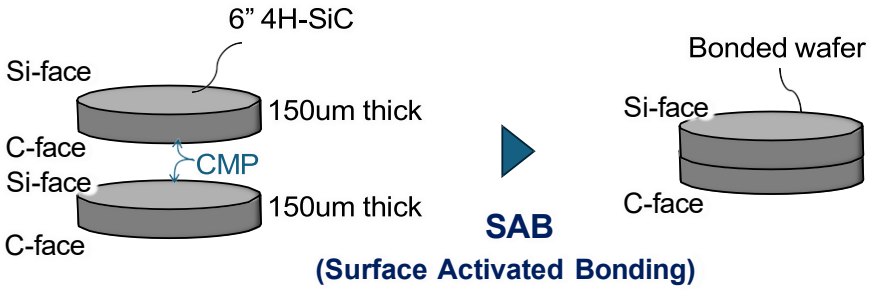

Fig. 2. Fabrication method of bonded wafers.

splitting technique after epitaxial growth. The evaluation was conducted through optical microscope observation, warpage measurement, and cross-sectional TEM analysis.

Fig. 3(a) shows appearance of the wafer immediately after wafer bonding. No significant differences in appearance between the bonded and normal wafers are noted except for a few small voids (1-5 mm in diameter) caused by particles at the bonding interface. Photos of the whole wafers after the Al implantation and the thermal annealing are shown in Fig. 3(b) and (c), respectively. Change of color due to Al implantation is observed in Fig. 3(b), but the color returns to the original color of as-bonded wafers after the thermal annealing. No cracks, chips or peelings originating from voids or wafer edges are observed after the bonding and subsequent Al implantation and the annealing processes. Despite the strong stress imposed on the wafer by high dose ion implantation and high temperature annealing, the bonded wafer shows no fatal changes.

The bonding interfaces immediately after bonding and after the annealing were observed in detail using the cross-sectional TEM. Corresponding TEM images are shown in Fig. 4(a) and (b), respectively. In the TEM image of the as-bonded wafer (Fig. 4(a)), an interface layer is clearly observed between the upper and lower wafers, and it is confirmed from the magnified image that this layer exhibits an amorphous structure. In contrast, at the bonding interface after the thermal annealing, the distinct amorphous layer disappears, indicating that solid phase reaction has occurred and yielded polycrystals at the interface during the high temperature annealing process. Since the polycrystals are strongly bonded to each other, the bonded wafers do not break or peel and are expected to withstand harsh wafer processes.

We investigated warpage of the bonded wafer. Fig. 5 shows the relationship between the SORI and the wafer thickness for the bonded and standard wafers. SORI of both types of wafers decreases with increasing the wafer thickness. It is found that they are on the curve calculated using Stoney's equation. Additionally, it has been confirmed that the SORI does not change significantly even after implantation and annealing. This indicates that we need no special care to handle the bonded wafers.

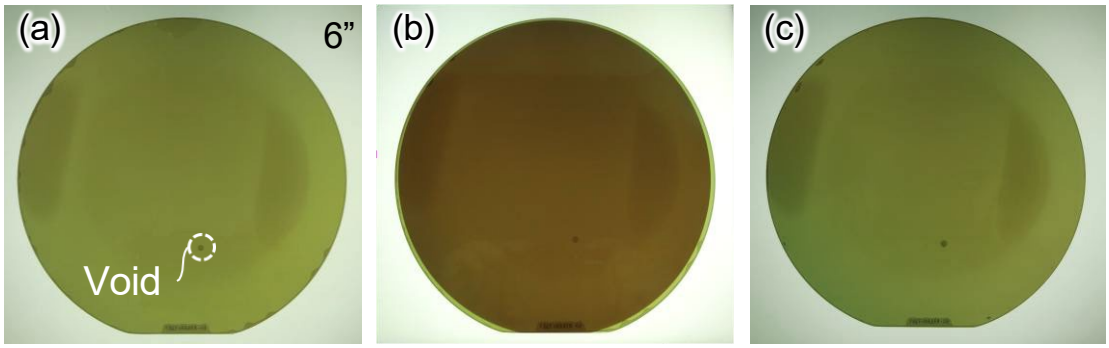

Fig. 3. Appearances of the wafer (a) after bonding, (b) Al implantation at a doping concentration of 2×10^{15} cm^{-2}, and (c) thermal annealing at 1750°C.

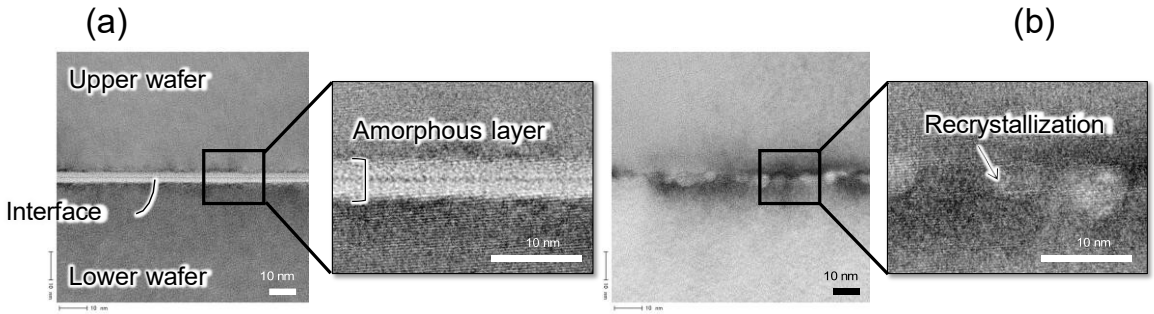

Fig. 4. Cross-sectional TEM images of the bonding interface (a) immediately after bonding, and (b) after thermal annealing.

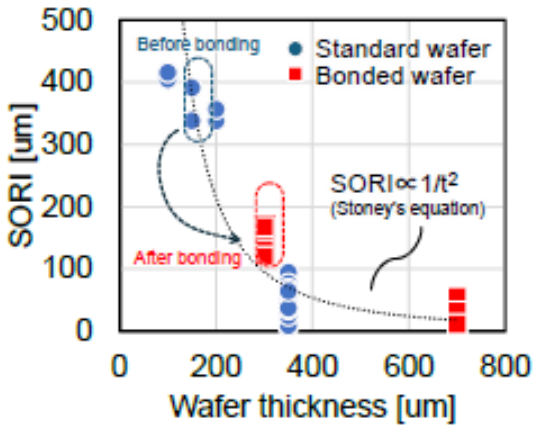

Fig. 5. Wafer thickness dependence of SORI for standard wafers and bonded wafers.

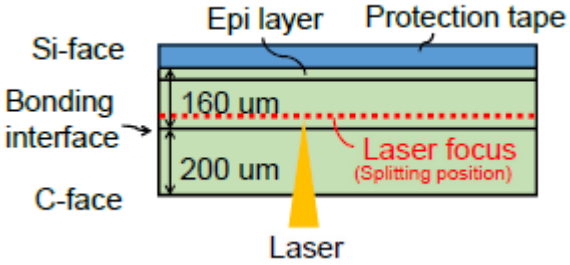

Fig. 6. Cross-sectional structure and splitting position of bonded wafers.

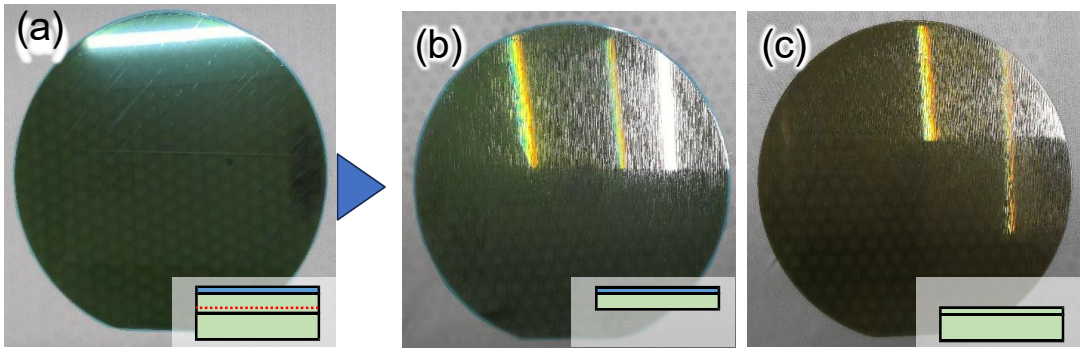

Fig. 7. Images of the bonded wafer (a) before laser splitting, and (b) the top side without bonding interface and (c) the bottom side with bonding interface after laser splitting.

Next, feasibility of re-splitting the bonded wafer using laser splitting technique [4, 5] was investigated. Cross-sectional structure and splitting position of the bonded wafer is illustrated in Fig.
6. After SiC epitaxial growth on top side of the bonded wafer, a protective tape was put onto it. The splitting was set at the position between the bonding interface and the epitaxial layer. Since the laser beam scan is performed from the backside of the wafer, the laser light focuses beyond the bonding interface.

Fig. 7 shows surface images of bonded wafer before laser splitting (a) and after laser splitting (b, c). The bonding interface exists in the bottom side wafer. No noticeable cracks or chips are observed in the wafer after splitting, indicating that the bonding interface does not negatively affect the laser splitting. This result shows that the bonded wafer can be re-split with the designed thickness irrespective of the position of bonding interface.

Influence of Laser Splitting Process on MOSFETs

The influences of laser splitting on characteristics of SiC power devices has been investigated to verify the feasibility of applying the laser splitting technique to device fabrication. SiC MOSFETs were fabricated using the laser splitting technique for the thinning process.

The fabrication procedure for the SiC MOSFETs is illustrated in Fig. 8. An epitaxial layer was grown on a standard 6-inch 4H-SiC substrate with a 4° off-cut angle, and 1200V SiC MOSFET structures were subsequently fabricated on this epitaxial layer. This wafer was then divided at a depth of 180 μm from the top surface by precisely controlling the laser focus during the laser splitting

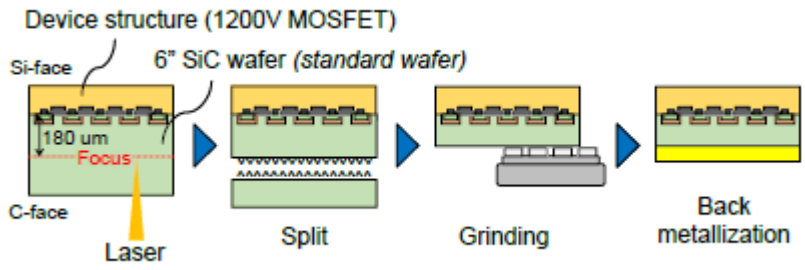

Fig. 8. Fabrication procedure.

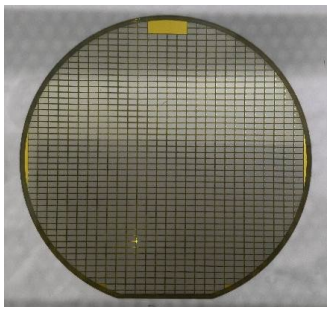

Fig. 9. Image of the wafer with device structures after laser splitting.

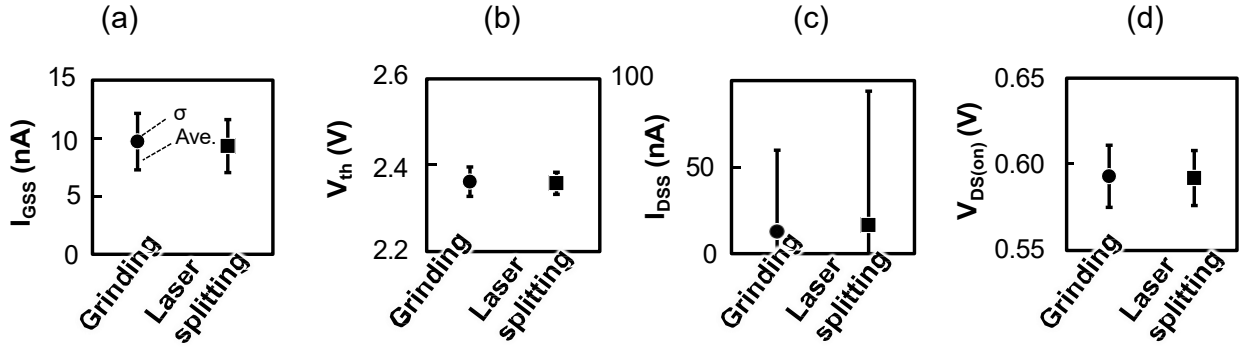

Fig. 10. Comparison of main electrical characteristics ((a) I_{GSS}, (b) V_{th}, (c) I_{DSS}, and (d) $V_{DS(ON)}$) of MOSFETs fabricated using laser splitting and conventional grinding process.

process. The rough splitting surfaces were subsequently ground to achieve a final thickness of 100 μm. Finally, a backside metal electrode was formed, and the wafer was diced into chips. Image of the wafers observed from the top side after laser splitting are shown in Fig. 9. No damage is visible in the image.

The main electrical characteristics of MOSFETs, including gate leakage current (I_{GSS}), threshold voltage (V_{th}), drain leakage current (I_{DSS}) and on-voltage ($V_{DS(ON)}$), were measured.

Fig. 10 shows the characteristics of the MOSFETs. In the figure, the values of the MOSFETs thinned by the laser splitting process are compared to those of MOSFETs thinned by the conventional grinding process. The I_{GSS} remains very low for the MOSFETs with the laser process (as shown in Fig. 10(a)), and the V_{th} shows no change compared to MOSFETs with conventional thinning process (as shown in Fig. 10(b)), meaning that the gate oxide film was not subjected to significant damage from the laser irradiation. No significant changes in mean values and deviations were observed for the I_{DSS} and the $V_{DS(ON)}$ (as shown in Fig. 10(c) and (d)), indicating that the laser splitting process does not damage the drift layer or electrodes. So far, we have obtained no results that show the laser process negatively impacts the MOSFET electrical characteristics.

Summary

We proposed a novel SiC wafer reutilization process that integrates laser splitting and wafer bonding techniques. This approach aims to drastically reduce costs and material loss in SiC power device manufacturing by enabling the recycling of the wafers.

Our preliminary investigations have demonstrated the technical feasibility of this proposed process. Through comprehensive experiments on SiC wafer bonding, we confirmed that strong and stable bonds can be achieved using the SAB technique. The bonded wafers withstand processes such as high-temperature annealing and high-dose ion implantation without significant changes or delamination. Detailed cross-sectional TEM analysis revealed the formation of robust polycrystalline bonds at the interface due to solid phase reactions during thermal annealing, confirming their suitability for subsequent device processing.

The influence of the laser splitting process on device characteristics was evaluated using SiC MOSFETs. The electrical characteristics of the devices thinned by laser splitting showed no significant degradation compared to those thinned by conventional grinding. This confirms that the laser splitting process does not induce damage to the gate oxide film, drift layer, or electrodes.

These results demonstrate the technical feasibility of the proposed approach, which offers a cost-effective and eco-friendly solution for SiC power device production. It will be necessary to conduct evaluations of thermal stress accumulation after multiple cycles of splitting and bonding, as well as reliability assessments of the MOSFET after laser splitting in the future.

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