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CMOS-Compatible Pore Nucleation on 4H-SiC Si-Face via Reactive Ion Etching for Homogeneous Electrochemical Etching

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Abstract. Electrochemical etching (ECE) of silicon carbide is a powerful route to porous 4H-SiC. Yet, reliable pore initiation on the Si-face typically requires additional sophisticated pre-conditioning (e.g. masked KOH etching, metal-assisted photochemical etching (MAPCE), focused ion beam (FIB) milling), limiting industrial adoption. We demonstrate a simple, CMOS-compatible pre-conditioning based on short reactive-ion-etching (RIE) steps (10–30 s, SF_6/O_2) that reproducibly nucleate pores on the Si-face of highly doped 4H-SiC (resistivity < 0.02 Ω·cm) and enable homogeneous ECE in HF/ethanol without UV illumination. Surface roughness increases modestly with RIE time (R_a ≈ 1.3 nm to 4.0 nm), while subsequent ECE does not significantly degrade topography. SEM cross-sections reveal continuous porous layers; image-based quantification shows enhanced vertical pore alignment with longer RIE duration. A stepwise voltage program (11.5 V → 8.5 V → 11.5 V) yields stable current transients during etching. Eliminating noble metals and lithography reduces contamination risk. It improves process compatibility with front-end manufacturing while remaining synergistic with our previously established ECE process flows and high-temperature reorganisation of thin, porous SiC layers.

Introduction

Porous semiconductors are essential for several processes in today's semiconductor industry, due to their unique properties as well as cost aspects. In silicon, electrochemical porosification followed by bonding, annealing, or selective dissolution is used at scale to implement ELTRAN® layer transfer for SOI [1] and to form sacrificial or architected layers in MEMS [2]. Extending the same strategy to silicon carbide would offer clear advantages for device operation at high temperature, or chemically aggressive media. Even more, the integration into process flows for power electronics would open up new possibilities [3], [4]. However, progress has been limited because the electrochemistry of SiC compared to silicon is more demanding, and the etching kinetics depend strongly on the exposed crystal face. Early work established that n-type 4H-SiC forms porous layers by photoelectrochemical etching (PECE) in HF electrolytes, with the Si- and C-terminated faces exhibiting substantially different oxidation as well as etching behaviours (e.g., C-face typically faster and yielding more columnar morphologies) [5], [6], [7].
To enable application-relevant morphologies and stacking, our group previously combined metal-assisted photochemical etching (MAPCE) with PECE to tailor porosity depth profiles and avoid cap or skin layers [8]. We used this approach to demonstrate that single-crystalline, porous 4H-SiC foils can be released from the mother substrate and later be compactified by high-temperature annealing while preserving crystallinity. This is an analogue to silicon "reorganisation" used in ELTRAN® and related processes [9]. Notably, we scaled PECE foil release to 2-inch diameter areas. We verified single crystallinity by TEM after He-annealing up to 1600 °C, highlighting a viable path toward

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substrate re-use and advanced SiC substrate concepts [10]. In parallel, we demonstrated controlled spalling of SiC using a Ni stressor layer anchored in MAPCE-generated surface porosity. This is another wafer-economical route that benefits from predictable, uniform near-surface microstructures [11]. But, all These developments point to porous-SiC-enabled integration strategies analogous to mature silicon technologies such as ELTRAN®, which rely on porous layers for bonding and controlled splitting. However, a persistent bottleneck in SiC is reliable, lithography-free pore nucleation on the Si-face in a manner compatible with CMOS contamination control. Common pre-conditioners include patterned KOH pits (silicon) [12], noble-metal seeding (MAPCE) [8], or FIB nanocavities [13]; in SiC, these either add topography, introduce metals, or lack throughput.

In this work, a reactive-ion-etching (RIE) pre-treatment is explored as a noble-metal-free approach for preparing the Si-face of 4H-SiC prior to electrochemical etching. Short SF_6/O_2 RIE steps are applied before ECE, resulting in a controlled modification of the near-surface region. Fluorine-based plasmas are known to induce subtle nanoscale roughness, micro-masking effects, and chemical surface modifications, which can influence surface energy, wettability, and local electric fields [14], [15]. The following sections investigate how such an RIE pre-conditioning affects pore initiation behaviour during subsequent electrochemical etching, including its influence on current transients, pore morphology, and pore orientation. The study focuses on evaluating the suitability of this approach as a CMOS-compatible pre-treatment for Si-face porosification.

Finally, we want to place this approach in the broader context of porous-SiC manufacturing. Beyond layer transfer and substrate engineering, recent works have revisited ECE of SiC for optical mirrors [16] and MEMS membranes [17], while other groups explore architected 3D microstructures by combined dry/wet routes. These directions reinforce the need for pre-conditioning methods that are selective, scalable, and fab-compatible-requirements our RIE-assisted ECE approach directly addresses [18], [19].

Experimental Details

Samples (2.5×2.5 cm²) were diced from 4-inch, N-doped 4H-SiC wafers (4° off-axis, Si-face roughness < 0.1 nm, resistivity 0.02 Ω·cm) from SiCrystal. After an HF dip, they received reactive-ion-etching (RIE) in a parallel-plate plasma (STS) at 300 W with 25 sccm O_2 and 5 sccm SF_6 for 10, 20, or 30 s. ECE was performed in a tabletop AMMT cell (see Fig. 1) with the SiC piece acting as the separator between anodic and cathodic compartments; pore formation occurred at the side facing the cathode, in an aqueous solution of HF and ethanol (5.52 mol L^{-1} HF, 1.7 mol L^{-1} ethanol). No UV illumination was required due to the high electrical conductivity of the samples. A step-programmed bias was applied (first minute 11.5 V, then 8.5 V for 2 min, followed by 11.5 V for 1 min) to manage nucleation and growth transients (see the current–time trace analogous to Fig. 2). More information about the ECE mechanism and setup is presented in Ref. [8]. Surface roughness was measured with a stylus profilometry (Bruker Dektak) and AFM (Bruker Dimension Edge). SEM (Hitachi SU8030) was used for plan-view and cross-section imaging. A custom Python/OpenCV workflow quantified pore alignment: pore cross-sections were segmented and clustered into orientation kernels, fitted by ellipses to extract principal axes, and visualised as polar histograms (see Fig. 5).

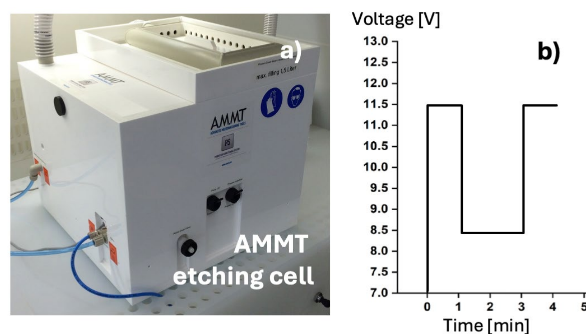

Fig. 1. a) Optical photograph of the tabletop etching cell from AMMT, and b) illustration of the applied voltage profile during electrochemical etching.

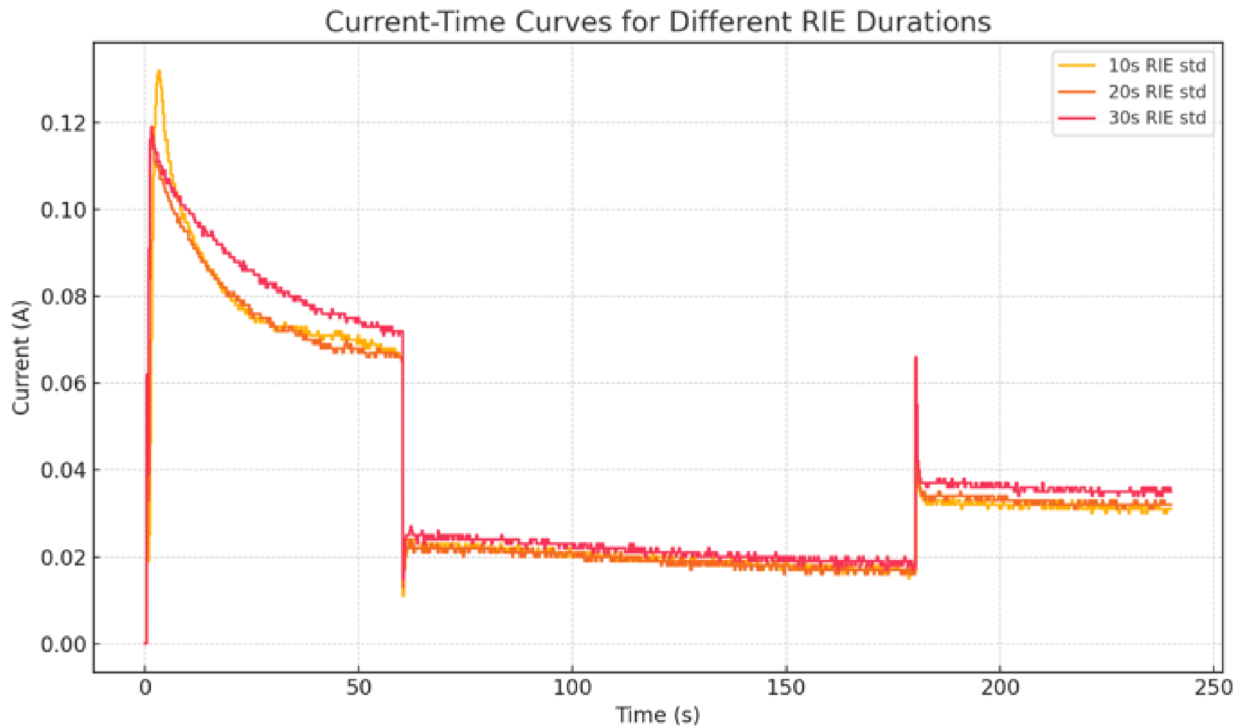

Fig. 2. Typical current response during electrochemical etching of RIE pre-treated samples. The applied voltage in the first minute was 11.5 V, followed by 8.5 V for two minutes and again 11.5 V for one minute.

Results

When analysing samples exposed to 10, 20, and 30 s RIE steps, the arithmetic mean roughness increased from $R_a \approx 1.3$ nm (10 s) and 1.4 nm (20 s) to 4.0 nm (30 s) as listed in Table 1. After ECE, R_a values were 1.3, 1.5, and 5.2 nm, respectively. The corresponding R_q values followed the same trend, thus the ECE step did not measurably degrade surface quality beyond the RIE-imposed baseline. Fig. 3 illustrates the surface after 20 seconds of RIE treatment prior to ECE. The current–time response exhibited characteristic plateaus/decays at each voltage level (11.5 V → 8.5 V → 11.5 V), indicating controlled transitions from nucleation-dominated to growth-dominated regimes (Fig. 2). The final 11.5 V step restored a stable current consistent with sustained pore propagation.

Table 1. Roughness results gained from surface profilometry.

Surface roughness [nm]	Before ECE		After ECE	
	R_a	R_q	R_a	R_q
10 s RIE	1.3	1.9	1.3	1.6
20 s RIE	1.4	1.7	1.5	1.8
30 s RIE	4.0	6.2	5.2	5.9

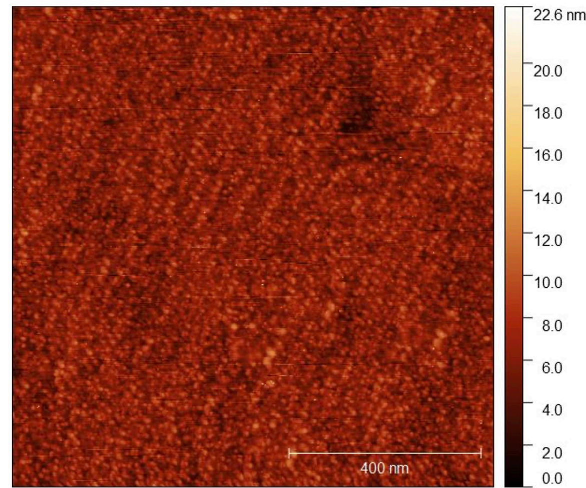

Fig. 3. Results from AFM analysis of a sample with 20 s RIE treatment before ECE.

SEM plan-views before and after ECE (Fig. 4a-f) show the RIE-textured Si-face surface. The corresponding cross-sectional views are shown in Fig. 4 g-i, revealing continuous porosity across the processed depth. Residual flakes seen in plan-view originate from dicing tape and are not morphological features of the RIE process nor from the porosified SiC using ECE. Image analysis of cross-sectional SEMs showed a progressive narrowing of the angular distribution of pore axes with increasing RIE time (polar histograms in Fig. 5), i.e., longer RIE pretreatments yielded a higher fraction of pores aligned closer to the surface normal.

Discussion

It is known from literature, that the Si-face is less reactive than the C-face. This demonstrated in multiple studies which show faster oxidation and higher etch rates under comparable conditions, which correlate with the prevalence of columnar pores on the C-face in PECE [5], [7]. Recent mechanistic analyses of SiC oxidation further indicate that the C-face develops thicker oxides within a given time frame and higher reaction currents than the Si-face, consistent with kinetically easier formation and/or removal of carbon-containing by-products on the C-face [20].

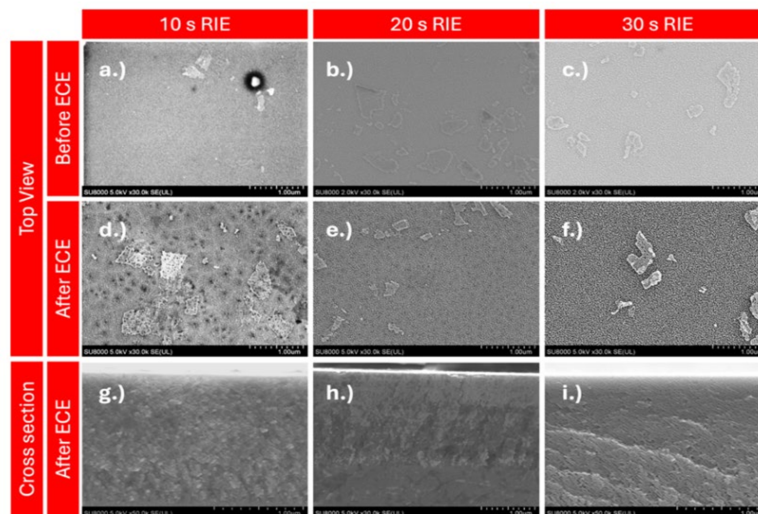

Fig. 4. SEM micrographs of the sample surface and cross-sections before and after RIE pre-treatment with different etching durations: 10 s (left column), 20 s (middle column), and 30 s (right column). The top row (a–c) shows the surface morphology before electrochemical etching (ECE), the middle row (d–f) shows the surface after ECE, and the bottom row (g–i) presents the cross-sectional views after ECE. The flake-like structures shown in the top-view micrographs are residuals from the dicing tape.

Our data suggest that brief SF_6/O_2 RIE steps compensate this kinetic disadvantage of the Si-face by (i) introducing sub-nanometric roughness and micro-defect sites that act as local field concentrators and oxidation nuclei, (ii) modifying surface chemistry (fluorination/oxygenation) to lower the barrier for initial SiC oxidation in HF electrolytes, and (iii) improving electrolyte wetting and transport into nascent cavities, which is enhanced by ethanol in the electrolyte [14], [15], [21]. The outcome is a reproducible pore nucleation density that enables homogeneous ECE at moderate voltages, without UV. The observed current transients under the 11.5 → 8.5 → 11.5 V program are consistent with an initial field-assisted nucleation burst followed by growth stabilisation and a re-acceleration step to sustain front propagation. This control principle mirrors our prior MAPCE/PECE approach, where time-programmed potentials were used to engineer porosity gradients and avoid cap layer formation [8]. In highly doped n-type SiC, band-bending at the semiconductor/electrolyte interface already confines holes at the surface under forward bias, enabling UV-free ECE when contact/transport conditions are favourable. The sharpening of the pore-axis angular distribution with longer RIE (Fig. 5) implies a transition from lateral/branched to preferentially vertical growth as the density and uniformity of initiation sites increase. We ascribe this to a combination of (i) more uniform initial pit geometry and (ii) reduction of local lateral field inhomogeneities once a dense array of nearly equally spaced pits forms, leading to self-screening of lateral growth paths. This interpretation is consistent with prior observations that controlled initiation influences pore directionality and that face-dependent kinetics reinforce vertical growth once nucleation is spatially homogeneous [8].

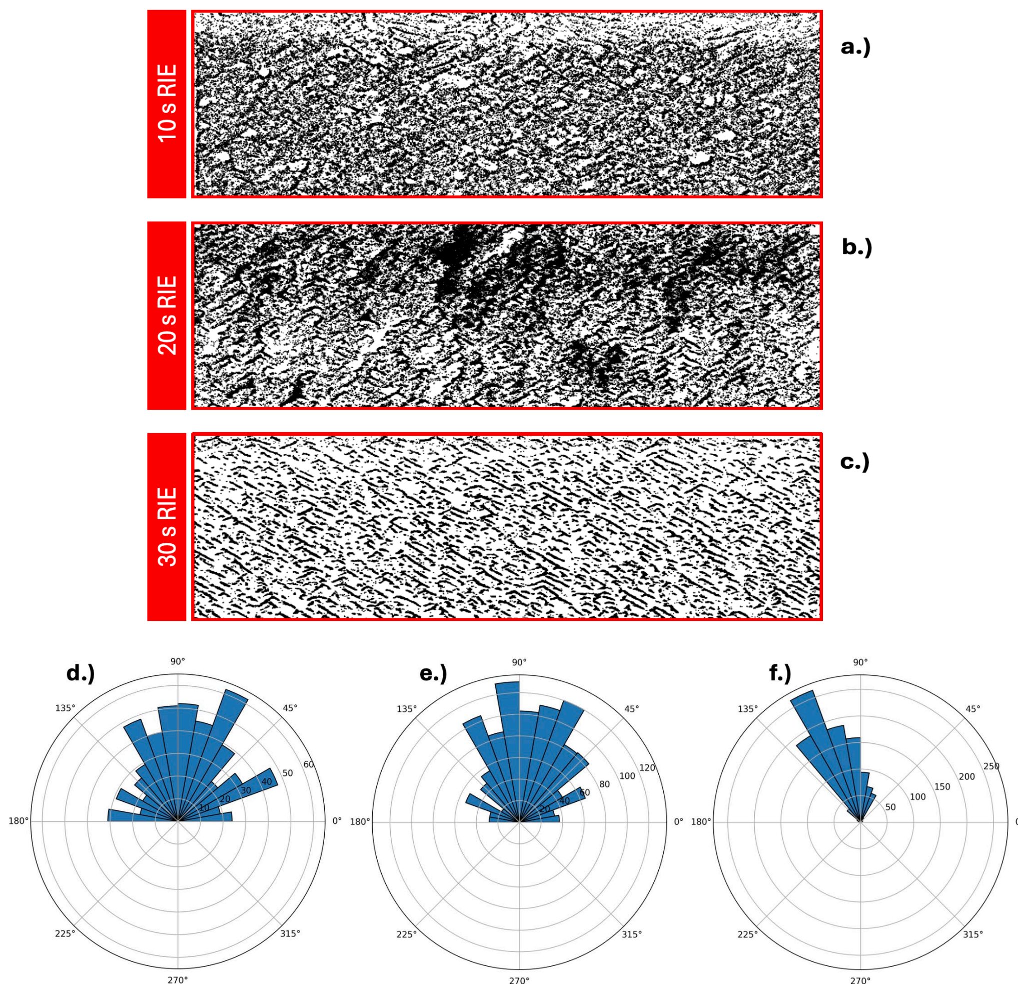

Fig. 5. Binarised SEM cross-section images (a-c) and corresponding polar histograms (d-f) of porous structures after electrochemical etching of samples pretreated by RIE for 10 s (a and d), 20 s (b and e), and 30 s (c and f). The pore orientation was analysed using Python and OpenCV: pores were segmented and clustered into orientation-specific kernels, then approximated by ellipses to extract the main axis direction. The resulting angle distribution was visualised in polar histograms, revealing increasing pore alignment with longer RIE duration.

Compared with MAPCE pore nucleation, the RIE pre-treatment removes a significant contamination possibility (Pt/Au residues) and avoids lithography or FIB. It uses standard precursor gas chemistry (SF_6/O_2) and short recipes compatible with front-end cleanliness protocols. In integration terms, the present method is complementary to our ECE-based foil release and high-temperature compactification: RIE-assisted ECE can pre-define homogeneous porous layers on the Si-face, after which ECE and post-annealing can yield homogeneously compactified, crystalline surfaces suitable for bonding to alternative carriers, similar to the ELTRAN® approach in silicon [10] [2]. The trade-off between nucleation reliability and surface roughness is evident: 30 s RIE provides the best alignment but increases R_a to ~5 nm after ECE. We hypothesise that the benefit from RIE derives from two coupled factors: (i) nanoscale topography that locally concentrates the interfacial field and (ii) a modified near-surface chemistry/defect state that lowers the barrier for pore nucleation.

Summary

We demonstrate a CMOS-compatible route to reliably initiate homogeneous pore formation on the Si-face of 4H-SiC without noble metals or added lithography. A short O_2/SF_6 reactive-ion etch (10–30 s, 300 W) raises the surface roughness from ~1.3 nm to ~4.0 nm, which is sufficient to seed uniform electrochemical etching in HF/ethanol (no UV required for highly conductive wafers). The increased roughness on the nanoscale correlates with (i) suppression of the initial current spike in the ECE transient, (ii) higher pore nucleation density with smaller pore diameter, and (iii) tighter pore-orientation distributions, yielding laterally uniform porosification across cm-scale areas. AFM/SEM and cross-sectional image analysis confirm a progression from sparse, misoriented pores (10 s RIE) to dense, aligned morphologies (30 s RIE). Compared with MAPCE-based preconditioning, the proposed RIE step is simpler, contamination-resilient, and backend-compatible. It can be combined with established ECE processes to engineer porosity profiles for applications such as photonics, power electronics, or MEMS. Overall, controlled nano scaled roughness (~4 nm RMS) is identified as a practical initiator for robust, homogeneous porosification even of the Si-face of 4H-SiC samples.

Further investigations will focus on the structural and chemical analysis using AFM, TEM, XPS and ToF-SIMS to identify the driving mechanisms of pore nucleation. Future investigations will be performed in a 3-electrode ECE setup to improve the validity of the current response.

Acknowledgement

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