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Study on Electrochemical Assisted Fixed-Abrasive Lapping for Wafer Thinning of Monocrystalline Silicon Carbide Wafer

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Abstract. This study aims to develop an electrochemical assisted fixed-abrasive lapping (ECAL) process for thinning 4H-SiC wafers (C-face). Process with 20 wt% $NaNO_3$ electrolyte to generate a softened passivation layer has been formed and simultaneously removed by a fixed diamond lap wheel. Electrochemical tests using a potentiostat have verified 20 V as the selected experimental potential, and a significant reduction in hardness has been confirmed by nanoindentation. Under these conditions, the 4-inch wafer has achieved a material removal rate (MRR) of 3.181 μm/h with wafer quality (Bow –7.80 μm, Warp 48.50 μm, TTV 7.70 μm). When the same conditions have been applied to 6-inch wafers, an MRR of 2.457 μm/h and wafer quality (Bow –5.00 μm, Warp 36.70 μm, TTV 6.60 μm) have been obtained. These results have demonstrated the scalability of ECAL for larger SiC substrates, offering potential for next-generation device manufacturing.

Introduction

Monocrystalline silicon carbide (SiC) is a key material for high-power applications such as electric vehicles, renewable energy systems, and 5G communication technologies due to its wide bandgap, high thermal conductivity, and excellent breakdown field. To meet the packaging and reliability demands, wafer thinning becomes an essential process for improving heat dissipation capability and ensuring reliable device operation. However, conventional thinning processes often introduce sub-surface damage (SSD) and residual stress, which have been identified as having negative impact on wafer quality and device performance. Therefore, an electrochemical assisted fixed-abrasive lapping (ECAL) process has been developed in this study, combining electrochemical reaction with mechanical removal of material, with the aim of reducing surface damage while improving process efficiency.

Research and Experimental Conditions

An electrochemical assisted fixed-abrasive lapping (ECAL) process has been developed for 4-inch and 6-inch 4H-SiC wafers, in which the wafer has been connected as the anode and the diamond lapping plate as the cathode. The process schematic and setup are shown in Fig. 1. A direct current has been applied through the electrolyte to form a passivation layer on the wafer surface, which has been simultaneously removed by the lapping plate during processing. Electrochemical characterization has been first carried out using a potentiostat to determine the potential and electrolyte conditions used in the subsequent ECAL experiments. Potentiodynamic polarization curves obtained in 20 wt% $NaNO_3$ at 70 °C have revealed a distinct passivation region, from which an applied potential of 20 V has been selected as shown in Fig. 2. Potentiostatic polarization tests further have indicated that at 20 V, the current density has the highest initial value and has rapidly decayed, resulting in a stable level within 60 s as shown in Fig. 3.

To investigate the mechanical effect of passivation, nanoindentation hardness tests have been conducted on untreated wafers and wafers after 20 V anodic polarization. For the untreated SiC wafer,

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the hardness has been measured as 24.59 GPa and the Young's modulus has been measured as 271.56 GPa. Under the condition of 20 V, the hardness has decreased significantly to 1.50 GPa and the Young's modulus to 64.60 GPa, confirming the formation of a softened passivation layer as shown in Fig. 4. Although tests at 15 V and 25 V have also been performed, the 20 V condition has been selected for subsequent experiments, as it has revealed stable passivation behavior.

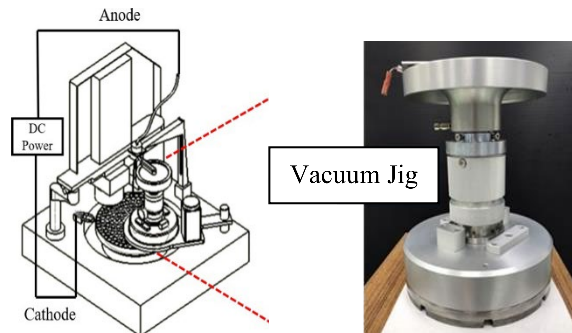

Fig. 1. Schematic and experimental setup of ECAL process [2].

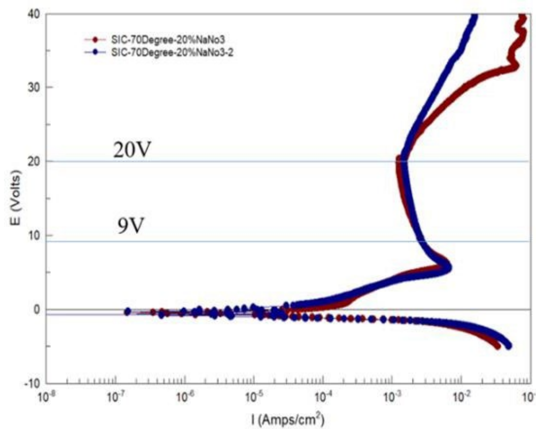

Fig. 2. Potentiodynamic polarization of SiC in 20 wt% $NaNO_3$ at 70 °C [2].

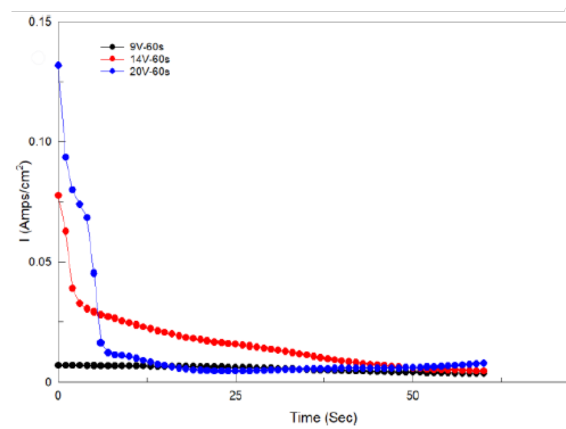

Fig. 3. Potentiostatic polarization of SiC at 20 V for 60 s [2].

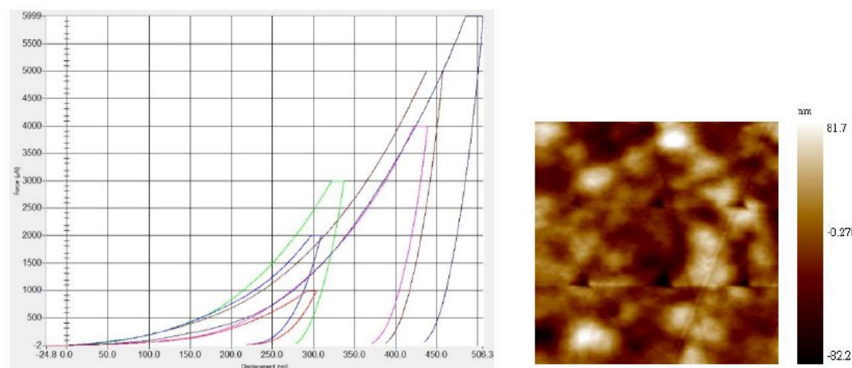

Fig. 4. Nanoindentation load and displacement curve under 20 V [2].

The ECAL process for 4-inch SiC wafers has been performed with a $NaNO_3$ electrolyte concentration of 20 wt%, an applied potential of 20 V, a head/platen rotation speed of 50/60 rpm, and a down pressure of 3 psi, ensuring uniform and stable contact between the SiC wafer and the diamond lap wheel. To verify the scalability of the process, the same electrochemical and mechanical parameters have been applied to 6-inch wafers. The electrochemical mechanism is illustrated in Fig. 5.

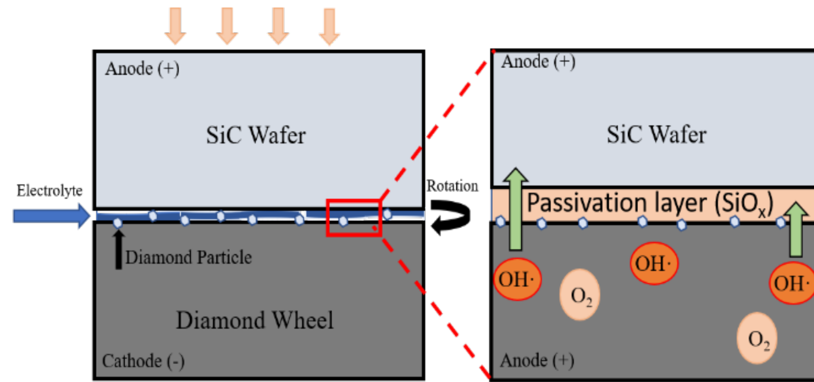

Fig. 5. Electrochemical reaction mechanism.

Results and Discussion

Based on the electrochemical reaction studies of 4H-monocrystalline silicon carbide (4H-SiC), the electrolyte parameters have been determined to be 70 °C and 20 wt% $NaNO_3$ from potentiodynamic polarization experiments. Potentiostatic tests further have indicated that 20 V provides the highest and distinct passivation layer growth rate. Under these conditions, electrochemical assisted fixed-abrasive lapping (ECAL) experiments have been carried out on 4-inch SiC wafers using a #800 diamond lapping plate. The effects of down pressure and rotational speed on MRR and surface quality have been evaluated, as summarized in Table 1.

Table 1. 4-inch SiC wafer (C-face) ECAL parameters [2].

4-inch SiC wafer lapping parameters	
Process	ECAL
Diamond Plate	#800
Down Pressure	1 psi / 3 psi
Electrolyte Type	$NaNO_3$ 20 wt%
Temperature	70°C
Flow Rate	0.5 L/min
Head/Platen Rotation Speed	30/40 rpm, 50/60 rpm
Process Time	1 h

In this section, the results of the ECAL process for 4-inch monocrystalline silicon carbide (SiC) wafers under different experimental parameters are summarized. The discussion focuses on the effects of varying down pressure and rotational speed on wafer surface quality and MRR. At 1 psi and 30/40 rpm, MRR_H has been measured as 1.770 μm/h and S_a 0.4394 μm. At the same pressure with 50/60 rpm, MRR_H has increased to 1.938 μm/h and S_a 0.4888 μm. For 3 psi and 30/40 rpm, MRR_H has reached 2.213 μm/h and S_a 0.5085 μm. The highest efficiency has been obtained at 3 psi and 50/60 rpm, with MRR_H 3.180 μm/h and S_a 0.6538 μm.

The 4-inch 4H-SiC wafer after ECAL processing under the 3 psi and 50/60 rpm as shown in Fig. 6. According to the experimental results, higher pressure and speed have enhanced the MRR but have slightly degraded the surface quality. The corresponding wafer quality results are summarized in Table 2. Although the Warp value has been slightly higher, the overall wafer has maintained good flatness and can be further improved by subsequent CMP processes.

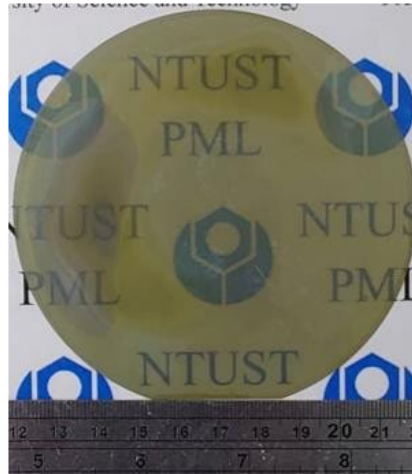

Fig. 6. 4-inch 4H-SiC after ECAL processing [2].

Table 2. Measurement results of Bow, Warp, TTV for 4-inch 4H-SiC [2].

Wafer quality after ECAL process			
Experimental Parameters	Bow/Warp/TTV	Experimental Parameters	Bow/Warp/TTV
1 psi 30/40 rpm	Bow：–2.22 μm Warp：37.02 μm TTV：6.29 μm	1 psi 50/60 rpm	Bow：–4.20 μm Warp：39.2 μm TTV：6.63 μm
3 psi 30/40 rpm	Bow：–4.82 μm Warp：39.63 μm TTV：7.71 μm	3 psi 50/60 rpm	Bow：–7.80 μm Warp：48.50 μm TTV：7.70 μm

To evaluate the scalability of the ECAL process, the same conditions have been applied to 6-inch monocrystalline SiC wafers. The resulting MRR is lower than that of the 4-inch wafers, with an MRR_H of 2.457 μm/h and S_a of 0.457 μm. This reduction has been attributed to the reduced current density on the larger surface area, while the surface roughness has remained comparable and relatively stable.

The wafer quality after ECAL has been summarized in Table 3. For the 6-inch wafers, Bow, Warp, TTV have been measured as –5.00 μm, 36.70 μm, and 6.60 μm, respectively. The 6-inch wafer has maintained overall flatness and surface condition after ECAL processing, with the Bow/Warp/TTV measurement map shown in Fig. 7(a) and the wafer photograph after processing in Fig. 7(b).

Table 3. 6-inch SiC Wafer (C-face) ECAL parameters [2].

6-inch SiC wafer lapping parameters	
Process	ECAL
Diamond Plate	#800
Down Pressure	3 psi
Electrolyte Type	$NaNO_3$ 20 wt%
Temperature	70°C
Flow Rate	0.5 L/min
Head/Platen Rotation Speed	50/60 rpm
Process Time	1 h

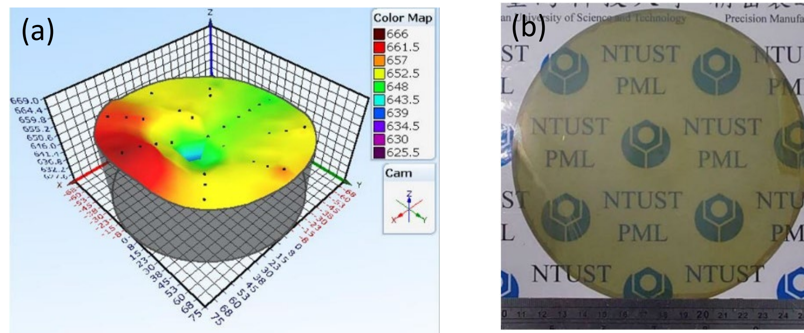

Fig. 7. (a) 6-inch 4H-SiC Bow/Warp/TTV measurement
(b) 6-inch 4H-SiC after ECAL processing [2].

Conclusion

In this study, the electrochemical assisted fixed-abrasive lapping (ECAL) process has been demonstrated on 4-inch and extended to 6-inch 4H-SiC wafers. Electrochemical analyses have confirmed that 20 V has provided stable passivation, enabling effective wafer thinning. The applied process parameters have resulted in high removal efficiency while maintaining wafer flatness. The successful demonstration on 6-inch wafers has emphasized the scalability of ECAL for next-generation SiC substrates. Future work can focus on further optimizing electrochemical conditions and integrating ECAL with CMP to improve overall wafer quality. These findings have demonstrated that ECAL has strong potential for integration into large-scale SiC wafer manufacturing, contributing to improved device performance in power electronics and communication applications.

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