Materials Science Forum *Online: 2008-03-24*
ISSN: 1662-9752, Vols. 573-574, pp 165-180
doi:10.4028/www.scientific.net/MSF.573-574.165

High-k: latest developments and perspectives

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Keywords: High-k, Hf-silicate, interface layer, capping layer, SONOS, memory.

Abstract. The paper reviews recent progress and current challenges in implementing high-k dielectrics in microelectronics. Logic devices, non-volatile-memories, DRAMs and low power mixed-signal components are found to be the technologies where high-k dielectrics are implemented or will be introduced soon. Two gate architectures have to be considerd: MOS with metal as gate electrode and MIM. In particular, Hf-silicates for logic and NVM devices in conventional MOS architecture and ZrO_2 for DRAM cells in MIM architecture are discussed.

Fields of applications

The breakthrough and thus the enormous growth of the microelectronics, especially in the Information Technology, in the past few decades is based, to a large extend, on the SiO_2/Si system which was therefore called "a simple gift of nature". Gate dielectrics consisting of ultra thin silicon dioxide layers are the key element in conventional silicon based microelectronic devices. In the very beginning of the microelectronics, the thickness of the SiO_2 gate oxide was a few hundred nanometers. Nowadays, state-of-the-art MOSFETs (metal oxide semiconductor field effect transistor) require gate oxide thicknesses of just a few atomic layers. Until recently, the continuous scaling of the ULSI (ultra large scale integration) devices has been accomplished by shrinking physical dimensions. Physical gate oxides with physical thicknesses in the range of 1.6 nm are currently fabricated and thicknesses below 1.0 nm will be requested for future device generations [1]. In this thickness range, key dielectric parameters degrade, like gate leakage current, channel mobility, reliability etc. [2,3,4]. Thus, the necessity arises to replace the SiO_2 with a dielectric of higher permittivity [5,6]. Application of oxides with a higher dielectric constant (high-k) allows for a physically thicker insulating layer with the same capacitance per unit area as that required for SiO_2. The so-called equivalent oxide thickness (EOT) is defined as follows:

$$EOT = d_{high\text{-}k} \cdot k_{SiO2} / k_{high\text{-}k} \,. \quad (1)$$

$d_{high\text{-}k}$ is the physical oxide thickness, k_{SiO2} and $k_{high\text{-}k}$ are the dielectric constant of the silicon dioxide and the high-k oxide, respectively. But, the high-k dielectric has to satisfy several requirements to fulfil all the demands of state-of-the-art gate dielectrics. First, it has to be thermodynamically stable in contact with silicon [7], it must be process compatible with CMOS (complementary MOS) and withstand source/drain implant annealing, oxygen diffusion should be low to prevent generation of a sizeable SiO_2 interface layer (IL) or trapping defects [8], and it must have sufficiently high band offsets to act as barrier for electrons and holes [9]. Also, the high-k oxide has to show a high quality interface to silicon, with only few interface or defect states within the silicon band gap, be-

cause the performance of a field effect transistor strongly depends on the quality of the dielectric-silicon interface [10].

Moreover, the development of an oxide insulator technology, that is not thermally grown, for the conventional silicon semiconductor technology may make the application of a similar approach to other semiconductors (e.g., Ge, GaAs, and SiC) feasible promising improved MOS device performance for these semiconductor materials [10].

The DRAM technology was among the first which had introduced high-k oxides into the devices. High-k oxides (e.g., Ta_2O_5, Al_2O_3) have been inserted to stack-cell capacitors, because they are formed after the transistors [11]. If the thermal budget of transistor processing is too high, capacitor performance will be degraded. Therefore trench capacitors are less suitable for integration of high-k oxides [12]. But, at the latest, for the 48 nm technology generation high-k oxides have to be adopted for trench capacitors [13], too. Most probably, metal-insulator-metal (MIM) capacitors will be introduced. Depending on the processing sequence, however, either capacitor before transistor or transistor before capacitor formation, different demands have to be fulfilled by the high-k oxides.

The minimum feature size of flash and charge-trapping memory devices has been reduced below that of DRAM memory products [1]. To keep up with this development, the reduction of the EOT of SONOS (silicon oxide nitride oxide silicon) memory stacks is of great concern. The introduction of a high-k oxide into the ONO-gate stack is very promising to reduce EOT [14,15,16,17]. Especially, the replacement of silicon dioxide as the material of the blocking oxide with various high-k oxides has shown significant improvements for several flash memory properties [18,19].

Integration of precision MIM capacitors into high performance technologies has been a key building block for mixed-signal IC applications, such as low offset voltage operational amplifiers, analog frequency tuning circuits, switched capacitor circuits, filters, resonators, digital-to-analog (D/A) and analog-to-digital (A/D) converters [20]. The use of MIM capacitors in these applications has attracted great attention because of their highly conducting electrodes and low parasitic capacitances [21,22,23]. A high capacitance density is required for a MIM capacitor to allow for small area, to increase the circuit density, and to further reduce the manufacturing costs. Therefore, adoption of high-k oxides is a very efficient way to increase the capacitance density [24].

The above examples illustrate that high-k oxides will be necessary in nearly all fields of applications in microelectronics, sooner or later. For stack-cell structured DRAM capacitors and for precision MIM capacitors for mixed signal applications, products with high-k oxide inside are already on the market. In 2007 Intel and IBM have announced that for their next processor technology generation high-k oxides will be the choice as material for the gate dielectric [25,26]. Great efforts have been made to fabricate high-k oxides ready for the market, but even greater common efforts have to be undertaken to scale further down the thickness of the high-k oxides by keeping the very high standards in microelectronics or even to enlarge it. In contrary to silicon dioxide, one big challenge proves to be the varying demands on high-k for different fields of applications. For example, for logic devices the thickness of the high-k oxide and the interface to silicon (e.g., to get a high on-current) is of utmost importance, whereas the leakage current is the critical parameter (e.g., to get long retention times) for memory application. Therefore, high-k oxides with different properties have to be considered for any of the various applications.

Selection of high-k oxide

The requirements on high-k oxides are challenging. Beside the absolute need for a higher k-value, the thermal stability inside the layer and with the interfaces of the high-k oxides to the substrates or the electrodes, the energy band offsets to the substrates or the electrodes, and interface and bulk charges inside the dielectric, are among others the most important properties which high-k oxides have to fulfil to satisfy the big challenges of future CMOS production processes [27]. The dielectric constant, k, and the energy band-offset values, ΔE_C and ΔE_V, between the conduction and the valence bands of the oxide and the silicon crystal, respectively, are fundamental layer parameters [28,43].

Thermodynamic stability of high-k oxides in contact with Si or with metal is another issue to be considered. Stability requires no or little reaction of the high-k oxide with the silicon or metal to prevent formation of interfacial SiO_2 [4,28] or metal silicides [29]. Depending on the application or the thermal budget which has to be applied after high-k formation, the selection of high-k oxides is limited. Furthermore, thermodynamic stability means no phase separation in compositions, in multi-layer, or in doped high-k oxides (e.g., forming SiO_2 and HfO_2 islands in deposited $HfSi_xO_y$ layers) [30] during successive annealing steps.

Hygroscopicity is another physical parameter which has to be considered. If the oxides of several lanthanides are brought in contact with water (e.g., humidity from the ambience or from cleaning steps) a chemical reaction can occur resulting in the formation of hydroxides [31]. Those hydroxides, however, show significantly increased leakage current densities or/and an increase in EOT. The oxides of La and Lu are very sensitive and the oxides of Gd, Dy, Sm, and Pr are sensitive to water. Hence, an increased operating expense in processing has to be carried out to protect these rare earth oxides from water (e.g., by using capping layers).

To predict promising candidates of high-k oxides for different applications some physical properties of the dielectrics have to be considerd. The dielectric constant, k, is determined by the polarizability, α. The relation between the two quantities is given by the Clausius-Mosotti expression [32]:

$$k = \frac{1 + \frac{2}{3} 4\pi \frac{\alpha}{V_m}}{1 - \frac{1}{3} 4\pi \frac{\alpha}{V_m}} \tag{2}$$

where V_m is the volume per molecule in the dielectric and the simple case assumed of a completely homogenous material surrounding the polarized molecule [33]. This is expressed by the factor 1/3 in the equation. Fig. 1 shows the dependence of the k-value on the ratio α/V_m. For a value of ≈ 0.24, it has an asymptote to infinity. Beside the molecular polarizability, α, it is obvious that the volume occupied per molecule, V_m, determines the k-value. Hence, the material structure, whether amorphous or arranged in different crystalline geometries, may have a considerable influence on the k-value. Furthermore, when α/V_m approaches the asymptote, a small change in the crystallinity of the structure may give rise to a large change in the dielectric constant [34].

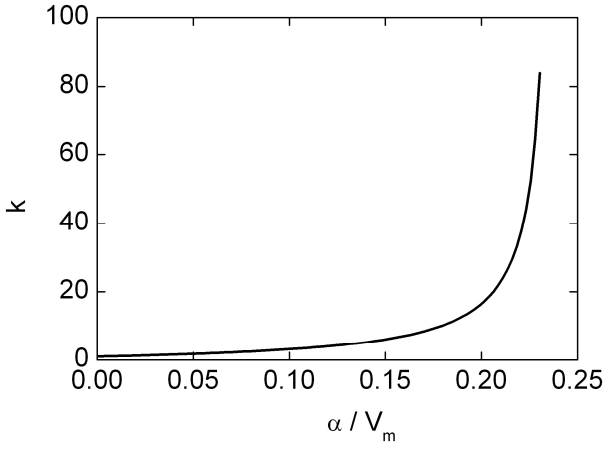

Figure 1: k-value as a function of the ratio between polarizability and molecular volume as given by Eq. (1)

The fourth factor is the band offsets. The band offsets at both valence and conduction band should be above about 1 eV in order to suppress the current injected into the oxide. Fig. 2 shows the band offsets between the conduction bands of different high-k oxides and silicon as a function of their respective k-value [28]. It is evident that the band offsets of many high-k oxides are considerably low. Indeed, the band gap tends to vary inversely with the k-value. Hence, band offsets can quite easily be below 1 eV. Therefore, the adoption of suitable high-k oxides on silicon substrate can be restricted,. Deposition of high-k oxides on metal electrodes with appropriate work-function can compensate the restriction in some cases.

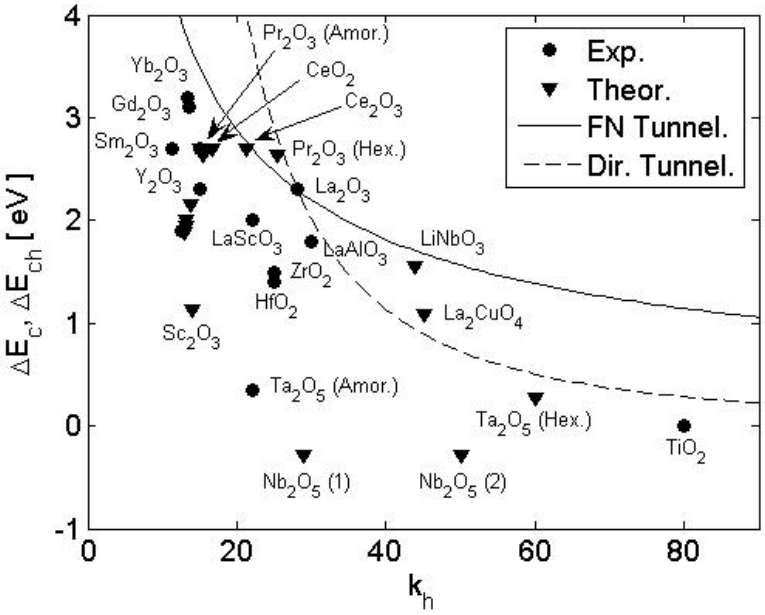

Figure 2: Band offset between conduction bands for different high-k oxides and silicon as a function of k-value [28]. Filled circles are experimental values from the literature, triangles are values where ΔE_{ch} has been predicted in [28].

The fifth factor is stability versus processing and electrical quality. This will be discussed mainly with HfO_2 as an example for high-k oxides. Depending on HfO_2 thickness, crystallization into predominantly monoclinic polycrystalline films occurs at 300-500°C deposition temperature or subsequent annealing step [35,36,37]. Moreover, additional interfacial SiO_2 is often formed, increasing EOT [38]. It can be assumed that grain boundaries in polycrystalline high-k oxides may provide paths for leakage current and, therefore, giving rise to increased leakage current densities. But, this was not conclusively proved by experiment [36]. However amorphous high-k oxides are preferred for other reasons. Grain boundaries were also suspected to be responsible for localized unoccupied states below the conduction band edge of high-k oxides. Such band edge defect states have been shown to occur in HfO_2 if and only if the dielectric exhibit crystallinity as detected by infrared spectroscopy, X-ray diffraction, and vacuum ultraviolet spectroscopic ellipsometry [39]. Such states are very close to the high-k oxide band edge and may not explain the significant increase in leakage current densities for polycrystalline layers. However, if defect states due to grain boundaries exist at the band edge it is very likely that defect states exist deeper in the band gap, too. Such defect states may explain why Poole-Frenkel hopping through the dielectric, which occurs via trapping sites, is the preferred conduction mechanism in high-k oxides. Therefore, it appears preferable to apply only amorphous high-k oxides [4]. In order to minimize crystallization and to reduce interfacial SiO_2 formation, the thermal stability of the high-k oxides can be increased by adding Si, Al, or N to the dielectric [36,39,40,41,42]. But, HfAlO gate dielectrics show reduced carrier mobility in the transistor channel which may be due to fixed charges in the layer [41]. Therefore, HfSiO or HfSiON layer are preferred. With the incorporation of small quantities of Si into the high-k oxide, electron peak mobility identical to that of low N-content SiON control devices can be reached. Since Si-O bonds

are stiffer than Hf-O bonds, soft phonon modes, which are suspected to reduce charge mobility, are reduced in intensity [4]. Additional N incorporation optimizes electrical thickness and thermal stability. However, N near the channel reduces carrier mobility through coulomb scattering by fixed charges. Thus, N incorporation is preferred near the top of the HfSiO [4].

For logic devices, it turns out that a thin interfacial SiO_2 layer is mandatory between the bulk silicon and the high-k oxide. The IL raises the EOT, but the performance of the transistor degrades severely without it. Therefore, a compromise between thickness and dielectric constant of the interfacial layer (e.g., by adding nitrogen to the IL which increase the dielectric constant and reduces IL growth during subsequent annealing steps) has to be found [4].

Until now, one of the biggest challenges to be met with high-k oxides is the stability of the threshold voltage. Threshold voltage shift of devices incorporating high-k oxides is probably caused by an oxygen deficiency in the dielectric layer which may be formed during annealing steps [44]. It is still unclear whether O can be reintroduced into the dielectric without unacceptable SiO_2 growth at the interface, and whether such O content can be maintained throughout a full CMOS integration flow. Capping layers deposited on the high-k oxide to minimize oxygen diffusion have shown that sufficient threshold voltage improvement can be achieved without degrading overall device performance [45,46,47]. Because gate electrodes consisting of poly-Si show a lot of drawbacks, significant research has been conducted on high-k/metal gate stacks which have shown the ability to scale EOTs below 1 nm while maintaining high electron mobility and low leakage current [48,49]. As for poly-Si gates discussed above, also for metal gates capping layers inserted between the high-k oxide and the metal gate are analyzed to adjust properly the threshold voltage [50]. But, controllable and reliable threshold voltage control still remains a potential issue.

Nevertheless, high-k oxides deposited by metal organic chemical vapour deposition (MOCVD) or atomic layer deposition (ALD) have the highest potential to substitute conventional SiO_2 as gate dielectric. Several examples where the implementation of high-k oxides in various device technologies is examined are illustrated using the following three examples:

HfSiO for logic devices

In this part, hafnium silicate layers on Si and Ge substrates are analyzed for gate dielectric application in logic devices. For future technology generations the hole mobility in the silicon channel of p-MOS transistors seems no longer high enough for advanced CMOS application. Ge instead of Si may be a promising alternative. Therefore, modified substrates, such as strained Si, SiGe, or Ge layers [1] are under investigation.

Physical characterization. Films were deposited by metal organic chemical vapour deposition using the single-source precursor $Hf(acac)_2(OSi^tBuMe_2)_2$. This precursor exhibits good properties in terms of hydrolysis stability, volatility, and deposition. The quantitative analysis of $Hf_xSi_yO_z$ layers deposited on Si wafers by X-ray photoelectron spectroscopy (XPS) reveals a high C contamination of up to 20 at.-% in as-deposited films. Carbon is known to be unfavourable for electrical properties (e.g., it increases leakage currents). Therefore, several attempts to reduce C content in the films as well as to analyze the thermal stability of $Hf_xSi_yO_z$ on Si were performed using different rapid thermal annealing (RTA) steps. Table 1 summarizes the results obtained on Si wafers for different RTA conditions and layer thicknesses (sample labeled A to F). Stoichiometric coefficients x, y, and z for $Hf_xSi_yO_z$, C content, and physical thickness before and after RTA are given. All XPS-spectra were measured in approx. 2 nm to 5 nm depth from the surface after Ar sputter cleaning. As discussed previously [51,52], C-free films can only be obtained after an O_2-RTA (A, B compared to C to F), which leads to structural changes (i.e., decreasing physical thickness $d_{annealed}$ (C to F)) and Si redistribution in the layers (i.e., change in stoichiometry compared to uniform as-deposited films [52] (A, D to F)). With decreasing layer thickness, Si enrichment in the dielectric film was observed after anneal (D to F).

sample	T_{dep} [°C]	$d_{as\text{-}dep.}$ [nm]	RTA	$d_{annealed}$ [nm]	stoichiometric coefficient Hf_x	Si_y	O_z	C [at.%]
A	550	14.6	w/o	14.6	0.78	0.22	2.1	18
B	550	14.6	700 °C / 10 s / N_2	13.0	0.80	0.20	1.9	20
C	550	14.6	700 °C / 10 s / O_2	11.0	0.86	0.14	2.0	-
D	550	14.6	900 °C / 10 s / O_2	10.5	0.86	0.14	2.0	-
E	600	7.7	900 °C / 10 s / O_2	6.5	0.62	0.38	1.7	-
F	575	6.6	900 °C / 10 s / O_2	5.2	0.52	0.48	1.7	-

Table 1: Effects of different RTA steps and decreasing layer thicknesses on stoichiometric coefficients x, y, and z for $Hf_xSi_yO_z$ (x+y = 1), C content, and change in physical thickness. Results are obtained on Si wafers [51].

In Fig. 3, high resolution TEM images for representative gate stacks with thick dielectric (as-deposited (A) and O_2-annealed (D)) as well as thin dielectric (O_2-annealed (F)) are shown. It should be noted that even for the as-deposited film (Fig. 3a), which was deposited immediately after removal of the native oxide by a HF dip, an interfacial layer of 1.3 nm thickness was grown, most probably SiO_x. Annealing the dielectric layer in oxygen atmosphere resulted in an increase of the interfacial layer thickness of about 3 nm irrespective of high-k layer thickness (Fig. 3b, c). Therefore, undesirable effects on electrical properties like increasing effective oxide thickness are expected. Another effect of the O_2-RTA step is a change in morphology. As-deposited layers reveal an amorphous structure, while annealed films exhibit a poly-/nano-crystalline structure in the case of thick films (indicated by the two different lines for the lattice planes in Fig. 3b) and completely crystalline structure in the case of thin films (Fig. 3c). It should be mentioned that for all samples identical RTA steps at 900 °C for 10 s in O_2 atmosphere were performed. Another interesting result refers to the metal/dielectric interface. For the as-deposited layer (Fig. 3a), a rough surface layer with a large thickness variation of 1.7 nm is seen. After RTA, this interfacial layer is smoothed and its thickness decreases to 1.2 nm for the thick layer (Fig. 3b). An explanation may be the carbon elimination along with film densification and structural changes. In case of a thin film (Fig. 3c) with identical metal electrode (Ni) deposited on top after RTA, no interfacial layer can be observed, at all.

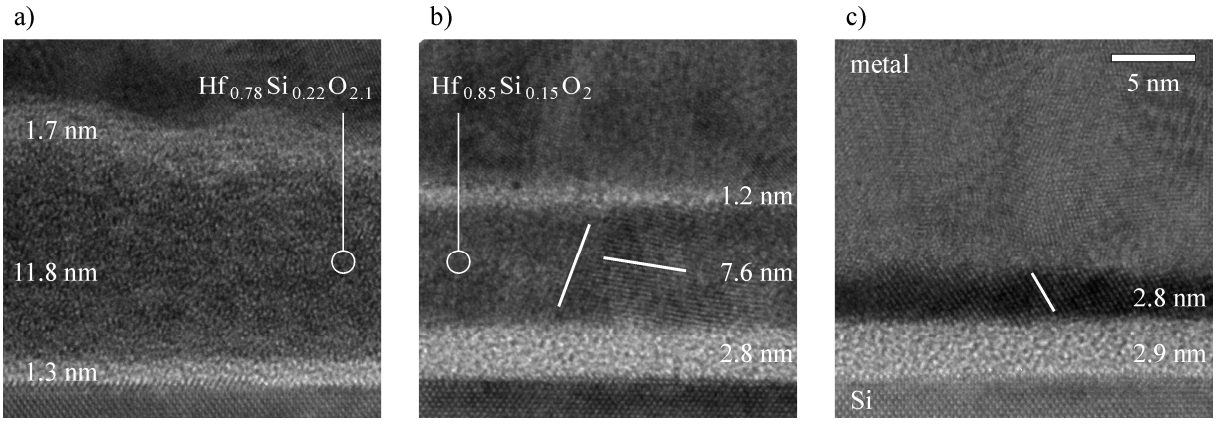

Fig. 3: High resolution TEM images of a) as-deposited 14.8 nm (A), b) O_2-annealed 10.4 nm (D) and c) O_2-annealed 5.7 nm (F) thick hafnium silicate layers on Si.

High-k oxides were deposited on Ge wafers, too. The deposition behaviour of $Hf(acac)_2(OSi^tBuMe_2)_2$ precursor changes compared to Si wafers. As discussed previously [51], TEM images (not shown here) reveal a three-layer structure of the dielectric stack similar to the results obtained for Si wafers. But, in contrary to the depositions on Si wafers, RTA causes no den-

sification of high-k layers on Ge wafers (i.e., layer thickness is unchanged) and XPS analysis identifies the bulk dielectric to be stoichiometric hafnium oxide.

To further analyze these findings, 16 nm thick high-k layers were deposited on both, blank and nitrided Ge wafers. Pre-deposition nitridation of the Ge surface was done by rapid thermal nitridation (RTN) at 600 °C for 120 s in NH_3 atmosphere. After HfSiO deposition, one part of the sample received a RTA (700 °C / 10 s / O_2 atmosphere) and was analyzed by XPS. Fig. 4 shows the XPS results obtained at the surface and in the bulk of the high-k oxide. Unlike to Si samples, no C is detected in the bulk of as-deposited films within the detection limit of XPS. This is rather unexpected, as Si samples showed C contamination of up to 20 at.-% under identical deposition conditions. This indicates a change in precursor decomposition mechanisms for different surfaces (i.e., Si and Ge wafers). For the as-deposited films, Si is detected in both cases of blank and nitrided Ge wafers in the surface region of the high-k oxide. Values of 6 at.-% to 7 at.-% of Si are obtained for samples without and with RTN (rapid thermal annealing), respectively. But, no Si can be measured in the bulk dielectric within the detection limits of XPS.

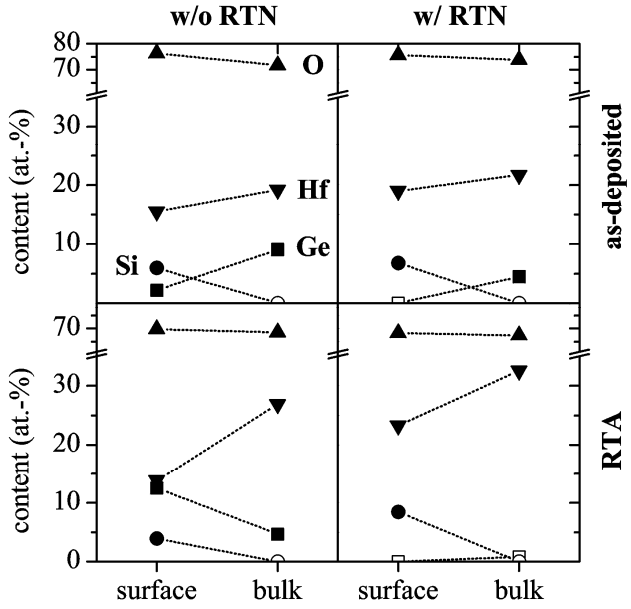

Figure 4: Film composition determined by XPS of a 16 nm thick high-k dielectric deposited on both blank and nitrided Ge wafers w/o and w/ post deposition RTA. XP spectra were measured both, directly on the surface and after 3 min of Ar-ion milling. Open symbols indicate results at or below the detection limit of XPS. The lines are drawn as guide for the eye.

Electrical Characterization. High-frequency (100 kHz to 1 MHz) capacitance-voltage (C-V) and temperature dependent current density-voltage (J-V) measurements of the samples labeled A to F in Table 1 and O_2-annealed layers deposited on nitrided [51] Ge wafers (sample label Ge) were performed. Extracted parameters for selected films are summarized in Table 2. For easier comparison, flatband voltage V_{FB} is given with respect to the work function difference Φ_{MS}.

As presented recently [51], C is a main issue for leakage current, especially for high-k oxides deposited by MOCVD. Therefore, post-deposition RTA in O_2 atmosphere is required. Such a RTA step improves electrical properties (e.g., it decreases effective oxide thickness (EOT) and leakage currents), but causes crystallization of the dielectric and growth of an interfacial layer between the dielectric and Si (Fig. 3). For instance, sample D processed with the highest thermal budget of 900 °C for 10 s of all analyzed sample with identical as-deposited film thicknesses of 14.6 nm reveals the lowest EOT of 3.3 nm compared to 5.2 nm of the as-deposited sample (A) and 3.8 nm for the at

700 °C annealed sample (C). However, effective k-values of 12 (including interfacial layers) are similar for this series (Table 2). Hence, the actual permittivity of the deposited $Hf_xSi_yO_z$ layer is even higher. Considering interfacial layer and degree of crystallization of the dielectric layer, which should be maximum for sample D, the permittivity can be correlated to morphology and layer composition (i.e., the higher the degree of crystallization and Hf content, the higher the permittivity). For samples with different film thicknesses annealed under identical conditions (D to F), a reduction of EOT is observed (Table 2). The reason is the formation of a dielectric/Si interfacial layer during RTA, which is of the same thickness of about 2.9 nm for all samples and defines EOT to a great extend. This is a severe drawback, as this interfacial layer limits the down scaling of EOT. For Ge sample (G), an effective k value of about 18 was extracted, which is reasonable taking the stoichiometric HfO_2 bulk dielectric into account.

sample	Film composition [bulk]	EOT [nm]	k	V_{FB}-Φ_{MS} [V]	$N_{eff} = Q_{eff}/q$ [10^{12} cm^{-2}]	current conduction mechanism
C	$Hf_{0.86}Si_{0.14}O_{2.0}$	3.8	11.3	0.2	-1.1	
D	$Hf_{0.86}Si_{0.14}O_{2.0}$	3.3	12.4	-1.1	7.2	FN/PF (1-1.1 eV)
E	$Hf_{0.62}Si_{0.38}O_{1.7}$	3.1	8.2	-0.35	2.4	PF/FAT (0.7-1 eV)
F	$(Hf_{0.52}Si_{0.48}O_{1.7})$	2.9	7.0	-0.96	7.0	acc.: PF/FAT (0.6-0.8 eV) inv.: FN
Ge	$HfO_{2.1}$	4.2	18.6	-0.10	0.5	PF (0.5 eV)

Table 2: Electrical parameters for selected films extracted from C-V and J-V analysis.

To obtain a better insight into electrical film properties with layer thickness as parameter, temperature dependent J-V curves were measured in the range of 25 °C to 180 °C for O_2-annealed Si-based samples (D to F) as well as for the nitrided Ge-based sample (Ge). Fig. 5 displays the obtained J-V characteristics. It is clearly seen that with reducing film thickness (D to F) the shape of J-V curves and the temperature dependence alter. The 10.5 nm thick film (D) reveals distinct temperature dependence for both injection polarities. In addition, good symmetry of leakage current with respect to V_{FB}-Φ_{MS} is observed, which is usually obtained for symmetric potential barriers. With the reduction in film thickness to 6.5 nm (E) and 5.2 nm (F), the asymmetry in J-V curves increases and the temperature dependence vanishes almost completely. These results indicate that with reduced film thickness a change in current conduction mechanism occurs. For the analysis of the current conduction mechanism, both material related conduction (e.g., Fowler-Nordheim (FN) tunneling, direct tunneling) and defect related conduction (e.g., Poole-Frenkel (PF), field-assisted tunneling (FAT)) were considered [53,54].

By plotting J-V curves in FN or PF coordinates, the data of all samples shown in Fig. 5 were analyzed. The results are summarized in Table 2. Thereby, the contributing current conduction mechanisms are listed and, in case of trap related processes, extracted values of trap depths are given. It turned out that trap-related conduction mechanisms dominate the leakage current behaviour in all layers except for the thinnest film (F) under substrate injection, where FN is dominant. An explanation may be the high fraction of SiO_x-rich dielectric at the Si interface. The finding that leakage currents for samples E and F are governed by trap-related field-assisted tunneling (Table 2) can explain the weak temperature dependence observed for these two samples. The FAT process follows an expression similar to FN equation with the only difference that the electrode/dielectric barrier height in FN equation is replaced by the trap energy level [54]. Regarding the energy level of traps involved, a decrease with decreasing thickness, or in other words, a decrease with increasing degree of crystallization and Hf content from 1-1.1 eV for 10.5 nm thick poly-/nanocrystalline Si-containing $Hf_{0.86}Si_{0.14}O_{2.0}$ layer (D) to 0.6-0.8 eV for a fully crystalline layer separated 5.2 nm thick layer (F) was evaluated. These results are in agreement with the dominant value of 0.5 eV determined for the trap energy of a high-k dielectric on Ge wafer (Ge) taking the stoichiometric

HfO_2 bulk dielectric into account. Therefore, we conclude that the trap level with energies of about 0.5 eV and 1 eV are related to Hf and Si bonds, respectively.

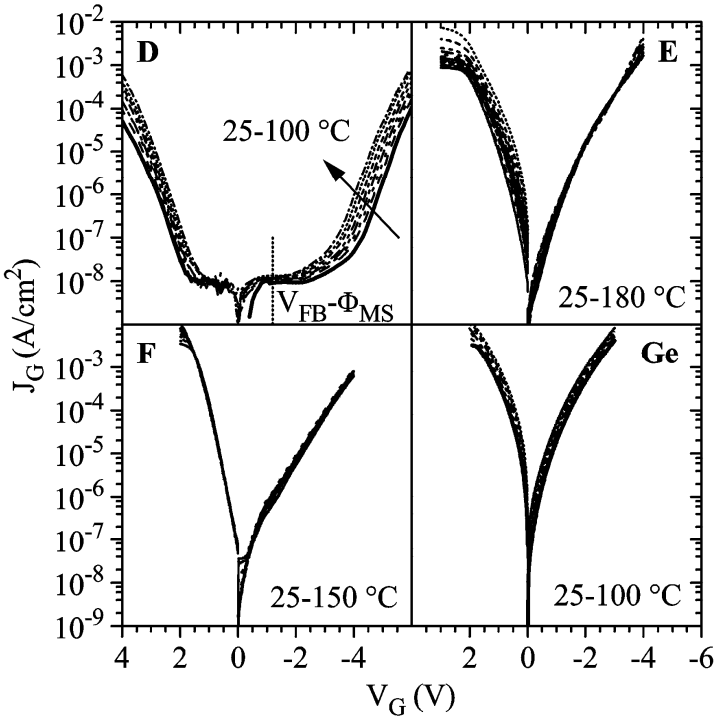

Figure 5: Temperature dependent J-V characteristics of O_2-annealed Si based samples D to F and for films deposited on nitrided Ge wafers (Ge) with thicknesses of the dielectric stack of 10.5 nm (D), 6.5 nm (E), 5.2 nm (F), and 20 nm (Ge).

In summary, post-deposition rapid thermal annealing in O_2 atmosphere causes crystallization of the deposited films, Si/Ge redistribution in the dielectric, and interfacial layer growth. However, oxygen annealing was also found to reduce effective oxide thickness significantly compared to as-deposited films, which is attributed to crystallization effects. But, scaling of effective oxide thickness is limited by the interfacial layer growth. Leakage currents are mainly caused by trap-related conduction mechanisms. Energy levels of involved traps decrease with increasing crystallization and/or Hf content and values of 0.5 eV and 1 eV related to Hf and Si bonds, respectively, are obtained.

HfSiO for SONOS

SONOS-type MIS capacitors with hafnium silicate as a control oxide were characterized and compared to devices with a conventional SONOS gate stack. Samples analyzed in this part were manufactured on p-type silicon substrates. After a tunnel oxide of 5 nm was grown by dry oxidation, an 8 nm thin silicon nitride trapping layer was deposited by LPCVD at 710 °C. Next, a SiO_2 control oxide of 5 nm thickness was deposited by LPCVD from TEOS and densified at 900 °C for 60 minutes in an inert ambient. For several samples this control oxide was etched back to 3 nm in diluted HF and a layer of 8 nm $Hf_xSi_yO_4$ (Hf-rich) was deposited by MOCVD. On top of all of these gate stacks, a metal gate consisting of 10 nm TaN and 300 nm Al was deposited by RF sputtering. Finally, MIS capacitors were structured by lithography and dry etching.

To examine the feasibility of $Hf_xSi_yO_4$ as a control oxide in SONOS-type memory cells, basic memory properties were analyzed. The charge trapping properties of a SONOS-like capacitor with $Hf_xSi_yO_4$ as control oxide using Fowler-Nordheim tunneling as charge injection mechanism are shown in Fig. 6.

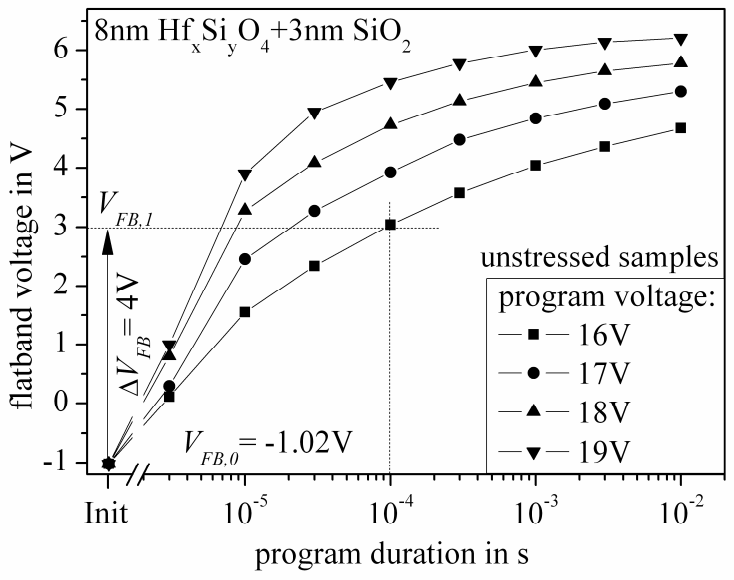

Figure 6: Charge trapping properties of a SONOS gate stack with an 8 nm $Hf_xSi_yO_4$ / 3 nm SiO_2 control oxide stack for various program voltages and pulse durations.

Samples with a control oxide of pure silicon oxide exhibit similar flatband voltages under programming voltages for comparable equivalent oxide thicknesses. This can be explained by the electric field in the tunnel oxide which does not differ for both sample types. Measurements under erase conditions show a significant improvement of erase speed for the samples with $Hf_xSi_yO_4$ in the gate stack. A comparison of erase voltage and duration between both control oxide types is given in Fig. 7.

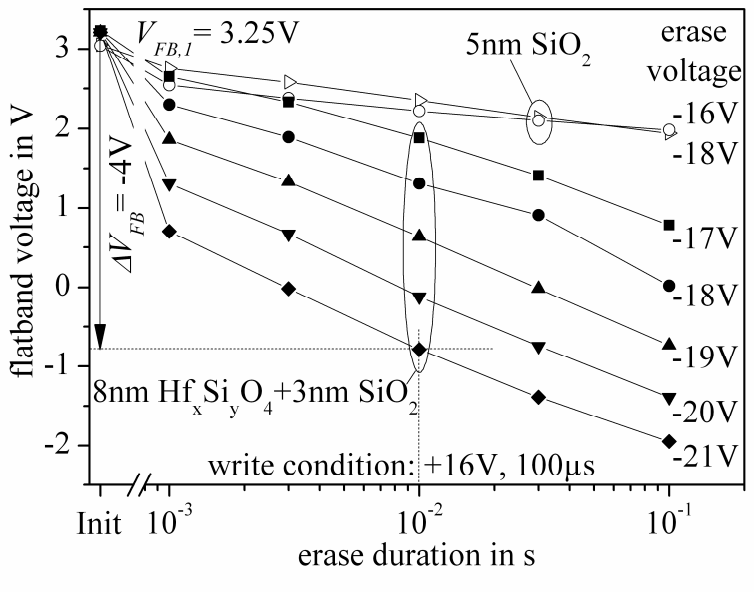

Figure 7: Erase properties of SONOS gate stacks with a 5 nm SiO_2 (open symbols) layer and with an 8 nm $Hf_xSi_yO_4$ / 3 nm SiO_2 (filled symbols) control oxide stack, respectively.

The poor performance of the device with the SiO_2 control gate is due to FN tunneling of electrons from the gate electrode through the control oxide during erase operation. These electrons reoccupy previously emptied traps in the silicon nitride layer and thus hamper the de-trapping process. For the $Hf_xSi_yO_4$ control oxide, however, the electron injection from the gate is efficiently sup-

pressed due to the lower electric field in the silicate. This effect can also be proved by simulating the band bending in the gate stack. FN tunneling of holes from the accumulated substrate ($J_{FN,h}$) becomes the dominant current transport mechanism under high erase voltages [18]. The injected holes recombine with trapped electrons in the nitride layer, thus enhancing the erase operation. Beyond, since the total leakage current in samples with a control oxide of $Hf_xSi_yO_4$ is several decades lower for comparable erase voltages, oxide degradation is expected to be less severe.

Next, the stability of the tunnel oxide in the gate stacks is characterized in accumulation to quantify this observation. The band diagram implies that the breakdown of the gate stack under negative gate bias (erase condition) takes place in the tunnel oxide near the anode due to the high electric field [55]. Constant voltage stress is applied in accumulation because charge injection from the gate is strongly affected by the material of the control oxide. Measurement results are depicted in Fig. 8.

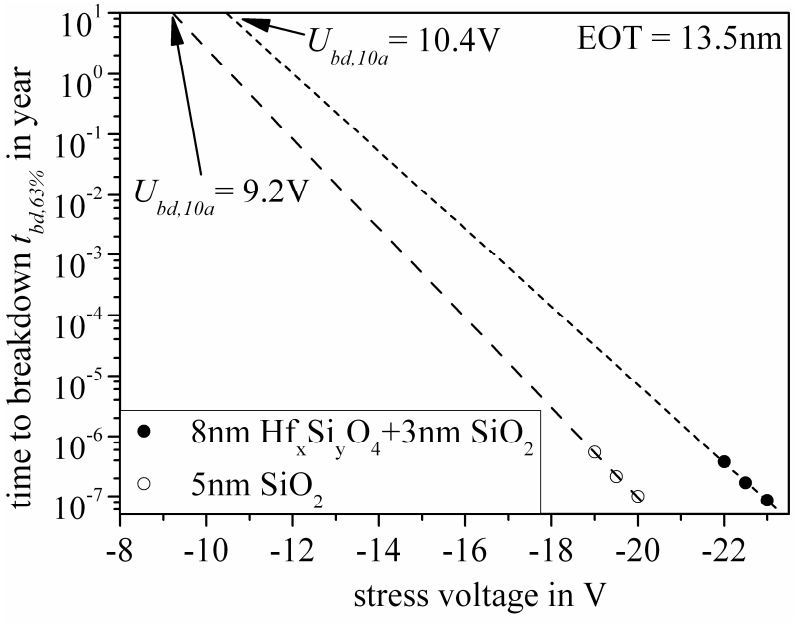

Figure 8: Oxide stability of SONOS gate stacks with different control oxide materials for different stress voltages (symbols) and extrapolation of oxide stability to 10 years (lines)

Each symbol represents the breakdown measurements of 30 individual samples and the subsequent evaluation by Weibull statistics. Collected data were extrapolated assuming an exponential dependence of the electric field on the time to breakdown of the gate stack [55].

As mentioned above, injection conditions for both types of samples are identical in inversion. The gate stacks with $Hf_xSi_yO_4$ sustain higher leakage currents before a breakdown event occurs. This observation is attributed to a less severe degradation at the anode (i.e., in the $Hf_xSi_yO_4$ layer near the gate electrode) due to a lower electric field. It is evident from both inversion and accumulation measurements that dielectric breakdown in gate stacks with $Hf_xSi_yO_4$ occurs under higher write as well as higher erase voltages compared to conventional SONOS gate stacks.

Finally, retention measurements of programmed ("1") and partially erased ("0") test structures at room temperature are performed. Measurement data are compared to a simulation considering thermal emission and trap-to-band tunneling as the dominant charge loss mechanisms. Without band bending, theory predicts that trapped charges in the silicon nitride layer are more efficiently retained by the $Hf_xSi_yO_4$ gate stack than by the conventional gate stack due to the higher physical thickness of the control oxide. Considering effective electron masses and conduction band offsets, the trap-to-band tunneling probability under low fields for the gate stack with $Hf_xSi_yO_4$ is considerably lower than that for the conventional gate stack. However, this is not the case for memory applications where high charge densities have to be retained. In this case, additional discharge is

observed in gate stacks with $Hf_xSi_yO_4$ for both programming states. This charge loss may result from trap-to-band tunneling of trapped charges in the $Hf_xSi_yO_4$ layer to the gate electrode. Additionally, increased tunneling of charges from the silicon nitride layer must be considered due to the strong band bending in the gate stack at high charge densities. For further discussion, band diagrams without external bias for gate stacks with different control oxides are presented in Fig. 9.

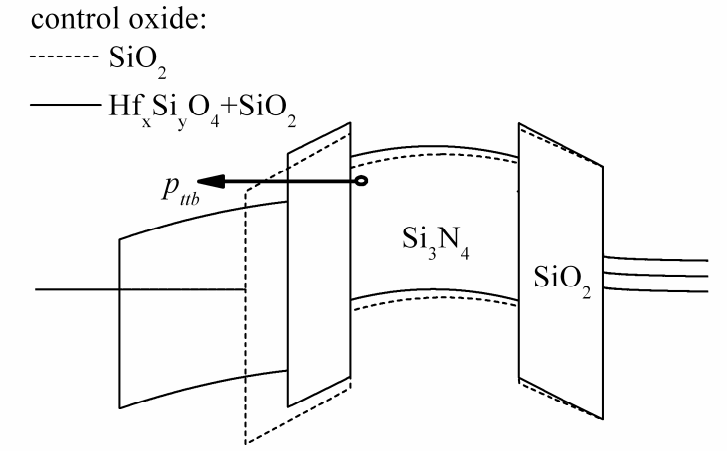

Figure 9: Band bending in SONOS gate stacks with different control oxides for a high density of trapped charges (homogeneously distributed) in the silicon nitride layer without an external bias

Under these conditions trap-to-band tunneling of charges occurs near the control oxide which completely bypasses the $Hf_xSi_yO_4$ layer due to its lower conduction band level. Thereby, the tunneling probability for trap-to-band tunneling p_{ttb} is significantly increased. This charge loss is evident even in the partially erased state for samples with the $Hf_xSi_yO_4$ control oxide.

The application of $Hf_xSi_yO_4$ in the control oxide of charge-trapping memories significantly enhances erase operation by effectively suppressing the tunneling of electrons from the gate. However, an EOT reduction cannot be achieved without degrading retention properties. For the future, the use of TaN as control oxide and a high-k layer with a lower trap density and a higher conduction band offset (e.g., Al_2O_3) [18] is suggested to reduce the flatband voltage shift due to charge trapping in this layer and to enhance charge retention, respectively.

ZrO_2 for DRAM application

Scaling trench DRAM down to the 48 nm node and below, MIM capacitors with an EOT of lower than 2 nm are envisaged [1]. But, to fulfil the stringent requirements on leakage current density which has to be lower than $1 \cdot 10^{-8}$ A/cm^2 at 1 V, amorphous HfO_2 or ZrO_2 show no high enough k-values [56]. At standard pressure, both HfO_2 and ZrO_2 can crystallize into three different phases which are the cubic, the tetragonal, and the monoclinic phase. A full crystallization into the tetragonal phase shows the highest dielectric constant of about 39 for the ZrO_2 [57]. Even though, the monoclinic phase is the most stable, the tetragonal phase can be tuned by temperature, film thickness, or doping (e.g., promising elements are Si, Al, etc). This is schematically illustrated in Fig. 10 [29]. Even, if the bandgap of ZrO_2 is about 0.5 eV smaller than that of HfO_2, ZrO_2 exhibits a 100 °C lower crystallization temperature and an about 20 % higher dielectric constant [56]. The critical thickness defines a maximum size where the tetragonal phase is stable. With temperature the critical thickness increases, but the tetragonal phase is not quenchable (e.g., during cooling it converts back to monoclinic phase). Another way to increase critical film thickness is doping and, furthermore, thinner films need less doping.

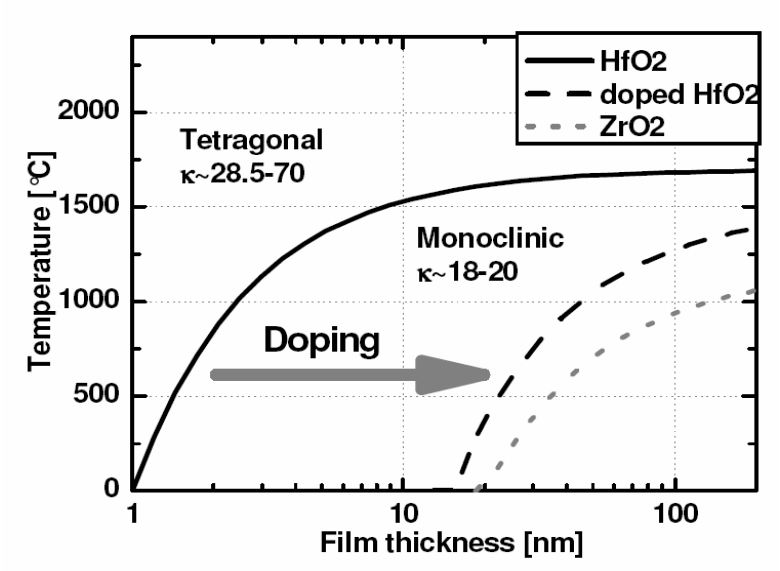

Fig. 10: Temperature and thickness dependence of phases in HfO_2 and ZrO_2, indicating schematically the effect of doping.

In the following part, ZrO_2 as a high-k dielectric for future trench gate DRAM generation is considered. The most challenging requirement on the dielectric is a thermal stability up to 1000 °C by preserving the specification of leakage current density. 5 nm ZrO_2 films on p-type silicon samples were deposited via ALD from TEMAZr and O3 as precursors [56]. Post deposition anneals in N_2 and NH_3 were performed at temperatures from 400 °C to 1000 °C. The thickness dependence on annealing temperature was measured with spectral-ellipsometry and X-ray reflectometry. For temperatures up to 400 °C no crystallization was seen, for temperatures between 400 °C and 800 °C the thickness of the layers shrinks significantly due to densification effects which leads to lower EOT values, and for temperatures higher than 800°C intensive interface growth takes place revealing an increase in physical thickness and therefore in EOT. X-ray diffraction indicates that the ZrO_2 is crystallized in the high-k cubic/tetragonal phase. The surface roughness was analyzed by atomic force microscopy (AFM) and transmission electron microscopy (TEM). The surface shows a very low roughness for annealing temperatures up to 800 °C, even after crystallization. But, there is a significant increase in roughness for higher annealing temperatures. In Fig. 11, the capacitance equivalent oxide (CET) thickness in dependence on the leakage current for at different temperatures and times annealed samples are shown. As already mentioned above, for annealing up to 400 °C no shrinking in CET can be seen, but a significant decrease in leakage current density is revealed which may be due to reorganization effects in the dielectric layer. A further raise in annealing temperature leads to a decrease in CET due to crystallization whereas the leakage current density remains constant. An increase in the annealing temperature beyond 700 °C results in an IL growth and in a significant increase in leakage current density. Annealing in N_2 is much more beneficial regarding leakage current density than in NH_3. In summary the phase of the film, the IL growth, and the thermal stability are the key points characterizing the electrical properties of thin ZrO_2 films.

Summary and perspectives

In nearly all sectors of microelectronics high-k oxides have to be introduced to fulfil the specifications of future technology generations. For several sectors high-k oxides are already introduced, for others they are shortly before implementation. But this is only the very beginning.

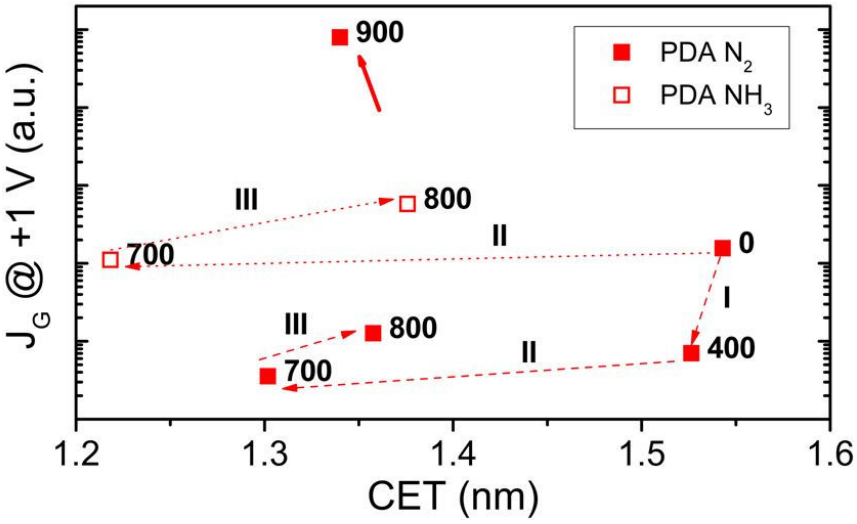

Fig. 11: Leakage current densities in dependency on CET with annealing temperature and atmosphere as parameter.

The available high-k oxides are only applicable for the current or next technology node. In the future, significant improvements have to be done to meet the stringent demands of subsequent technology generations. A very promising but challenging field for improvements of high-k oxides is using more "exotic" metals or doping the current high-k oxides with those "exotic" materials. It was shown that doping can influence crystallization (e.g., leakage current densities, soft phonon scattering), interface reaction (e.g., mobility degradation, threshold voltage shift), and trapping properties (e.g., reducing oxygen vacancies) and therefore electrical stability and reliability. The deposition method for high-k oxides will be ALD. With ALD lower deposition temperatures are possible, above all if Plasma ALD is used, the layer by layer growth enables more precise doping, and for 3D-structures with high aspect ratios, ALD is the only applicable deposition technology. Furthermore, high-k oxides are conceivable only together with metal electrodes. Metal electrodes guarantee less interface reaction, lower CET, and better adjustment of the work function difference. But, as for high-k oxides, for metal electrodes further big efforts have to be undertaken for implementation.

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