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Effect of Source and Drain Contacts Schottky Barrier on 3C-SiC Nanowire FETs I-V Characteristics

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Abstract. In this work, SiC nanowire (NW) FETs are prepared and their electrical measurements are presented. From the samples fabricated on the same substrate, various I-Vs shapes are obtained (linear, non linear symmetric, and asymmetric). With the assistance of simulation, we show that this is a result of different values of Schottky Barrier Heights (SBH) at Source (S) / Drain (D) contacts of FETs. An origin for this might be a non uniformity in annealing, NW doping level and high interface traps density (that pins the Fermi level) as well as the high sensitivity of the metal-NW contacts to local surface contaminations.

Introduction

The majority of the research groups working on NW FETs use metals as S / D areas and they are trying to lower the rectifying SB [1] or even transform them to completely ohmic [2] by proper annealing step. In the first work on SiC NW FETs [2], the researchers used low work-function metal (Ti) in contact with highly n-type doped nanowire and so the initial SB was easily suppressed after the annealing leading to ohmic contacts (linear I-V for low V_d). In contrast in [1], a high work-function metal (Au) was used so the SB of the contacts was not suppressed completely after the annealing step and a non linear shape of I-Vs was obvious. Anyhow, forming SB instead of ohmic contacts might have interesting applications in nanoelectronics. In standard CMOS technology, SB-MOSFETs have recently attracted a renewed interest as an alternative to conventional MOSFETs with doped S and D contacts [3,4]. SB-MOSFET devices with metal as S and D replace S/D impurity doping with metal parts. This is due to the fact that in the near future the continued downscaling of transistor dimensions calls for highly conductive source and drain electrodes otherwise the current through the device will be limited by the contacts. There are numerous motivations for replacing doping with metal in the S/D regions, including low parasitic S/D resistance, low-temperature processing for S/D formation and inherent physical scalability which is due to the low resistance of metal and the atomically abrupt junctions formed at the metal–semiconductor interface. This picture is more stressed in the case of NW FETs due to the 1D nature of the semiconductor.

In the present work, SiC NW FETs are prepared and their electrical measurements are presented. From the samples synthesized on the same substrate using the same metal contacts and device process steps, various I-Vs characteristics shapes are obtained (linear, non linear symmetric and asymmetric). With the assistance of simulation, we show that this is a result of different values of SB heights at S/D contacts.

Experimental results

SiC NWs were grown by using a Hot-Wall Chemical Vapor Deposition (HW-CVD) system with a methyltrichlorosilane (MTS, CH_3SiCl_3) source precursor (see more detailed information about the synthesis and materials characteristics of cubic SiC NW in [2]). The SiC NWs had diameter less than 100nm and lengths of several microns. As-synthesized SiC NWs were prepared on a highly doped silicon wafer covered with a 500 nm-thick thermal SiO_2 layer on top. The highly doped ($>10^{20}$ cm^{-3}) n^+ Si wafer was served as a back gate electrode in three-probe FET structures. Prior to the metal deposition (Ti/Au=50/150 nm) by electron-beam evaporation, the substrate was pre-patterned and the SiO_2 was removed from the ohmic contact areas by dipping in buffered hydrofluoric acid (BHF) for 30 seconds. Then, source and drain electrodes (Ti/Au) were defined by standard e-beam lithography and lift-off process. Fig. 1 shows a schematic view of the single SiC NW FET prepared on the SiO_2/n-Si wafer in three-probe FET configuration and Fig.2 shows a SEM image of the device. The I-V characteristics of three NWFETs of the same sample are shown in Fig.3. As it is obvious from the linearity of the I-V device 1 has ohmic contacts while devices 2 and 3 have non linear I-Vs. As depicted below from simulation results, the different SBs of S/D lead to these non linear I-V characteristics.

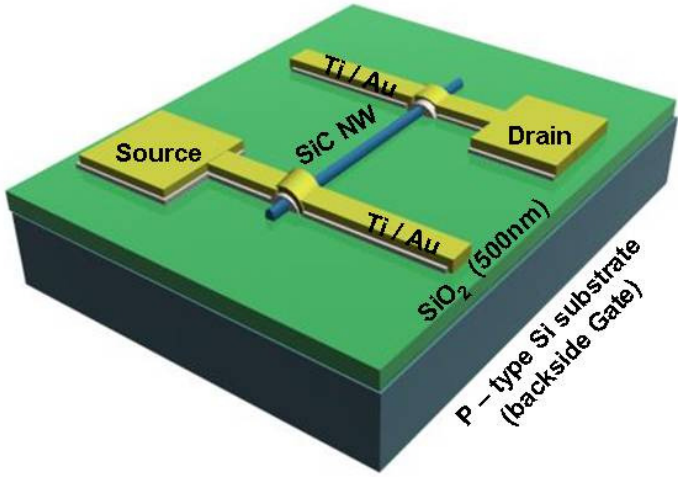

Fig. 1 Schematic view of SiC NWFET

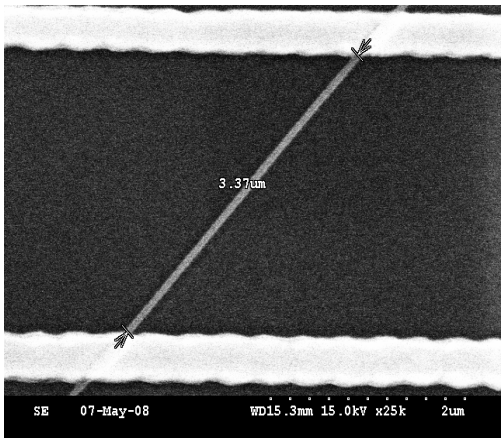

Fig. 2. Scanning Electron Microscope view of one of the SiC NWFETs

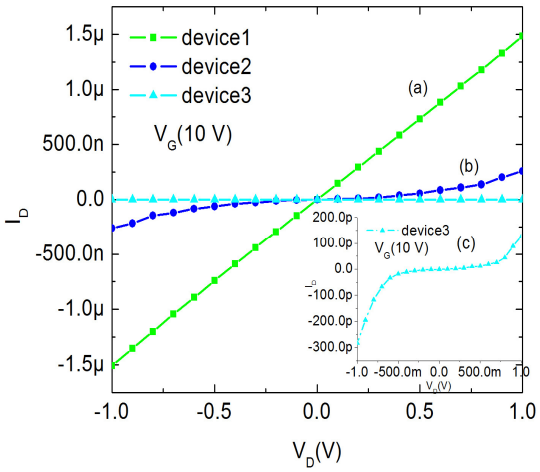

Fig. 3. Experimental I-Vs from various NWFETs of the same sample; inset: zoom for device

Simulation results

A commercial simulation tool [5] is used which solves the Boltzmann transport equation within the drift-diffusion approximation with the Poisson equation. Indeed at the micrometer scale the drift-diffusion model used in SILVACO is a well adapted tool to describe electronic transport in semiconductor devices operating within a diffusive transport regime and far away from the strong quantum regime (>10 nm) [6]. Using the same method with [6], we tried to simulate the non-linear I-Vs of the experimental devices. The simulated device has exact the same dimensions and geometry with the experiment one. By using ohmic or Schottky contacts (with a non-zero SB), we simulate the experimental behavior. As shown in Fig. 4, by applying non-zero and not equal SBs at the S/D contacts has as result the non linear I-V shape (Fig. 4 curve b). When ohmic contacts are considered at the same device, Fig. 4 curve (a), then a linear I-V is obtained. At this point we have to note down that in the case of small difference between source and drain SBs, as in case of curve (b) of Fig. 4, the accurately fitting of the experimental results with Silvaco software is not possible. When ohmic contacts are considered [6] like curve (a) of Fig.4, and when the SB difference is quite big like in [7], then accurate fitting with the experimental results is achievable.

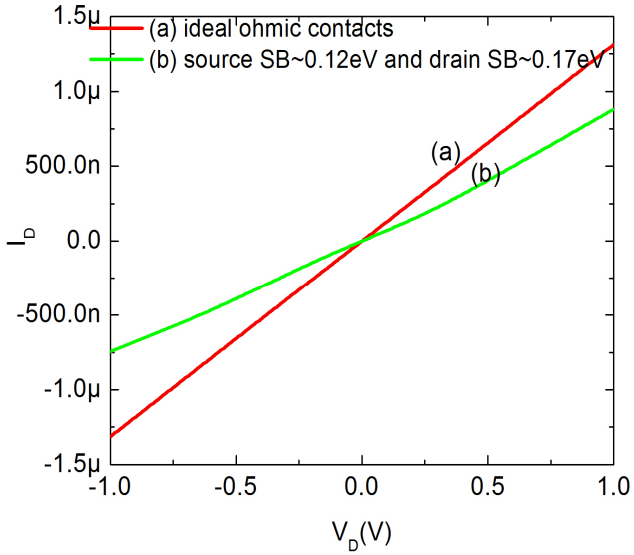

Fig. 4. Simulated I-Vs for (a) ohmic and (b) Schottky source and drain contacts with small difference in barrier heights.

Discussion and conclusions

A qualitative analysis of S/D contacts SBs effect on the SiC NWFETs I-V characteristics is presented. Even at the same wafer with many 3C-SiC NWFETs, various I-Vs shapes are obtained (linear, non linear symmetric and asymmetric). According to simulation results, this behavior is due to different (non zero) SB at S and D contacts. The fact that the devices belong to the same wafer exclude all the other reasons such as different metal material or different fabrication process to explain this different behavior. A non uniformity in annealing, NW doping level [8,9] and high interface traps density (that pins the Fermi level) as well as the high sensitivity of the metal-NW contact to local surface contaminations [10-13] might explain the different SBs between S and D. In [11-13] the researchers noticed a similar behavior with non linear I-Vs of Carbon Nanotube (CNT) FETs. Lu *et al.* [12] used intentionally a chemical in the process of one of the two metal contacts surface of a CNTFET and they noted asymmetric I-Vs due to the different SB of S and D. Moreover, they presented some ab initio calculations and they showed the increased sensitivity of the metal work-function to these chemicals. Kim *et al.* [13] showed that remaining from the PMMA (due to imperfect development) during the lift off process step might have an impact to the SB of the contacts. More specialized experiments should be performed in order to identify the origin of

these different contacts SBs of the same device. If not, a bottleneck in the mass production of nanowire FET devices will be present.

Acknowledgements

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