

## Influence of Negative Charging on High Rate SiC Etching for GaN HEMT MMICs

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**Abstract.** We discuss the influence of negative charging on high-rate ICP etching of SiC via-holes for GaN HEMT MMICs. There is large differential etching behavior such as etch rate, etching profile, and RIE lag between S.I.- and n-SiC substrates because of the difference in wafer heating and negative charging of the sidewall during etching between both substrates. We analyze the difference in negative charging between both substrates by simulating the etching profile.

### Introduction

SiC backside via-holes are a key technology for millimeter-wave GaN HEMT MMICs to reduce source inductance, as shown in Fig. 1. However, the SiC etch rate for inductively coupled plasma (ICP) etching is normally 1  $\mu\text{m}/\text{min}$  or less due to the strong silicon-carbon bond. Recently we have reported several technical issues such as pillar formation associated with micropipes [1] and differential etching behavior between semi-insulating (S.I.) and n-doped SiC [2] regarding ICP etching at a high rate in the order of around 2  $\mu\text{m}/\text{min}$ , higher than any rate ever reported. Furthermore, we have developed a 3-inch SiC backside via-hole process for GaN HEMT MMICs using high-rate ICP etching at 2  $\mu\text{m}/\text{min}$  [3]. In addition, we have demonstrated an X-band hybrid power amplifier IC [4] and W-band transceivers [5] by using this SiC via-hole technology. In this study, we investigate the influence of negative charging on high-rate SiC etching for GaN HEMT MMICs.

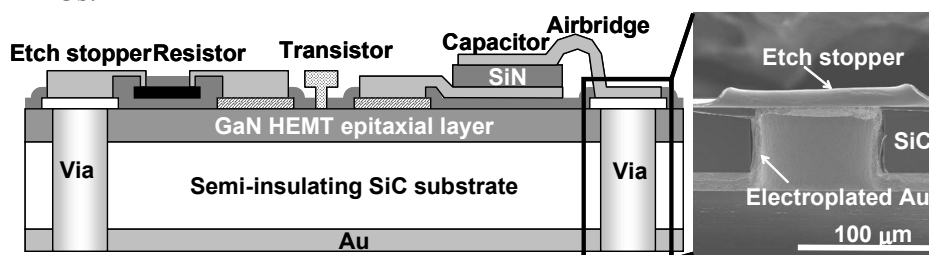


Fig.1. Schematic GaN HEMT MMICs with SiC via-hole (photograph).

### Experimental

We used S.I.- and n-type 4H-SiC (0001) substrates and their resistivities were 0.1  $\text{M}\Omega\text{cm}$  and 0.125  $\Omega\text{cm}$ , respectively. An electroplated Ni metal mask with openings of a 50-150  $\mu\text{m}$  diameter circle and a 10-150  $\mu\text{m}$  width line was fabricated on the SiC substrates. Etch experiments were performed by using an ICP system in which RF (13.56 MHz) power was supplied to the ICP coil and platen. The flow rates of  $\text{SF}_6$  and  $\text{O}_2$  were fixed at 200 and 50 sccm, respectively. The operating pressure was 5 Pa. Samples were bonded onto the carrier using a high-temperature-resistant thermoplastic adhesive. The backside of the carrier was cooled with helium. Etched samples were evaluated using a scanning electron microscope (SEM) and confocal laser scanning microscope (CLSM).

### Results and discussion

First, we investigated the etching characteristics of S.I.- and n-SiC substrates under various etching conditions. Figure 2 shows cross-sectional SEM images of typical 150  $\mu\text{m}$ -diameter via-holes of both

substrates etched under a coil and platen power of 2 and 0.3 kW, respectively. For both substrates, the anisotropic etching profile was obtained without an undercut against a metal mask, and the sidewalls had a retrograde profile and were undulated. Furthermore, it was found that the etched bottom of S.I.-SiC became much rounder compared with n-SiC. The height difference in S.I.-SiC between the center and edge of the via-hole bottom was approximately 10  $\mu\text{m}$ . Therefore, when etching via-holes of GaN HEMT/S.I.-SiC MMIC, the GaN surface appeared first in the center of the via-hole bottom as shown in Fig. 3. Then, the thickness of the GaN HEMT layer was about 1  $\mu\text{m}$ . Since the etch selectivity for GaN is 30 to 50, the punch-through in the GaN HEMT layer was not observed until SiC on the edge of via-hole bottom was completely etched. However, thinner GaN thickness may lead to a punch-through in the center. Therefore, it is desirable that the via-hole bottom is flat. Figure 4 shows the platen power dependence of the etch rate (a) and sidewall angle (b) for both substrates at a coil power of 2 kW. Then, the via-hole diameter was 150  $\mu\text{m}$ . With both substrates, as the platen power increased, the etch rate increased as a matter of course. However, the etch rates of S.I.-SiC were clearly lower than those of n-SiC. Furthermore, the sidewall angles of S.I.-SiC were larger than those of n-SiC. This is also undesirable when considering metallization.

Next, the RIE lag difference between both substrates was investigated using CLSM. Figure 5 shows the via-hole diameter dependence of the normalized etch depth in both substrates. The normalized etch depth is defined as the ratio of etch depth to that of the 150- $\mu\text{m}$  diameter hole. As a result, S.I.-SiC had a more significant RIE lag compared to n-SiC. Thus, the via-hole diameter must be unified in a GaN HEMT MMICs wafer to obtain a high yield of via-hole fabrication.

According to our previous work [2], this differential etching behavior is attributed to the difference in wafer heating and negative charging of the sidewall during plasma etching between both substrates. In n-SiC, the wafer temperature during etching became higher compared to S.I.-SiC because of a higher free-carrier absorption coefficient. Therefore, the etch rate of chemical reaction was enhanced in n-SiC. On the other hand, the negative charging in S.I.-SiC is larger compared to n-SiC due to the low electrical conductivity. Therefore, in S.I.-SiC, many positive ions are steered toward the sidewall, so the amount of vertically-incident ions decreases more significantly by reducing the via-hole diameter, resulting in a greater RIE lag compared to n-SiC.

To understand the difference in negative charging between S.I.- and n-SiC substrates, we

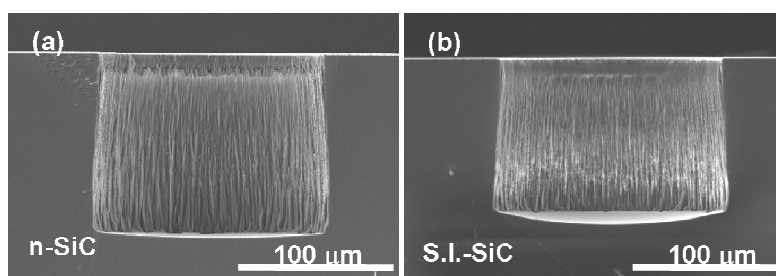


Fig.2. Cross-sectional SEM images of 150  $\mu\text{m}$ -diameter via-holes: (a) n-SiC and (b) S.I.-SiC.

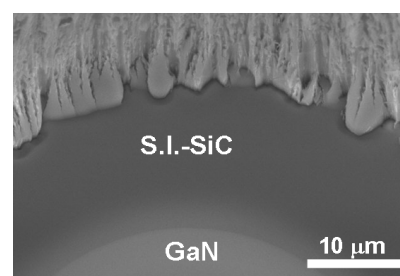


Fig.3. SEM image of via-hole bottom for GaN HEMT/S.I.-SiC.

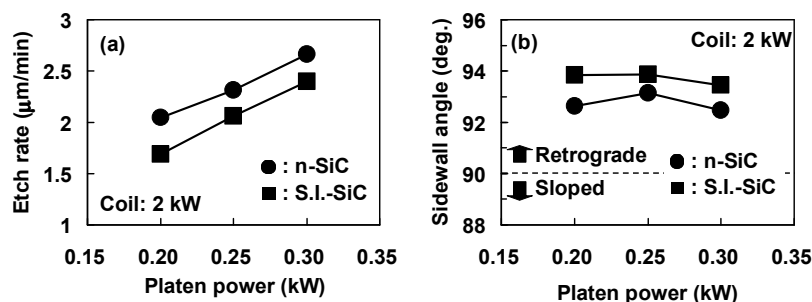


Fig.4. Platen power dependence of etching characteristics for n-SiC and S.I.-SiC: (a) etch rate and (b) sidewall angle.

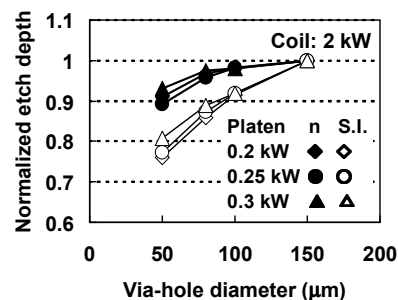


Fig.5. Via-hole diameter dependence of normalized etch depth in both substrates.

simulated the etching profile using the Monte Carlo method. Many researchers [6-10] have already reported precise plasma etching profile simulations including particle transport, kinetic energy, surface reaction, and polymer deposition. However, for simplicity, we took into account particle (positive ions and radicals/neutrals) transport only.

Figure 6 shows a schematic etching simulation model. First, we assumed that positive ions within the sheath are not affected by the negative charge because such charge is not built up in a conductive metal mask. Then, the incident angles of ions have a Gaussian-distribution with an angular spread of  $\pm 1.5^\circ$ , which is introduced from uniformly distributed random numbers by Box-Muller transform. When positive ions pass through the metal mask, these ions are steered by the Coulomb potential of the negative charge accumulated on both sidewalls. Then, the steered angle ( $\theta$ ) of the ions was defined as

$$\theta = \arctan \left( NCR \times EC \times \left( \frac{1}{(W/2 - Xi)^2} - \frac{1}{(W/2 + Xi)^2} \right) \right), \quad (1)$$

where  $NCR$  is the negative charge build-up rate,  $W$  is the line width of metal mask,  $Xi$  is the x-axis position of the incident ion and  $EC$  is the etching cycle. Then, it is assumed that the amount of negative charge linearly increases with the etching cycle. Additionally, the deflected ions are completely reflected by the sidewall when they collide with the sidewall within  $7.5^\circ$  in the incident angle against the sidewall ( $\alpha$ ). However, it is assumed that those ions with a larger incident angle do not contribute to etching. On the other hand, radicals within the sheath have a very wide angular distribution and are not affected by the negative charging. It is assumed that only ions and radicals that attach to the bottom and the edge can contribute to etching. Etch rate ( $ER$ ) was defined as

$$ER = ER_{chem} + ER_{ion} = ER \times \eta + ER \times (1 - \eta), \quad (2)$$

where  $ER_{chem}$  is the etch rate of chemical reaction by radicals,  $ER_{ion}$  is the etch rate of ion etching, and  $\eta$  is the etch rate ratio of radicals to ions.

The etching profile is shown by string nodes as shown in Fig. 6. We calculated the amount of etching on each string node by counting the number of ions and radicals that reached the string node. The actual etching profile had no undercut against the metal mask as shown in Fig. 2 because the sidewall was passivated with the non-volatile and difficult-to-etch material of NiSiF [1]. However, because the sidewall was actually retrograde, we assumed that it was possible to move in the x-direction only in the string node on the edge. Then, the former edge node becomes the sidewall node. In this case, the densities of the generated ions and radicals were both set to 100 per  $\mu\text{m}$ .

Figure 7 shows a typical simulated etching profile at a line width of  $150 \mu\text{m}$ . Then, the charge build-up rates of n-SiC (a) and S.I.-SiC (b) were set to 0.001 and 0.1, respectively. Consequently, the

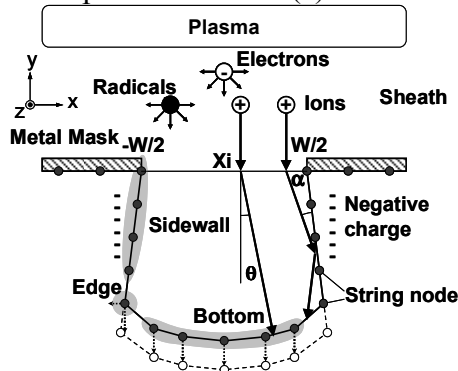


Fig.6. Schematic etching simulation model.

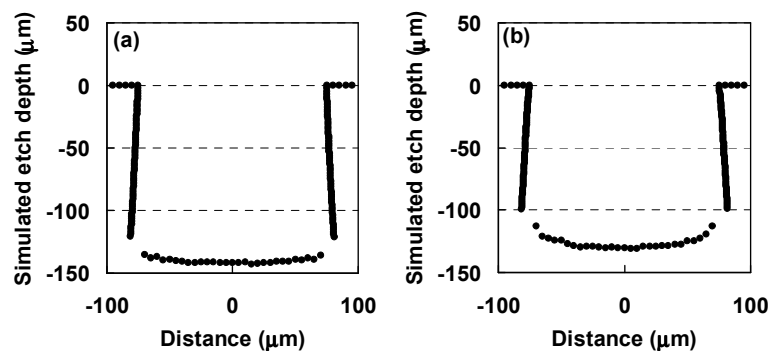


Fig.7. Simulated etching profiles of (a) n-SiC ( $ER=2.4 \mu\text{m}/\text{cycle}$ ,  $NCR=0.001$ ) and (b) S.I.-SiC ( $ER=2.2 \mu\text{m}/\text{cycle}$ ,  $NCR=0.1$ ):  $EC=60$  cycles,  $\eta = 0.15$ . Closed circles are string nodes.

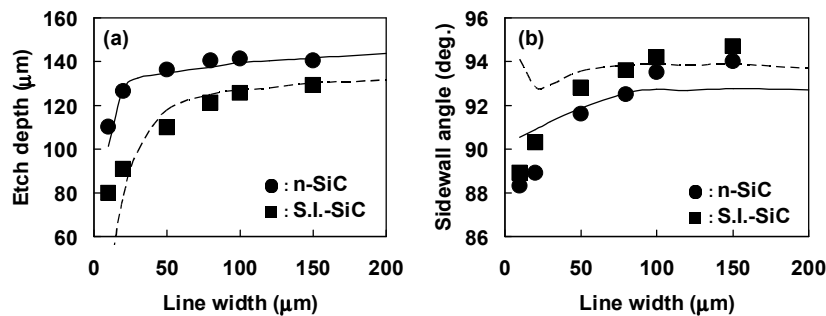


Fig.8. Line width dependence of (a) etch depth and (b) sidewall angle: experimental data of 500- $\mu\text{m}$ -length trenches etched at coil/platen power of 2/0.25 kW; n-SiC ( $\bullet$ ) and S.I.-SiC ( $\blacksquare$ ), calculated data; solid line ( $ER=2.4\text{ }\mu\text{m}/\text{cycle}$ ,  $NCR=0.001$ ) and broken line ( $ER=2.2\text{ }\mu\text{m}/\text{cycle}$ ,  $NCR=0.1$ ).

simulated etching profile of S.I.-SiC shows a larger sidewall angle and rounder bottom compared to n-SiC as well as SEM images shown in Fig. 2. Figure 8 shows the line width dependence of the etch depth (a) and sidewall angle (b). Experimental data of 500- $\mu\text{m}$ -length trenches etched at a coil and platen power of 2 and 0.25 kW were plotted. As a result, we found that the simulation result was in good agreement with the experimental data regarding the etch depth and sidewall angle. This result indicates that the amount of negative charging significantly influences high-rate SiC etching. However, S.I.-SiC is indispensable for GaN HEMT MMICs to reduce the parasitic capacitance, so it is necessary to suppress the negative charging during etching.

## Summary

We investigated the influence of negative charging on high-rate SiC etching for GaN HEMT MMICs. There was large differential etching behavior such as etch rate, etching profile, and RIE lag between S.I.- and n-SiC substrates because of the difference in wafer heating and negative charging of the sidewall during etching between both substrates. Furthermore, the difference in negative charging between both substrates was evaluated by simulating the etching profile.

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