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Forced-Air-Cooled 10 kW Three-Phase SiC Inverter with Output Power Density of more than 20 kW/L

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Abstract

A forced-air-cooled three-phase inverter built with SiC-JFETs and -SBDs as power semiconductor devices was designed and fabricated. The inverter can operate steadily at a rated power of 10 kW in a junction temperature range up to 200°C. Output power density of more than 20 kW/L was achieved. The design specifications, the power module fabrication process, the results of a high-temperature operating test and a continuous switching test are described in turn.

Introduction

There are various important requirements for SiC inverter and converter systems, including smaller size, lighter weight, greater availability, more robustness and lower cost. A promising approach that comprehensively meets all of them is to increase the output power density (OPD) of the system. In a higher OPD system, low on-resistance SiC power devices mounted on a small and simplified heatsink are operated at larger current densities and/or in extended junction temperature ranges. Recently, Kinouchi and his coworkers fabricated a 3.7 kW/400 V three-phase all SiC inverter for motor drive applications [1]. However, their system was still comparable in OPD to a state-of-the-art Si-IGBT inverter [2]. This paper describes a forced-air-cooled 10 kW/400 V three-phase SiC inverter with an OPD of more than 20 kW/L and a minimized heatsink volume [3] and capable of operating at junction temperatures ranging from room temperature to 200°C.

Configuration and Module Fabrication

Figure 1 shows a full view of our SiC inverter system for motor drive applications. Figure 2 illustrates its circuit configuration. The system is composed of 2 1 ype power modules, individually equipped with Cu heatsinks, DC-link capacitors and cooling fans, and is 500 cm^3 (15 cm × 9 cm × 3.7 cm) in volume. SiC normally-off JFETs (SJEC120R050, 1.2 kV, 30 A) and SiC SBDs (SDC30120, 1.2 kV, 30 A) from SemiSouth Laboratories, Inc. were selected as the power devices. One arm consists of two JFETs and two SBDs. A dedicated gate drive and control unit was also fabricated (not shown).

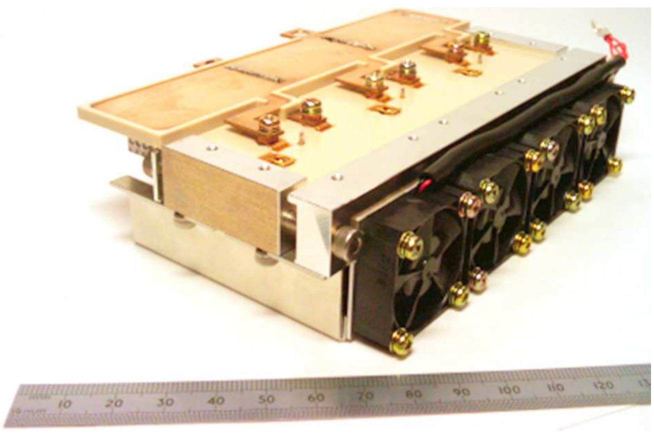


Fig. 1 Photo of 3-phase all SiC inverter.

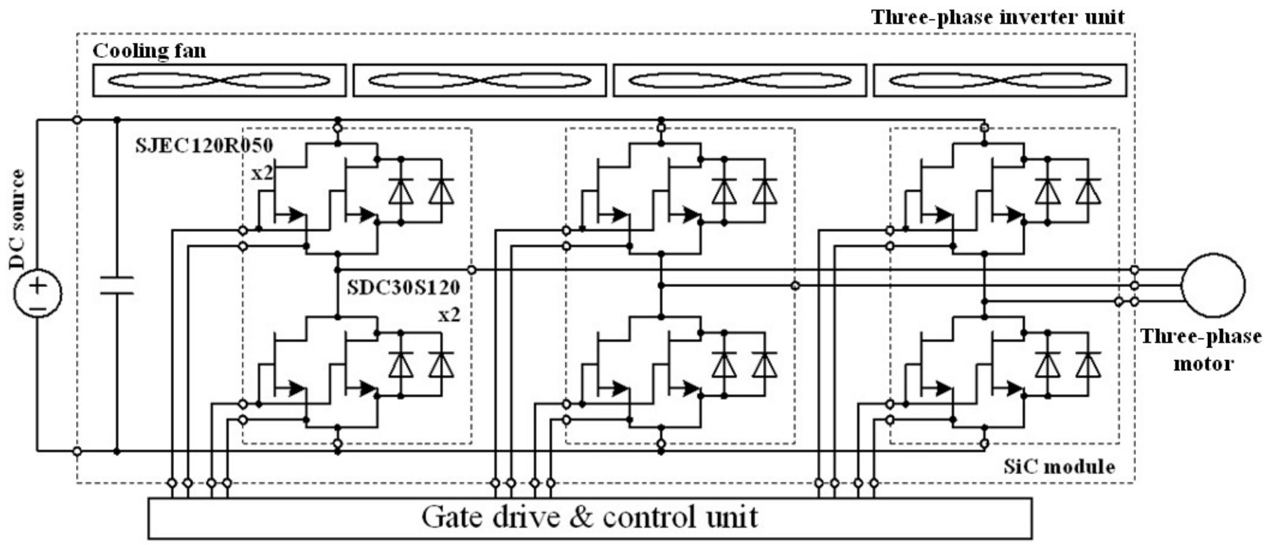


Fig. 2 Circuit configuration of three-phase all SiC inverter.

Figure 3 is a photograph of the power module. SiC devices for two arms were first soldered on Ni/Au plated Cu foils on an SiN ceramic substrate using a Au-Ge alloy (melting point = 356°C) [4], and the substrate was attached on a Cu heatsink using Au-Sn solder (melting point = 280°C). Terminal pins for control signals were also attached in this second step. A heat-resistant silicone (ADEK YX 001G) and a polypheny sulfide (PPS) resin were used as the encapsulation and housing materials, respectively.

3 y (2 arms). Four JFETs and four SBD chips are mounted on one SiN substrate.

Operating Tests

Figure 4 shows the current density distribution in two arms (a module) for the turn-on and turn-off transient. These results were calculated by using a Q3D parasitic extraction software tool. It is clear that the current through the JFETs and the SBDs ( ) adequately. It was also found that the parasitic inductance between the DC terminals was 15.3 nH per module.

Static and dynamic characterizations were carried out at module and various block levels. Typical turn-off and turn-on waveforms of the inverter at Tj = 200°C are shown in Fig. 5, where the DC-link voltage and the switching current were 600 V and 30 A, respectively. Figure 6 shows the drive circuit. To speed up the turn-on performance of the transistor, an additional circuit was used to supply a large current to the gate of the transistor in a short time at the beginning of the turn-on transient. To shorten the turn-off , 12 V

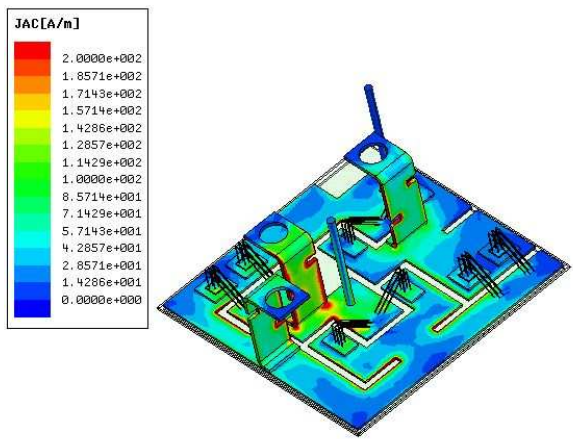
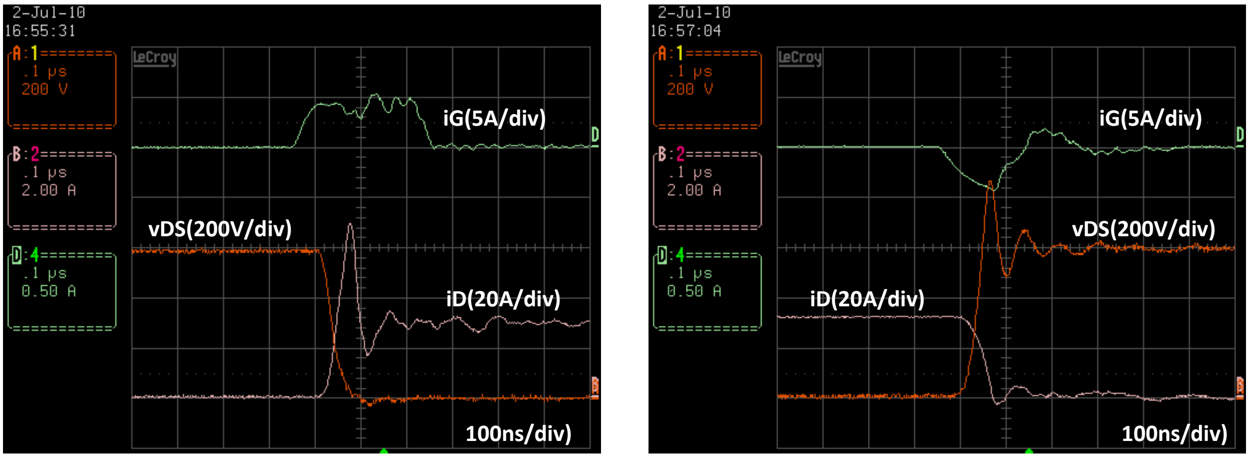


Fig. 4 Analysis results of current density distribution for the switching transient.



(a) (b)

Fig. 5 Switching behavior at 200°C for one arm of the module: (a) (b)

off transient. As a result, turn-on and turn-off times of 40 ns were achieved.

Figure 7 shows the setup of a continuous switching test using two power modules. The equivalent circuit is presented in Fig. 8. The active switching blocks, Q1 and Q4, were operated by the 90-degree phase difference. The load current i_L was kept constant by feedback control. The voltage (v_{DS}) and current (i_D) waveforms in Q1 are shown in Fig. 9. It is clear from these waveforms

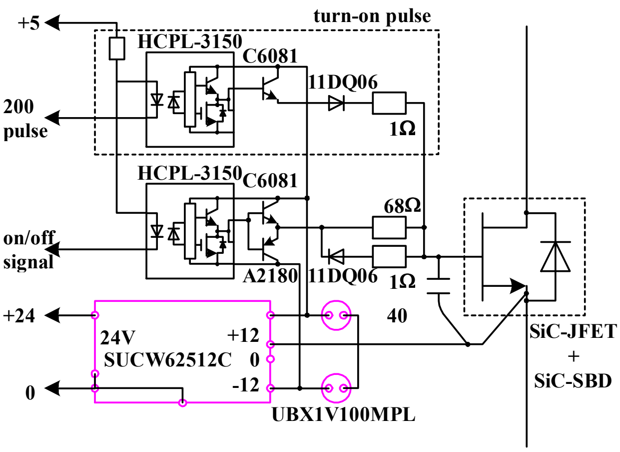


Fig. 6 Gate drive circuit with speed-up options used for measurement of the module in Fig. 3.

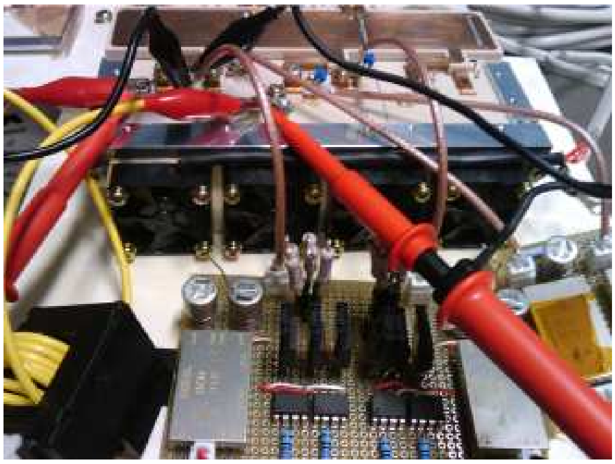


Fig. 7 Setup of the continuous switching test using two power modules.

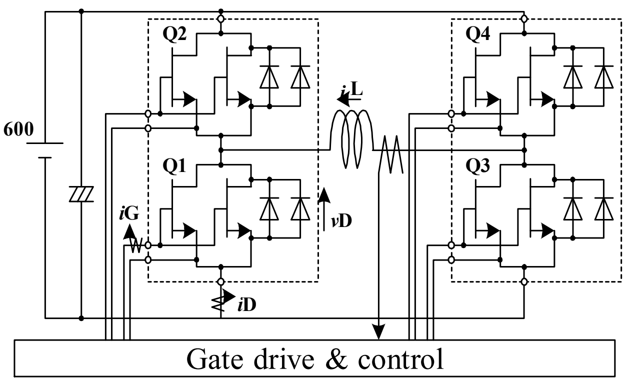


Fig. 8 Circuit configuration of setup in Fig. 7.

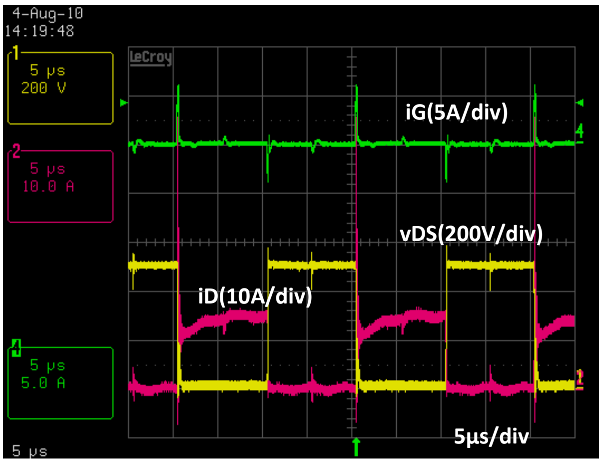


Fig. 9 Switching waveforms of setup in Fig. 7.

that these test conditions induced the same level of switching stress as a 10 kW load condition in the three-phase inverter system. The cooling fin temperature was 100°C under the conditions of a 50 kHz switching frequency, 25°C ambient temperature and no forced air cooling. With forced air cooling using the fans shown in Fig. 1, the cooling fin temperature was 55°C. The wind speed was 3 m/s, which was measured with a hot wire anemometer at the outlet. These results suggest that higher output power is attainable.

Figure 10 shows the waveforms of the output load current and the voltage across the active switching device under inverter operating conditions of a 50 kHz switching frequency and dead time of 0.75 μs. The waveforms indicate that our inverter produces a fairly good sinusoidal wave.

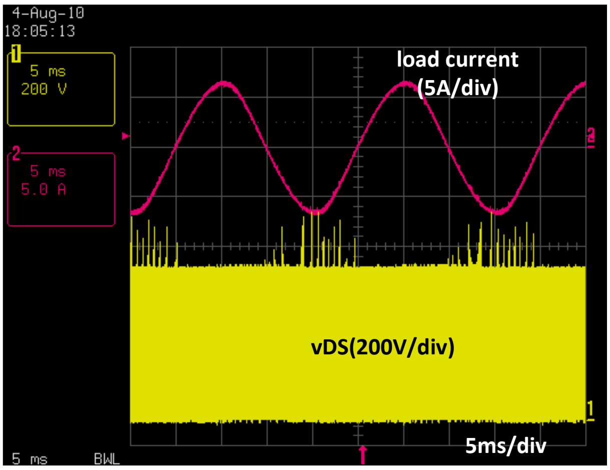


Fig. 10 Waveforms of the output load current and the voltage across the active switching device under inverter operating conditions.

Summary

A forced-air-cooled 10 kW three-phase inverter prot ype, including three 2 1 ty power modules, was designed and fabricated. SiC modules, Cu heatsinks, k cooling fans were enclosed in a volume of 500 cm^3. An output power density of more than 20 kW/L was successfully achieved. The system can operate stably at the rated power without any problem in a junction temperature range up to 200°C. Regulated sinusoidal wave output power was stably observed for the single-phase full bridge circuit configuration. The parasitic inductance between the DC terminals was estimated to be 15.3 nH per module. More detailed characterization is now in progress. New results will be reported elsewhere in the near future.

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