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A compact 5-nH one-phase-leg SiC power module for a 600V-60A-40W/cc inverter

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Abstract

We have developed a small-volume, high-power-output inverter with a high output power density using SiC power devices. To fully utilize the advantages of SiC power devices, it is necessary to reduce the inductance of the power module. This is done by using a double-layer ceramic substrate, attaining a low inductance of 5 nH. A double pulse test was carried out up to 60 A under a DC voltage of 600 V. The low inductance greatly reduced the surge voltage and the oscillation at the switching transient. The SiC inverter unit with a volume of 250 cc was assembled using three power modules. The cooling performance of the inverter unit was evaluated at a loss equivalent to an output power of 10 kW, and it was found that the inverter unit can output 10 kW at a junction temperature (Tj) of about 200 ºC.

Introduction

We have been developing a 600V-60A 3-phase inverter with a high output power density of 40 W/cc using SiC power devices [1]. This requires a high Tj drive capability and low power device switching losses [2-4]. Low parasitic inductance is needed to attain low-loss switching because parasitic inductance causes various problems such as surge voltage and oscillations [4]. A one-phase-leg power module with low parasitic inductance has been developed to avoid such problems. This module has a compact size of 20 cc, including an air-cooled heatsink, and can operate at Tj higher than 200 ºC. This paper describes: (1) the reduction of parasitic inductance in the module and (2) the cooling performance.

All-SiC power module with double-layer ceramic substrate

Figure 1 shows a photograph of a one-phase-leg SiC power module, and Fig. 2a shows the circuit configuration. Two SiC-JFETs (SXEC120R025, normally-off) and two SiC-SBDs (SDC30S120) (SemiSouth Laboratories, Inc.) are used for each arm. Capacitors were installed between gates and sources to prevent false turn-on of the JFETs [5]. A double-layer ceramic (Figs. 2b and 2c, Kyocera Co., Ltd.) is used for the substrate, consisting of three metal sheets (Cu) and two ceramic sheets (SiN). Parasitic inductance between terminals D1 and S2 during the switching transient is closely related to the area of the main current loop in the module. As shown in Fig. 2(b), the source of the low-side JFETs is connected to the top Cu sheet S2' by Al wires. S2' is connected to the mid-layer Cu sheet via through holes, and the sheet is connected to S2 via another through hole. Therefore, the main current loop has a much smaller area than a conventional single-layer structure. At the switching transient, the main current flows as indicated by the arrows in Fig. 2c. This small current loop greatly reduces parasitic inductance through terminal D1 to S2; the inductance was

estimated to be 4.5 nH by 3D electromagnetic simulation. The drawback about using a double-layer ceramic substrate is a potential increase in heat resistance, but the effect is negligible in a high Tj drive system with forced air cooling because the heat resistance of the heatsink accounts for most of the overall heat resistance and the contribution of the substrate resistance is very small. The ceramic substrate is directly joined to the Cu heatsink in order to reduce the size. To achieve high Tj operation exceeding 200 ºC, the materials were carefully selected.

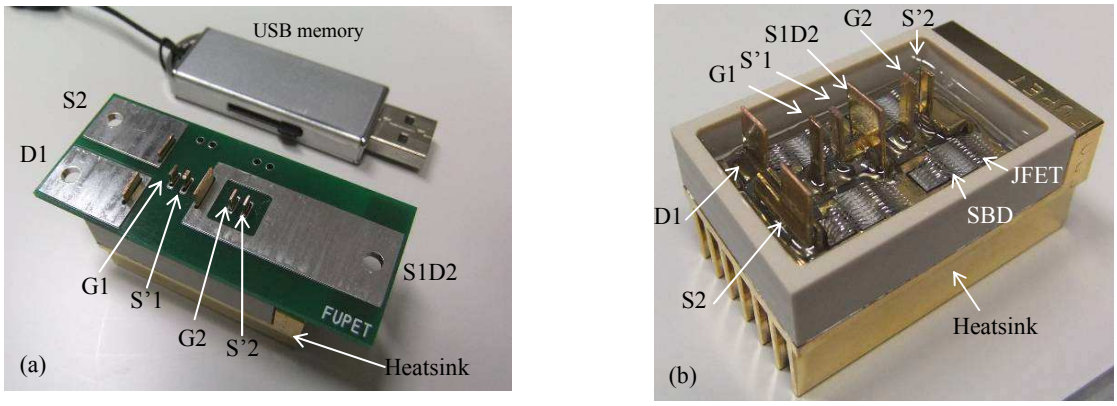


Fig. 1 Photographs of the power module: (a) outside view and (b) inside view.

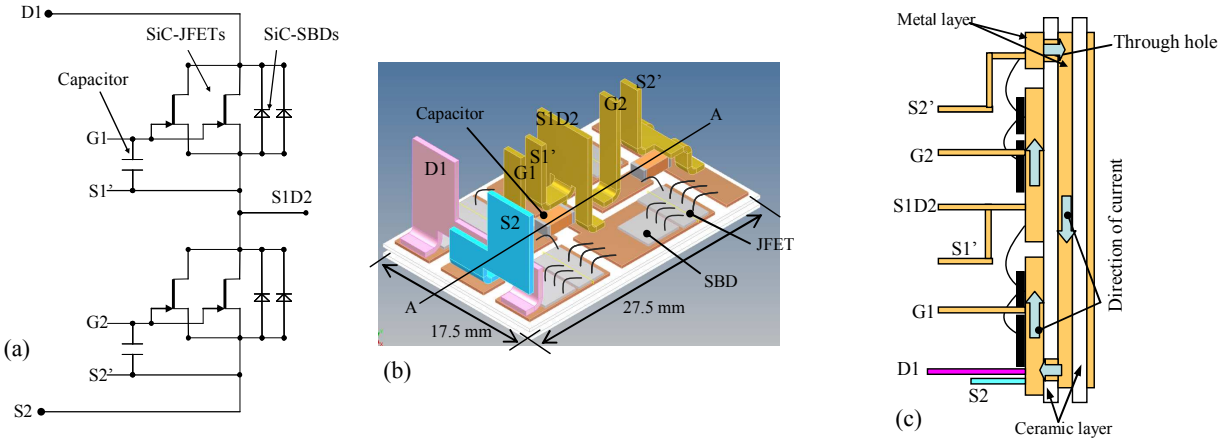


Fig. 2 Internal structure of the module:
(a) circuit configuration, (b) 3D view and (c) section A-A.

Electrical evaluation

A double pulse test was carried out under a DC voltage of 600 V [5]. A snubber capacitor (Murata, 300 nF, 1 kV) was mounted between terminals D1 and S2. Figure 3 shows the turn-off, turn-on transient (JFET) and reverse recovery waveform (SBD) at a drain current of 60 A. The black lines of V_{DS} in Fig. 3 are the voltage waveforms obtained with a current transformer (CT) probe and the red lines are the waveforms without the CT probe. The red lines clearly show very low surge and very small oscillation, indicating that the module has a fairly small inductance. We attempted to evaluate the parasitic inductance through terminal D1 to S2 based on the current and voltage waveforms. However, a CT probe must be used to measure the current, and the wiring must be extended to connect a CT probe. This increased the inductance and caused spurious oscillation, as indicated by the V_{DS} black lines. Another evaluation method was therefore used in which inductance was determined only from the voltage waveform (red line), and was calculated by:

$$\int \Delta V dt = L I_D, \quad (1)$$

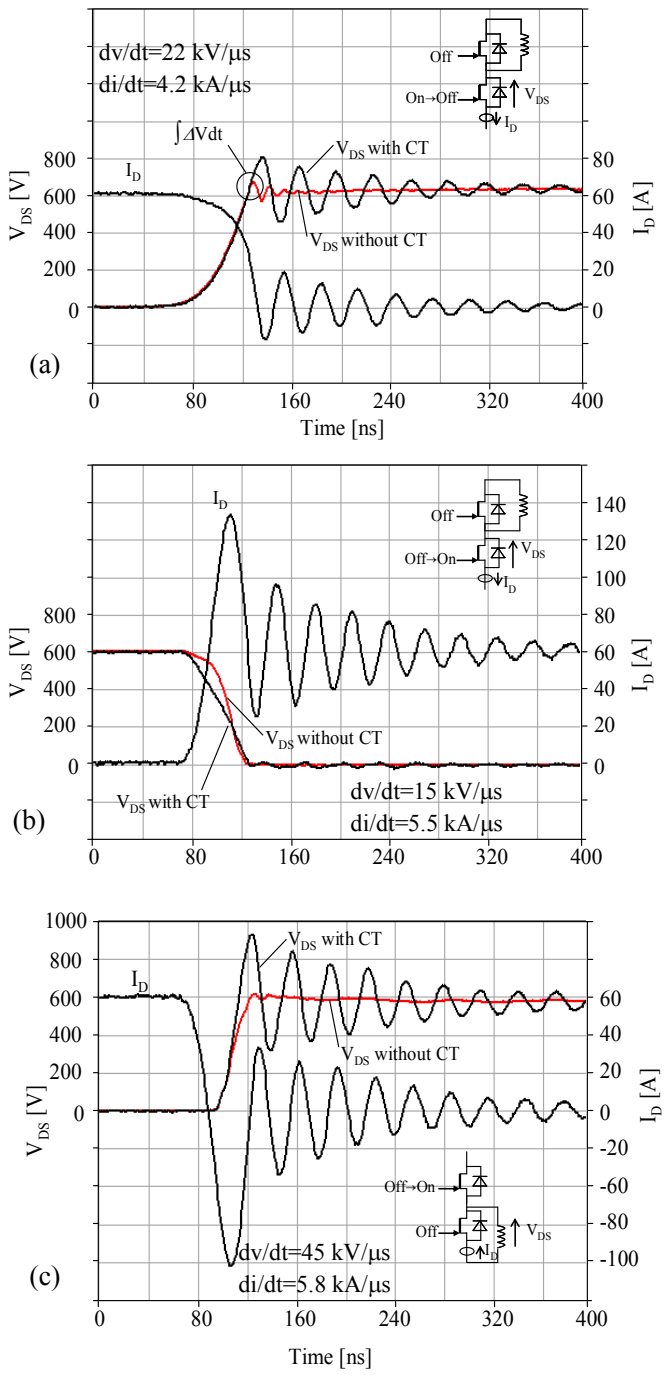


Fig. 3 Results of double pulse test at I_D = 60 A under a DC voltage of 600 V: (a) turn-off transient waveform (JFET), (b) turn-on transient waveform (JFET) and (c) reverse recovery transient waveform (SBD).

Table 1 Inductance measurements

Method	Components	L
Electromagnetic simulation	Module	4.5 [nH]
Impedance analyzer	Module	5.5 [nH]
	Snubber capacitor	3.7 [nH]
Double pulse test	Module + Snubber capacitor	9.3 [nH]

where $\int\Delta$Vdt is obtained by integrating the area of the first surge voltage waveform over the line of 600 V, as shown in the circled area in Fig. 3a, L is the synthetic inductance of the module and the snubber capacitor, and I_D is the current flowing through the SiC chips. Figure 4 plots $\int\Delta$Vdt obtained by varying I_D from 20 to 60A where the slope in the $\int\Delta$Vdt-I_D relationship corresponds to the inductance L. Thus, the inductance L is estimated to be 9.3 nH. The static inductances were also measured by using an impedance analyzer. However, since the inductance of the probe causes a significant error when L is several nH, accurate measurement is difficult. Therefore, the static inductance is for reference only. Table 1 shows the inductances obtained by simulation, double pulse test and impedance analyzer. Judging from each evaluation result, the module inductance is estimated to be about 5 nH.

Thermal evaluation of the inverter

The three-phase SiC inverter unit was assembled as shown in Fig. 5. This inverter unit was designed to attain an output power density of 40 W/cc, and its specifications were as shown in Table 2. The body of the inverter unit consists of three power modules with heatsink, cooling fan, DC linked capacitors and the case. The inverter unit is designed so that Tj is 200 ºC when the output is 10 kW and ambient temperature is 25 ºC. The fans are chosen to make the air flow between the fins of the heatsink 2 m/s. Measured and simulated temperatures of the heatsink versus heat loss from the unit are indicated by dotted and dashed lines in Fig. 6, respectively. The measured and simulated heat resistances are 0.91 ºC/W and 0.90 ºC/W, respectively, showing an error of less than 1%. Using the same simulator, the heat resistance between the chip and heatsink can be calculated as 0.05 ºC/W. Therefore, Tj can be estimated as the solid line in the figure, which is approximately 10 ºC higher than that of the heatsink. Based on these estimations, the heat loss will become approximately 180 W when the inverter unit output is 10 kW, yielding an efficiency of 98.2%. Therefore, the unit can output 10 kW power with Tj of 200 ºC.

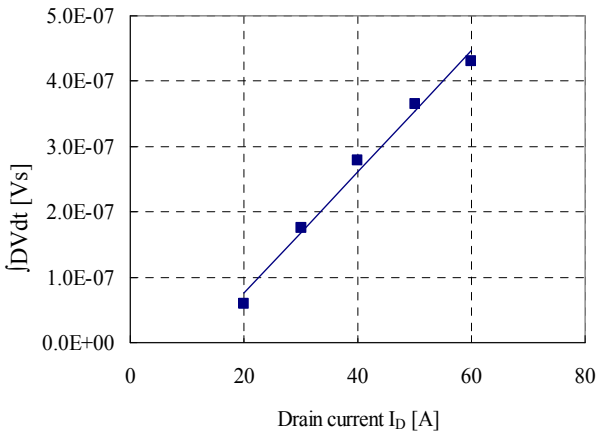
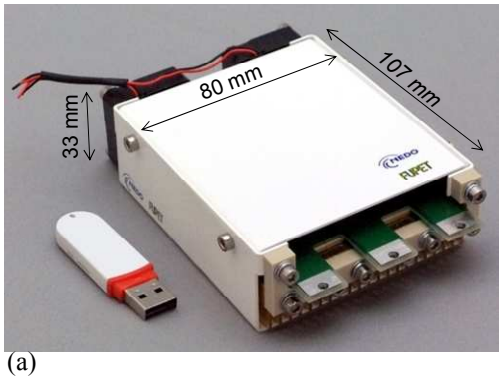
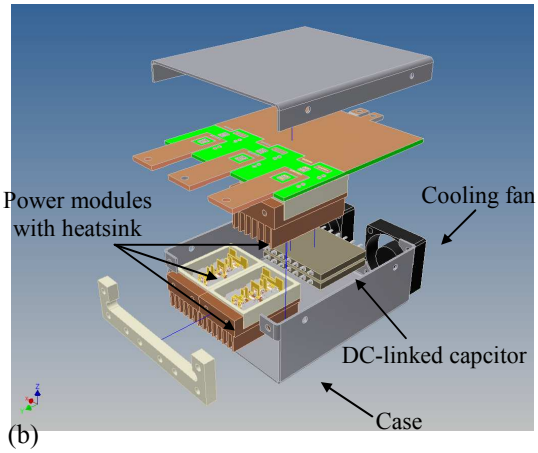


Fig. 4 Relationship of $\int \Delta V dt = LI_D$ from I_D = 20 to 60 A.



(a)



(b)

Fig. 5 Assembled inverter:
(a) photograph and (b) exploded view.

Table 2 Specifications of the inverter

Input	DC600 V
Output	3ϕ -400 V, 10 kW
Size	107 x 80x 33 ≈ 250 cc
Power density	40 W/cc
Switching frequency	Up to 50 kHz

Summary

We achieved a power module with a low inductance of 5 nH by using a double-layer ceramic substrate. The surge voltage and oscillation were markedly reduced at the switching transient. A three-phase inverter unit with a 10 kW rating and 250 cc in volume was assembled. The results of thermal radiation tests suggested that our inverter unit can work at Tj of about 200 ºC, with an output power density of 40 W/cc.

Acknowledgement

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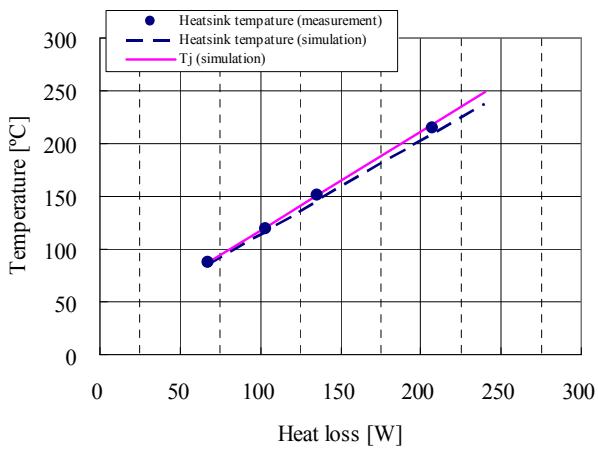

Fig. 6 Measured and simulated temperatures of heatsink versus heat loss