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Power module package structure capable of surviving greater ΔTj thermal cycles

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Abstract. A new SiC power module package structure is proposed that is capable of withstanding greater ΔTj cycle stress. Its most notable feature is the use of a SiN substrate having Cu/Invar/Cu foils (C/I/C thickness ratio of 1/8/1) brazed on both sides as conductor plates. The CIC foils show a very low coefficient of thermal expansion (CTE) of 5.1 ppm/°C and therefore can significantly reduce package degradation resulting from the larger CTE mismatch of the conductor to SiC and SiN. A thermal cycle test (TCT) was conducted between -40°C and 250°C (ΔTj = 290°C). It was found that the SiC/Au-Ge/CIC-SiN die attachment maintained joint strength of 78 MPa even after 3000 cycles.

1. Introduction

High-voltage SiC unipolar power devices (JFETs and MOSFETs) can switch markedly faster with lower conduction loss even at higher junction temperatures (Tj > 200°C). This feature offers many power applications tremendous benefits such as smaller size, lighter weight, greater robustness and superior cost effectiveness [1-3]. However, extended Tj operation naturally needs a multi-chip power package capable of withstanding greater ΔTj (> 250°C) cycle stress. Conventional high-temperature packages for SiC power devices mostly have a die-substrate structure where semiconductor dies are attached using a high-temperature solder on one of a pair of single conductor foils (typically Cu), direct-bonded or active-metal-brazed (AMB) on both sides of a ceramic plate, usually made of Al_2O_3, SiN or AlN. This substrate structure with Cu foils often causes two failure modes when subjected to greater ΔTj cycle stress: (1) ceramic fracturing under the conductor plates (See (a) in Fig. 3, discussed later) and (2) steep degradation in joint (shear) strength of the die attachment (See (b) in Fig. 5, discussed later) [4, 5]. The objective of this work is to overcome these issues and create a package that has higher reliability against greater ΔTj thermal cycles.

2. Guideline and Proposal

Table 1 lists the coefficients of thermal expansion (CTE) of the major materials used to make conventional die-substrate structures [6, 7]. There are large differences in CTE between the conductor and other materials (ceramics and SiC power chip). This large CTE mismatch repeatedly induces stronger stress at the material interfaces during greater ΔTj cycling, presumably resulting in the two failure modes mentioned above. In

Table 1 Coefficients of thermal expansion

Material		CTE (ppm/°C)
Power chip	SiC	4.5-6.6
	Si	2.49
Conductor	Cu	16.8
	Al	23.6
	CIC (1/8/1)	5.1
Substrate	SiN	2.8-3.2
	Al_2O_3	7.4
	AlN	4.2

order to resolve this problem, it is crucial to reduce the conductor's CTE to a level as close as possible to that of the ceramics and SiC chip.

A new die-substrate structure has been designed and fabricated following this guideline. Figure 1 illustrates a schematic cross-section. The most notable feature is the use of a CIC-SiN substrate where CIC stands for Cu/Invar/Cu clad foils and Invar is a Fe (64%)-Ni (36%) alloy having a very low CTE of 1.2 ppm/°C [6]. The CIC foils used in this work had a C/I/C thickness ratio of 1/8/1 and a total thickness of 0.3 mm. The equivalent CTE of the CIC foils was measured to be 5.1 ppm/°C, comparable in magnitude to that of SiC and SiN (Table 1).

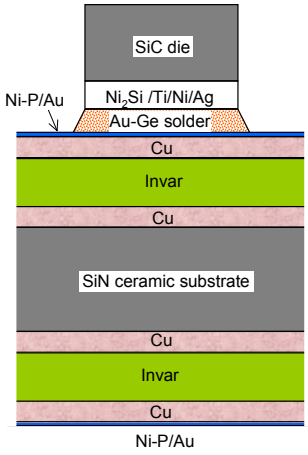

Fig. 1 Schematic cross-section of proposed die-substrate structure

3. Experimental

CIC-SiN substrates were specially prepared by Kyocera Corp., Japan using an AMB method, where a SiN plate (20 × 18 mm^2) had two CIC foils (17 × 8.5 mm^2) on each face and Ti-Cu-Ag was used as a braze alloy. The top surface of the foils was then electroless-plated with 5-µm-thick Ni-P and finished with 0.1-µm-thick Au. Finally, die attachments were performed under a reduced pressure with a reflow soldering system (ATV Technology GmbH, Germany) [4, 5]. Eight SiC dies (2 × 2 mm^2), having Ni-based back contacts and Ti/Ni/Ag metallization [5], were simultaneously soldered on one CIC-SiN substrate using a eutectic Au-Ge solder (m.p. = 356°C, Tanaka Kikinzoku Kogyo K.K., Japan). A typical test sample is shown in Fig. 2.

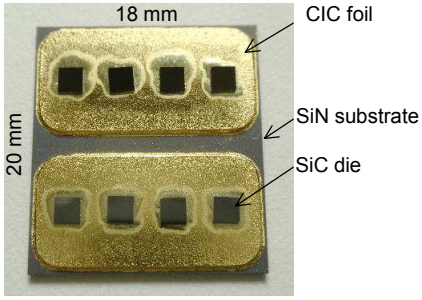

Fig. 2 Typical sample for thermal cycling test

A thermal cycle test (TCT) was conducted between -40°C and 250°C (ΔTj = 290°C) using a TSE-11-AS test system (ESPEC Corp., Japan) [4] and terminated at 10000 cycles for single CIC-SiN samples and at 3000 cycles for die attach samples. One cycle lasted 28 minutes. A standard die shear test was performed to quantify the joint strength of the die attachment system. A bond tester (Model 4000, Dage Holidings, Ltd., UK) was used with a 200-KgF load cell [4, 5].

4. Results and Discussion

Three single CIC-SiN samples without any plated Ni-P/Au were subjected to a TCT and checked every 500 cycles with an optical microscope. The samples displayed a normal appearance at the end of the 10000-cycle TCT, as shown in Fig. 3b, except that the top Cu surface of the CIC foils was considerably oxidized. One single sample was carefully observed by scanning electron microscope (SEM). Figure 4 shows a cross-section near an outer corner of a CIC foil. Note that the thermal stress is concentrated in this area. This X-SEM photograph clearly shows no

(a) (b)

Fig. 3 Appearance of single SiN substrates subjected to a TCT between -40ºC and 250ºC: (a) Cu-SiN (100 cycles) and (b) CIC-SiN (10000 cycles)

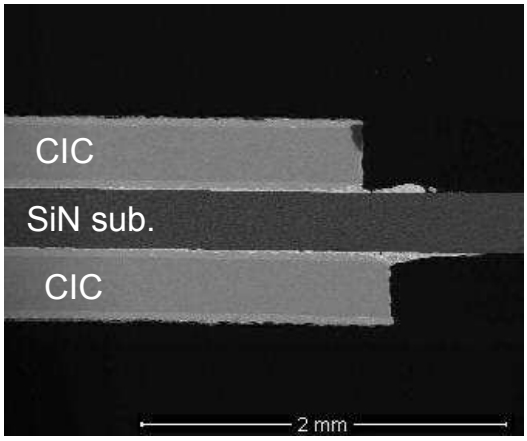

Fig. 4 SEM photograph showing a cross-section across a white lineof the CIC-SiN substrate in Fig. 3b after 10000 cycles of a TCT between -40ºC and 250ºC

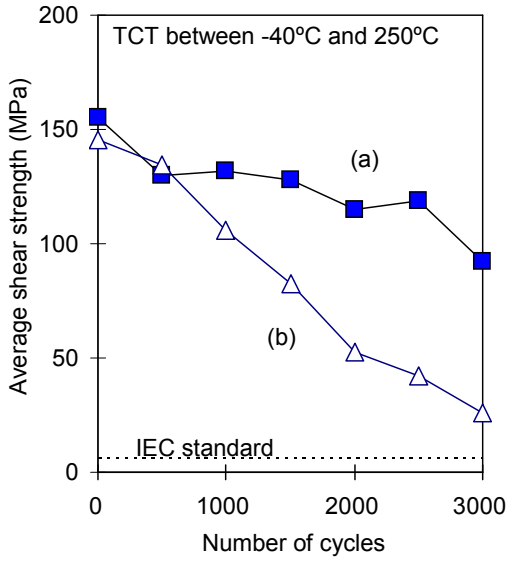

Fig. 5 The average shear strength of the Au-Ge die attachment as a function of the number of cycles: (a) CIC-SiN and (b) Cu-SiN (conventional).

sign of ceramic fracturing under the CIC foil or conductor peeling at the Cu/Invar/Cu metal interfaces. These results confirmed that our CIC-SiN substrate can survive a larger number of greater ΔTj cycles without any problem.

At the point where the single substrate completed 3000 cycles, a TCT was started for the Au-Ge die attachment on CIC-SiN substrates. Test samples (i.e., six substrates with eight SiC dies) were picked out one by one every 500 cycles. Figure 5 presents the test results, as well as our previous results on

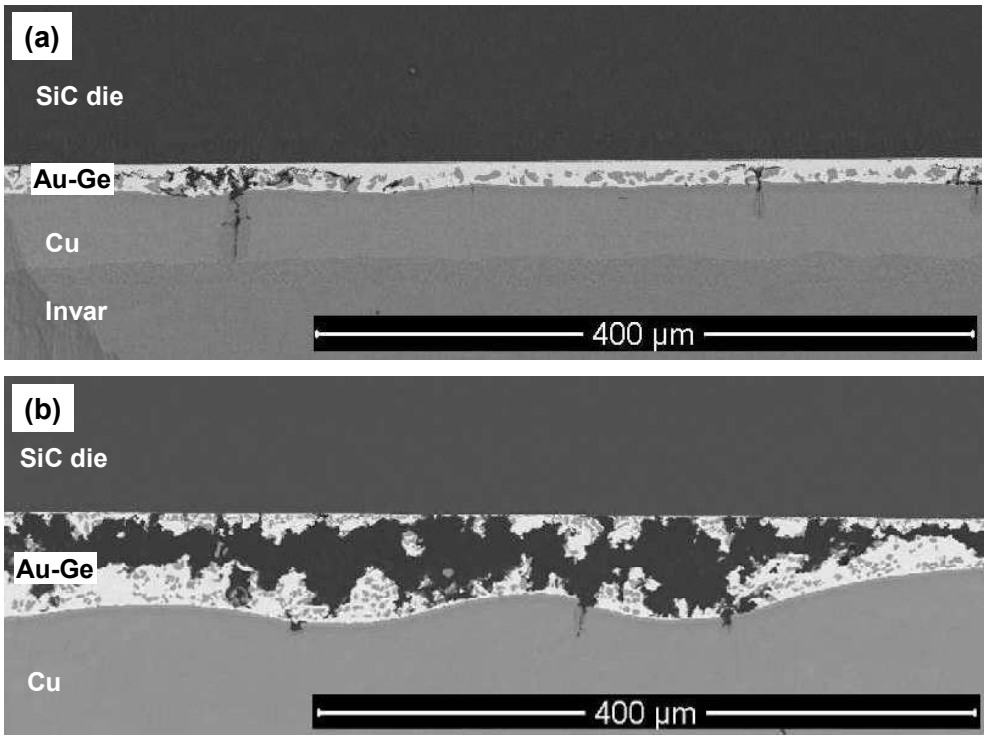

Fig. 6 SEM photograph showing a cross-section of the Au-Ge die attachment on (a) CIC-SiN and (b) Cu-SiN substrate after 3000 cycles of a TCT between -40ºC and 250ºC

standard Cu-SiN substrates [4], where the average shear strength of the SiC dies (N = 7) is plotted as a function of the number of thermal cycles. The results indicate that their shear strength decreased at a rate much slower than that for the standard substrates and still stayed at a level of 78 MPa after 3000 cycles, a value that is 15 times higher than the IEC standard specified in Document 60749-19. This means that our die attachment is extremely highly reliable and has a prolonged thermal cycle life. The results of a linear regression revealed that the estimated cycle life expectancy was more than 8500 cycles. The two SEM photographs in Fig. 6 compare the cross-section of Au-Ge die attachments on both the CIC- and Cu-SiN substrates after a 3000-cycle TCT. It can be seen from these photographs that the die attachment on the CIC-SiN substrate fully maintained the regular joint condition with minimal cracking, while a part of the Au-Ge solder layer on the Cu-SiN substrate almost broke off entirely and an air gap was spreading between the die and the substrate.

5. Summary

A new ceramic package structure for SiC power modules was proposed that is capable of withstanding greater ΔTj cycle stress. Its most notable feature is the use of a SiN substrate with Cu/Invar/Cu foils (C/I/C thickness ratio of 1/8/1) brazed on both sides as conductor plates. The CIC foils show a very low coefficient of thermal expansion of 5.1 ppm/°C and therefore can significantly reduce substrate and die attachment degradation resulting from the larger CTE mismatch of the conductor to SiC and SiN. A thermal cycle test was conducted between -40°C and 250°C (ΔTj = 290°C). It was found that the SiC/Au-Ge/CIC-SiN die attachment maintained joint strength of 78 MPa even after 3000 cycles. The cycle life of this attachment was estimated to be > 8500 cycles.

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References

[1] J. Hornberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. Magan Lal and A. Mantooth, 2004 IEEE Aerospace Conference Proceedings (Big Sky, MT, USA, 2004), pp. 2583-2554.

[2] D.A. Marckx, Breakthrough in Power Electronics from SiC, Subcontract Report NREL/SR-500-38515 (2006).

[3] S. Sato, K. Matsui, Y. Zushi, Y. Murakami, S. Tanimoto, H. Sato and H. Yamaguchi, Forced-Air-Cooled 10 kW Three-Phase SiC Inverter with Output Power Density of more than 20 kW/L, Mater. Sci. Forum, 679-680 (2011) 739-741.

[4] S. Tanimoto, K. Matsui, Y. Zushi, S. Sato, Y. Murakami and T. Yamada, Proceedings, The 18th Symposuim on Microjoining and Assembly Technology in Electronics (Yokohama, Japan, 2012), pp. 107-112 (in Japanese).

[5] S. Tanimoto, K. Matsui, Y. Murakami, H. Yamaguchi and H. Okumura, Proceedings, IMAPS International Conference and Exhibition on High Temperature Electronics 2010 (Albuquerque, NM, USA, 2010), pp. 32-39.

[6] A. Krum, ThermoMechanical Design, in: D.B. Barlow, III and A. Elshabini (Eds.), Ceramic Interconnect Technology Handbook, CRC Press., Boca Raton, 2007, pp. 105-161.

[7] Information on http://global.kyocera.com/prdct/fc/product/pdf/material_e.pdf