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High-voltage diffusion-welded stacks on the basis of SiC Schottky diodes

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Abstract. In the present work we have considered the prototype of a high-voltage diode stack made on the basis of commercial SiC Schottky diodes. Implementation of vertical integration for four diode chips yielded a stack with a reverse current of 25 μA under a reverse voltage of 6 kV. The capacitance of the stack at zero bias was reduced more than three-fold in comparison with the initial diodes. The reverse recovery time of the stack was 7.4 ns. This paper proposes a convenient analytical approach to the estimation of parameters of modular compositions with vertical architecture.

Introduction

With the increasing commercial production of semiconductor devices based on silicon carbide, modular compositions are also activated (e.g. [1]). Horizontal integration using wire bonding is traditionally implemented in the manufacture of modules. Meanwhile, in the manufacture of modules based on silicon and gallium arsenide devices, the method of vertical integration is heavily used (e.g. [2, 3]). For example in [2], High Voltage Power Solutions, Inc. offers a large range of commercial high-voltage diode stacks and rectifier assemblies. In [3], high-voltage GaAs diode stack models made by diffusion welding are presented. We analysed the static and dynamic parameters of the models, and the preliminary technical requirements for GaAs epistructures intended for stacks were determined. It should be noted that the manufacture of high-voltage stacks in the above examples was used for silicon *pn* structures, and *pin* structures were used for the high-voltage GaAs diode stacks. In the manufacture of GaAs diode stacks by diffusion-welding, the metallization of contact surfaces of *pin* structures was carried out simultaneously. In the case of the manufacture of stacks on the basis of SiC Schottky diodes, a somewhat different situation appears. Reference [4] reported that diffusion welding contact directly on the surface of silicon carbide led to a decrease in the potential barrier caused by the microplastic deformation of the contact silicon carbide surface. However, the diffusion-welding connection of the chips with previously formed Schottky contacts by commonly used method avoids these disadvantages. This fact can be considered as a first success from the perspective of the use of diffusion welding applied to Schottky diodes.

In the present work, we have considered the prototype of a high-voltage diode stack made on the basis of commercial SiC Schottky diodes. Implementation of vertical integration is attractive because it is possible to obtain compact integral connections using the entire contact surfaces. The stacks can be used not only as high-voltage rectifiers but also in various composite assemblies as rectifier bridges, AC/DC and DC/DC converter elements, and so on in this field.

Materials and Methodology

To manufacture a high-voltage stack, commercial CPW3-1700-SO10B Schottky diodes produced by Cree, Inc. were used. Four diode chips were connected in series in the column by diffusion welding in vacuum at a temperature of 550 °C and a pressure of 20 MPa. The process was implemented on an SL-05 modernized diffusion welding unit from Frisch GmbH Mechatronic Systems. Aluminium foil with a thickness of 60 μm was used as the connecting material. The connection scheme is shown in Fig. 1.

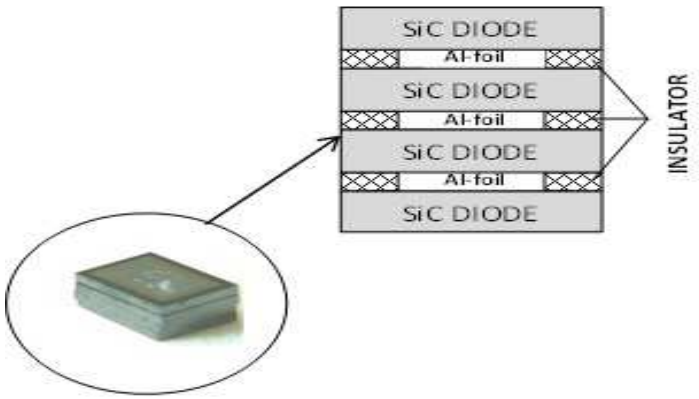

Fig. 1. The scheme of diffusion welded stack.

After welding, the samples were processed by an appropriate treatment in order to provide additional insulation protection of the sides and the gaps between the chips. Then, for the initial characterization of the sample, a series of electrical measurements were taken. The same measurements were taken from the chips of which the stack was made before they were connected by welding to the stack. To carry out electrical measurements, we used the following equipment: an Agilent B1500A semiconductor device analyser, a DLS-83D deep level transient spectroscope, an HCP 350-20000 POS high voltage power supply with a Vitrek 4640B precision high voltage meter, a LEMSYS DMS dynamic parameter system, and an Agilent MSOS104A mixed signal high definition oscilloscope.

Results and Discussion

The results of measurement of key electrical parameters for single chips and for assembled on their base stacks are shown in Figs. 2–5. Key parameters of the diodes and the diode assembly determined from the I-V and the C-V characteristics are summarized in Table 1. In [5] are summarized the conditions at which the diodes can be connected in series without external components for symmetrical parameters. It has been shown that the initial devices must be equivalent in the parameters both in static and dynamic conditions. Therefore, the work we have started with the selection of the initial chips by the closest parameters. However, a simple summation of the parameters in accordance with the number of junctions connected in series would be too simplistic. It is easy to understand that the group of Schottky junctions combined in a series is a complex system of interaction between the energy states, on the barriers, and the analysis of such a system requires special techniques and appropriate equipment. At the same time, the simple measuring instruments applied in this work take connected in stack diodes as a single diode unit with its own quasi-parameters. A good proof of this is the comparison of the ideality factors (n) determined from semi-logarithmic forward I-V characteristics (see Table 1).

As can be seen, the ideality factor of the stack is four times greater than the ideality factor of the initial chips. If we use the definition of the barrier height that is most convenient for us, $\varphi_b = n\frac{kT}{q}\ln\left(\frac{A^*T^2}{J_S}\right)$, and represent the ideality factor as $n = \frac{\varphi_b q}{\ln\left(\frac{A^*T^2}{J_S}\right)}$ (where k is the Boltzmann constant, T is the temperature, q is the elementary charge, and A^* is the Richardson constant), we can see that a four-fold increase in the ideality factor (n) may only be associated with a four-fold

increase in the barrier height (φ_b), since all the other components of the formula for the chips and stack are almost identical. Thus the barrier at room temperature calculated for A^* = 1.2 x 10^{-2} A/m^2K^2 was 1.12 eV for chips and and 4.94 eV for stack respectively. It is understood that in fact the physics of the process must be otherwise. Only a 3.3-fold reduction in the barrier capacitance due to the expected increase of the space charge in the assembly (as opposed to a four-fold, as could be expected) can be attributed to the loss of the active contact area because of the needle-like probe used in the measuring and submicron-sized thickness of the outer metallization (see Fig. 1).

Table 1. Key parameters of the diode chips (mean value) and the stack at room temperature.

n/n	Series resistance R_s [Ohm]	Knee voltage U_0 [V]	Built-in voltage U_B [V]	Capacitance at zero bias C_0 [pF]	Ideality factor n	Saturation Current Is [A]	Reverse recurrent time τ_{rr} [ns]
Chips	79.75	0.65	2.26	724	1.10	7.4×10^{-15}	20.1
Stack	96.50	2.58	5.96	217	4.41	7.5×10^{-15}	7.4

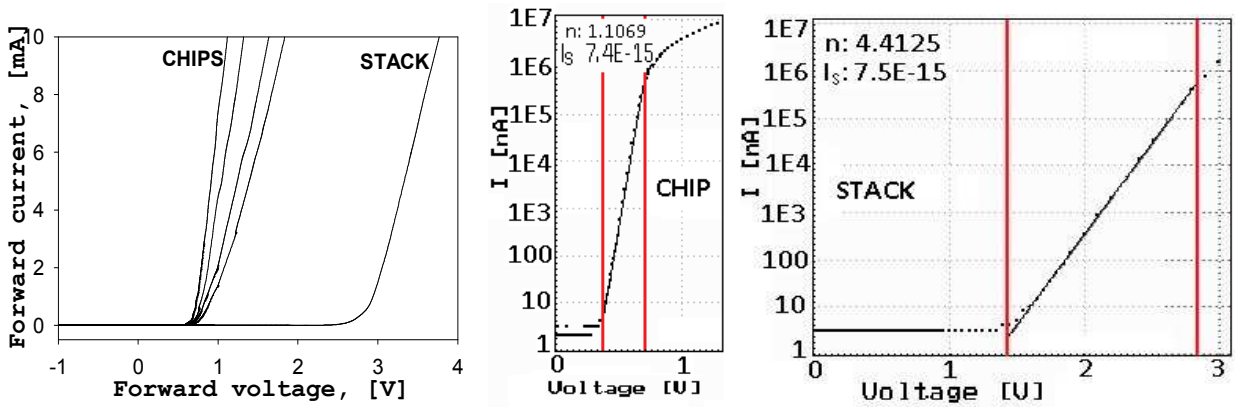

Fig. 2. The forward I-V characteristics and n calculation for chip and stack.

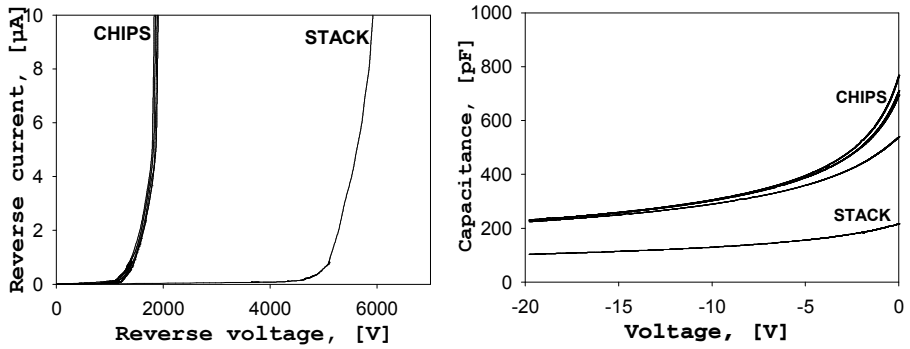

Fig. 3. The comparative reverse I-V characteristics (left) and the comparative C-V characteristics (right) for chips and stack.

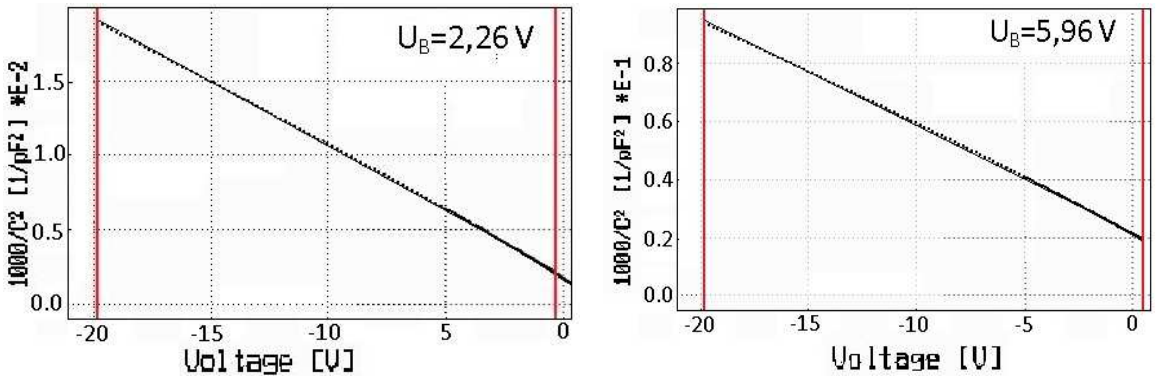

Fig. 4. $1/C^2$ plots for chip (left) and stack (right).

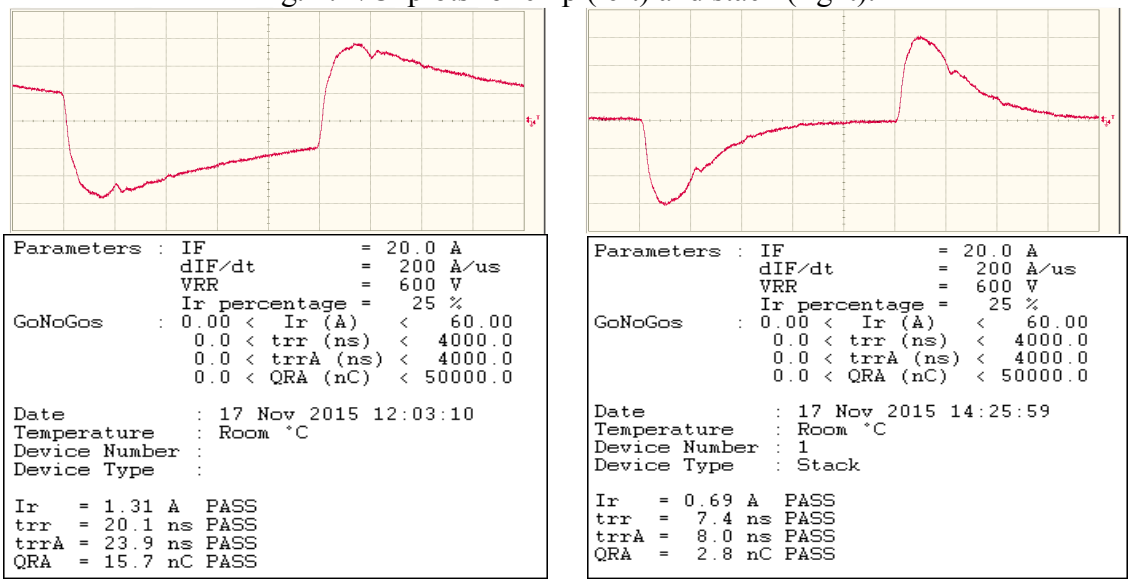

Fig. 5. The comparative view of reverse recovery oscillograms for the chips (left) and stack (right) with the corresponding reverse recovery parameters under waveforms.

Using thick aluminum foil intermediate contacts apparently leads to a slight (only 1.2 fold) increase in R_s for the stack. At the same time, the measured reverse recovery time (τ_{rr}) is in good agreement with the actual values of R_s and C_0. The explanation can be offered based on the expression of Maxwell relaxation time (τ_M) between the two equilibrium states: $\tau_M = \rho\varepsilon\varepsilon_0$, where ρ is the resistivity, ε the dielectric constant, and ε_0 the electric constant. Rewriting the expression as $\tau_M = bR_sC_0\ \varepsilon$ (where the coefficient b takes into account ε_0), we can see that τ_{rr} chips / τ_{rr} stack is equal to R_sC_0 chips / R_sC_0 stack and there is a 2.7-fold decrease (see Table 1).

Summary

In this paper we offered one of the ways of convenient analytical approach to the estimation of the parameters of modular compositions with vertical architecture.
It is shown that in terms of production and consumption of vertical modules, at least in relation to high voltage stacks, the parameters can be predicted and taken into account in the selection of the initial diode elements.

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