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3C-SiC Hetero-Epitaxially Grown on Silicon Compliance Substrates and New 3C-SiC Substrates for Sustainable Wide-Band-Gap Power Devices (CHALLENGE)

Francesco La Via[1,a], Fabrizio Roccaforte[1], Antonino La Magna[1], Roberta Nipoti[2], Fulvio Mancarella[2], Peter Wellman[3], Danilo Crippa[4], Marco Mauceri[4], Peter Ward[5], Leo Miglio[6], Marcin Zielinski[7], Adolf Schöner[8], Ahmed Nejim[9], Laura Vivani[10], Rositza Yakimova[11], Mikael Syväjärvi[11], Gregory Grosset[12], Frank Torregrossa[12], Michael Jennings[13], Philip Mawby[13], Ruggero Anzalone[14], Salvatore Coffa[14], Hiroyuki Nagasawa[15]

[1]CNR-IMM Headquarter, VIII Strada, 5, I-95121 Catania, Italy

[2]CNR-IMM of Bologna, via Gobetti 101, I-40129 Bologna, Italy

[3]University of Erlangen, SCHLOSSPLATZ 4, 91054 Erlanghen, Germany

[4]LPE SpA, VIA DEI GIOVI 7, 20100 BARANZATE Italy

[5]Anvil Semiconductors, WINDMILL INDUSTRIAL ESTATE, BIRMINGHAM ROAD, CV5 9QE, Coventry, United Kingdom

[6]University of Milano-Bicocca, PIAZZA DELL'ATENEO NUOVO 1, IT-20126 Milano, Italy

[7]NOVASIC SA, SAVOIE TECHNOLAC ARCHE BAT. 4, 73375 LE BOURGET DU LAC, France

[8]ASCATRON AB ISAFJORDSGATAN 22 ELECTRUM 207, 164 40 KISTA, Sweden

[9]Silvaco Europe LTDSilvaco Technology Centre Compass point, PE27 5JL St. Ives, United Kingdom

[10]MOVERIM Consulting sprl, SQUARE AMBIORIX 32, 1000 Bruxelles, Belgium

[11]University of Linkoping, CAMPUS VALLA, 581 83 Linkoping, Sweden

[12]Ion Beam Service, RUE GASTON IMBERT PROLONGEE, 13790 Rousset, France

[13]University of Warwick, Kirby Corner Road - University House, CV4 8UW Coventry, United Kingdom

[14]STMicroelectronics SpA, Stradale Primosole, 50, I-95121 Catania, Italy

[15]CUSIC, Sento-Kaikan 5F, 2-2-10 Chuo, Aoba-ku, 980-0021Sendai, Japan

[a]corresponding author: francesco.lavia@imm.cnr.it

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Abstract. The cubic polytype of SiC (3C-SiC) is the only one that can be grown on silicon substrate with the thickness required for targeted applications. However, the crystalline quality of 3C-SiC on silicon has to be improved in order to benefit from the intrinsic 3C-SiC properties. In this project new approaches for the reduction of defects will be used and new compliance substrates that can help to reduce the stress and the defect density at the same time will be explored. Numerical simulations will be applied to optimize growth conditions and reduce stress in the material. The structure of the final devices will be simulated using the appropriated numerical tools where new numerical model will be introduced to take into account the properties of the new material. Thanks to these simulations tools and the new material with low defect density, several devices that can work at high power and with low power consumption will be realized within the project.

Introduction

Emerging wide band gap (WBG) semiconductor devices based on both silicon carbide (SiC) and gallium nitride (GaN) have the potential to revolutionize power electronics through faster switching speeds, lower losses, and higher blocking voltages, relative to standard silicon-based devices.[1] Additionally, their attributes enable higher operating temperature yielding increased power density with reduced thermal management requirements. To date, the advantages demonstrated by WBG power electronics have yet to be fully realized due to their high costs and reliability problems.

Silicon carbide (SiC) is a material presenting different crystalline structures called polytypes. Amongst these only two hexagonal structures (4H-SiC and 6H-SiC) are commercially available and the cubic form (3C-SiC) is an emerging technology. All these materials are broadly similar with high breakdown fields (2-4 MV/cm) and a high energy band gap (2.3–3.2 eV), much higher than silicon. The cubic polytype of SiC (3C-SiC) is the only one that can be grown on a Silicon substrate, reducing the cost by only growing the silicon carbide thickness required for the targeted application. 3C-SiC/Si technology also offers the possibility of increasing wafer size much faster than will be possible with the difficult crystal growth of the hexagonal polytypes.

Tab. I – Property of the main semiconductors for power electronics

Property	**Si**	**3C-SiC**	**4H-SiC**	**GaN**
Band-gap [eV]	1.12	2.35	3.28	3.4
Breakdown field [MV/cm] at $N_D=5x10^{15}/cm^3$	0.3	1.5	2.2	3.5
Intrinsic carrier concentration at 300K [cm^{-3}]	1×10^{10}	1.5×10^{-1}	5×10^{-9}	1×10^{-10}
Electron mobility [$cm^2V^{-1}s^{-1}$]	1350	900	800	2000
Hole mobility [$cm^2V^{-1}s^{-1}$]	480	40	120	200
Saturated electron velocity [$\times10^7$ cms^{-1}]	1	2	2	2.5
Thermal conductivity [$Wcm^{-1}K^{-1}$]	1.5	3.2	3.7	1.3
Dielectric constant	11.7	9.7	9.6	8.9

Different materials can be competitive with 3C-SiC for power applications, as reported in Tab. I.

From this table it can be understood that 3C-SiC and GaN can work in the same range of breakdown voltage but 3C-SiC is more suitable for high power applications thanks to the high thermal conductivity while GaN is more suitable for RF applications thanks to the high saturated electron velocity.

The relatively narrow band-gap of 3C-SiC (2.3eV) with respect to 4H-SiC (3.28 eV) is often regarded as detrimental in comparison with other polytypes but is in fact an advantage. The lowering of the conduction band minimum brings about a reduced density of states at the SiO_2/3C-SiC interface. Therefore, a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) on 3C-SiC has demonstrated the highest channel mobility of above 300 $cm^2/(V\bullet s)$ ever achieved on any of the SiC polytypes, promising a remarkable reduction in the power consumption of these power switching devices.[2] A further advantage of 3C-SiC/Si compared to current 4H-SiC noted by Anvil is the much lower Temperature Coefficient of Resistance between RT and 200°C, ~10% compared with ~100%. This leads to a large reduction of device on-resistance at realistic junction temperatures for power device operation. As in 4H-SiC, the potential electrical activity of extended defects in 3C-SiC is a concern for electronic device functionality. To achieve viable commercial yields the mechanisms of defects formation must be understood and methods for their reduction developed. This project proposes a toolbox of solutions for the reduction of defects based around new compliance substrates that will help to reduce the inherent hetero-epitaxy stress and the defect density at the same time. The structure of these substrates will force the growth to proceed along selected pathways towards a reduction of the defects. Numerical simulations of the growth and simulations of the stress reduction will drive this growth process.

Three different high voltage devices (Schottky diode, MOSFET and IGBT) operating at high power and with low power consumption will be realized within the project. These devices realized on the 3C-SiC material can have a very low R_{on} (R_{on}<5 mOhm) and then a considerable reduction of the power loss with respect to Si and 4H-SiC, in an intermediated breakdown voltage range, can be obtained.

If we suppose to change all the actual silicon power devices used in the world in this range with 3C-SiC devices, a reduction of $1.2x10^{10}$ kWh/year can be obtained. This reduction corresponds to a reduction of 6 millions ton of CO_2 emission. This reduction will be even higher in the next years when the increase of the Photo Voltaic (PV) and of the Hybrid Electric Vehicle (HEV) or Electric Vehicle (EV) market.

The low cost of the 3C-SiC hetero-epitaxial approach, and the high scalability of this process to 300 mm wafers and beyond, makes this technology extremely competitive in the motor drives of Electric Vehicle/Hybrid Electric Vehicle (EV/HEV), air conditioning systems, refrigerators, and LED lighting systems. Furthermore the opportunity of using a p^+ Si substrate can be used to realize an Insulated Gate Bipolar Transistor (IGBT) with a further reduction of the R_{on}.

Our consortium is unique in breadth across the whole supply chain (equipment, materials, characterization, processing, power devices, simulations), and contains the wealth of talent that can be brought together only at international European scale. Furthermore, all the participants have a strong technology and Intellectual Property (IP) on the main arguments of this project and several patents will be used during the project.

A successful CHALLENGE project will place all the consortium members at the leading edge of this technology, and place Europe in a competitive position to fully exploit this new and vital market.

Objectives

Typical figures of merit for power devices suggest that SiC is approximately ten times better than Si in terms of device on resistance for a given operating voltage and also in power density per unit area. Today 4H-SiC is the preferred material but its main limitation is the low channel mobility of carriers, which reduces the performance of the MOSFET switch used in high power applications. This limitation is extremely important especially in the region below a breakdown voltage of 800 V where DC-DC converters and DC-AC inverters are needed for electric vehicles or hybrid cars (see Fig. 1). Currently silicon power devices are used for these applications where the inevitable power dissipation requires the use of very heavy and expensive heat sinks to keep the device junction temperature in the range where Si devices are able to function, because of the low Si band-gap.

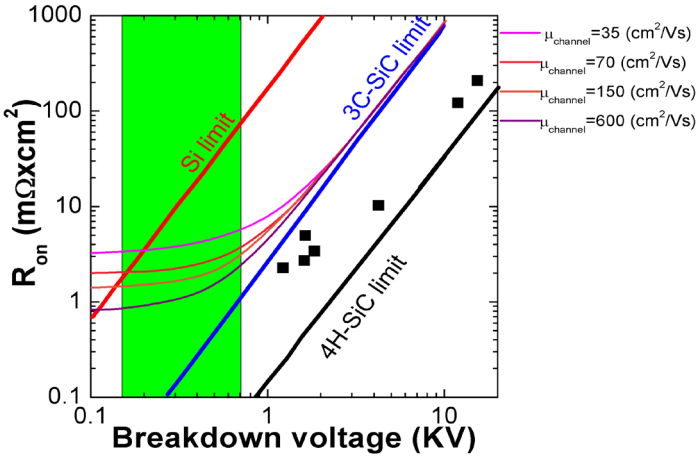

Fig. 1 – R_o vs. breakdown voltage for Si, 3C-SiC and 4H-SiC

The best alternative for these applications is 3C-SiC. To become feasible this emerging technology needs to improve the quality of the material that is grown on the silicon substrate, which can have a high density of defects at the Si/SiC interface. We propose a new approach to improve the quality and to reduce stress: it is necessary to modify the structure of the substrate (compliance substrate)[3,4] in order to force the system to reduce the defects while increasing the thickness of the layer. Furthermore, by using the typical bulk growth techniques used for 4H-SiC it is possible to grow bulk 3C-SiC wafers, improving considerably the quality of the material. This will circumvent the need for silicon with its poor thermal conductivity, leading to a more robust system. With these

improvements in material quality and robustness, it will be possible to obtain good device characteristics and yields to meet the market needs of low power dissipation devices in the automotive applications of the future.

Then the main objectives of the project are the following:

- Develop new compliance substrates that can reduce both the defects (essentially stacking faults) and the stress, hence reducing wafer bow and making device manufacturing easier;
- Develop a **new** CVD process specifically on these compliance substrate to grow thick 3C-SiC layers that can be used both for the realization of some power devices and as seed for the 3C-SiC bulk growth;
- Develop a **new** bulk process using both Hot Wall CVD with chloride precursors and PVT systems on the seed obtained on the compliance substrates;
- Develop new fabrication processes (e.g. gate oxidation, laser annealing of implanted layers, Vanadium doping and more)) that can be used for the fabrication of power devices;
- Develop new simulation codes (Molecular Dynamics, Monte Carlo, Finite Elements, …) to help the experiments on the growth on compliance substrate, to simulate the fabrication process and to simulate the devices;
- Develop new device structure**s** and processes for the realization of some prototype devices (Schottky diodes, P/N junctions, MOSFET and IGBT) that can be used to test the properties of the material (both epitaxial and bulk) and the fabrication processes;

Advance Beyond the State of the Art

Although the hexagonal form of Silicon carbide is the current technology for advanced power conditioning applications, the possibility of 3C-SiC growth on a silicon substrate remains a real advantage in terms of wafer size and hence cost. To date growth of 3C-SiC on silicon has been demonstrated on 150 mm Si wafers and is feasible, with the appropriate tools, on 200 mm or 300 mm wafers. The pace of development of 3C-SiC technology has been hampered by the few industrial epitaxial reactors available, but Europe is currently the main centre of excellence. With this project we will do a further step in the development of this technology and we will bring it closer to the market needs. We will try to develop two different approaches. In the first one we will try to improve the quality of the hetero-epitaxial material using several structured substrates (compliance substrates) that can decrease the defect density and the stress. This approach keep low the cost of the material (a factor 10 or 20 lower with respect to 4H-SiC and comparable to silicon), but it does not take advantage of all the quality of the 3C-SiC in term of heat dissipation due to the low thermal conductivity of silicon. The second approach of the bulk growth increase the cost of the final material but the complete properties of 3C-SiC can be used. Furthermore, the device processing becomes easier because the high temperature processes typical of 4H-SiC processing can be also used. In this case the main advantage with respect to 4H-SiC is the possibility to reach large dimensions directly using the silicon substrates and not the long and expensive process of the ingot enlargement. Furthermore the lower band gap and the higher channel mobility can do of the 3C-SiC polytype the optimum candidate for the breakdown voltage region between 200 and 800 V that is too high for silicon and too low for 4H-SiC.
Furthermore the main patents on this technology are inside the CHALLENGE consortium.

The main problems to solve remain the intrinsic stress created during the growth process due to the lattice mismatch between 3C-SiC (4.36Å) and Si (5.43Å). In addition, thermo elastic stress is introduced during the post-deposition cooling due to the 8% difference in the thermal expansion coefficients between the materials. The resulting stress, which induces the formation of different planar or extended defects in 3C-SiC, is a major parameter leading to a noticeable degradation of the crystalline quality of the epitaxial layer.

Two kinds of defects within epitaxial 3C-SiC films are widely documented. Anti-phase boundaries are planar defects formed at the geometrical separation of two 3C-SiC grains differing

one from each other by a 90° rotation in the Si(100) growth plane. These anti-phased domains (APDs) are formed by the presence of steps on the Si surface, these steps being constituted by an odd number of Si atomic steps. A second kind of defect of importance is linked to the formation of stacking faults along the {111} planes. Most of the published work dealing with 3C-SiC growth on silicon substrates highlight the intrinsic nature of these defects and point out that a drastic reduction of their density is possible by increasing the film thickness or converting the surface polarity of stacking fault. The electrical activity of extended defects in 3C-SiC is a major concern for electronic device functioning. Consequently a drastic reduction of the defects or of their electrical activity is essential to improve the yield and performance of power electronic devices.

Tab. 2 – Advance beyond the state of the art of the CHALLENGE project

Current State of the art of 3C-SiC	**Benefits offered by Project CHALLENGE**
Stacking fault density > 10^4/cm	Stacking faults density ~ 10^2/cm
Bow on 4 inches wafers < 10 m radius for 10 μm layer	Bow on 4 inches wafers > 25 m radius for 10 μm layer
Leakage current > 10^{-2} A/cm^2	Leakage current < 10^{-4} A/cm^2
Channel mobility < 100 cm^2/Vs	Channel mobility > 200 cm^2/Vs

With this project the participants want to reduce these defects density to a level that can decrease strongly the leakage currents of the devices. Furthermore the use of compliance substrates should decrease also the bow of the wafers and then increase the processability of this material. Finally the good quality of the material and the lower band gap with respect to 4H-SiC should give high channel mobility and then low R_{on} of the MOSFETs or of the IGBT devices.
CHALLENGE will address the lack of native substrates and structural defects in 3C-SiC epitaxial layers. These two unresolved problems are the main obstacles towards successful device applications based on 3C-SiC, which has an unexplored potential for power devices, solar cells, biosensors, and many others.

There will be two main routes towards 3C-SiC material fabrication: (i) Si substrate based epitaxy and (ii) boule growth to produce native substrates for subsequent epitaxial growth and device processing. In both routes different innovative approaches will be pursued.

The first approach can have a lower material cost but cannot take advantage of the 3C-SiC high thermal conductivity (see table I) that can reduce the device temperature in the high current applications (as in the HEV or EV) without the necessity of a heavy radiator. The production of a 3C-SiC substrate can solve this problem but will probably increase the cost of the material. An estimate of this cost increase cannot be easily done because it strongly depends on several parameters (growth rate, boule length, growth temperature, market size, etc.) that are not really known at present but after the project conclusion, a more accurate prevision can be done.

Impact

3C-SiC technology can have a large impact in the future power device market. This market is segmented by voltage rating such that different materials can find their applications according to their technical capability and cost. In the low voltage (~100V) section silicon dominates thanks to the technology that has been developed in the last 50 years. In the high voltage (>1200V) section of the market probably 4H-SiC will dominate thanks to its material properties and the possibility to grow large wafers (up to 6 inches). The high voltage segment is not overly cost sensitive and so the high cost of the 4H-SiC substrate is not critical.
The key requirements in each area vary and consequently so do the optimum technology to achieve those requirements. Figure 6 shows the different market sectors and the power ranges in which they operate with approximate market size for 2020.

The technology choices for improving power efficiency in the consumer market between 200V and 1200V are still being debated. One key characteristic of this market is that it is very price sensitive, consequently 4H-SiC technology is unlikely to fit here. These huge markets, as illustrated

below, are likely to be divided between two emerging technologies, We can suggest that between 200V and 500V GaN/Si is best suited to the market needs while between 600V and 1200V the 3C-SiC/Si technology is optimum. This market is growing rapidly and according to the HIS previsions it will go from 100 million dollars in 2020 to 300 million dollars in 2023.
Today, low voltage applications (<1.2kV) represent over 99% of device sales and this is where 3C-SiC/Si comes into its own. Whilst not achieving quite such high breakdown voltages as 4H-SiC, (it is expected to be limited to below 2kV), once mature, it can achieve device prices near to Si and here cost is key. These systems need to be efficient to reduce the demand for electrical power, but designers will be driven by the cheapest way of achieving an acceptable efficiency. Using SiC has the advantage of significantly reducing the component count so SiC components can afford to be slightly higher price of Si and still achieve a lower cost system.

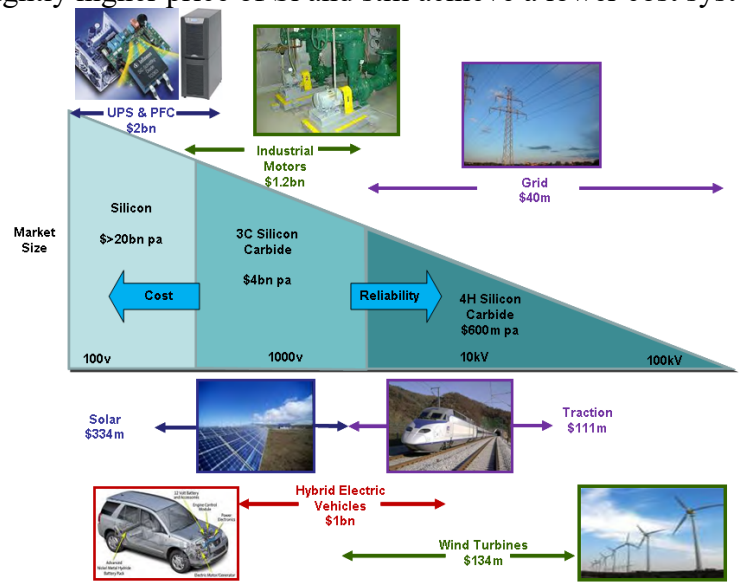

Fig. 2 - SiC Applications and market size in 2020

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