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Electrical Characterization of Integrated 2-Input TTL NAND Gate at Elevated Temperature, Fabricated in Bipolar SiC-Technology

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Abstract. This work presents the design and electrical characterization of in-house-fabricated 2-input NAND gate. The monolithic bipolar 2-input NAND gate employing transistor-transistor logic (TTL) is demonstrated in 4H-SiC and operates over a wide range of temperature and supply voltage.

The fabricated circuit was characterized on the wafer by using a hot-chuck probe-station from 25 °C up to 500 °C. The circuit is also characterized over a wide range of voltage supply i.e. 11 to 20 V. The output-noise margin high (NM_H) and output-noise margin low (NM_L) are also measured over a wide range of temperatures and supply voltages using voltage transfer characteristics (VTC). The transient response was measured by applying two square waves of, 5 kHz and 10 kHz. It is demonstrated that the dynamic parameters of the circuit are temperature dependent. The 2-input TTL NAND gate consumes 20 mW at 500 °C and 15 V.

Introduction

Silicon based integrated circuits (ICs) have been improved significantly in terms of speed, power, and size, but mainly in the low-temperature range (< ≈ 200 °C). At significantly higher temperatures these circuits are susceptible to various issues e.g. thermal runaway, leakage current etc. For the applications such as space exploration, oil and gas drilling, automation and aviation industries we need reliable ICs to work in extreme environment e.g. for Venus surface exploration (surface temperature ≈ 460 °C). Silicon carbide (SiC), because of its wide bandgap of 3.2eV is attractive for elevated temperature and radiation critical applications [1]. Measurement results of digital circuits designed using transistor-transistor logic (TTL) have previously been reported up to 355°C [2]. However, many integrated circuits designed using MESFETs, BJTs, or JFETs have been reported working up to 600 °C [3-5]. Because of its critical gate oxide, the MOSFET is not an ideal candidate for higher temperature applications, which causes reliability issues at higher temperatures. However, CMOS based digital circuits have been reported recently to work up to 470 °C [6].

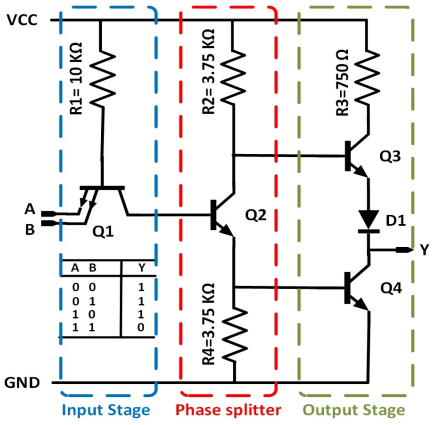

Fig. 1. 2-input TTL NAND gate schematic.

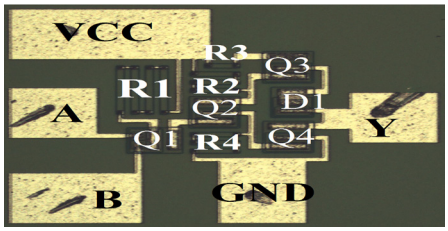

Fig. 2. Micrograph of 2-input TTL NAND gate.

Circuit Design, Implementation and Measurement Setup

This work presents the design, in-house fabrication and electrical characterization of 2-input NAND gates. The schematic of a 2-input NAND gate designed using TTL is given in Fig. 1. According to the schematic of the TTL NAND gate, it consists of three stages. The first stage is

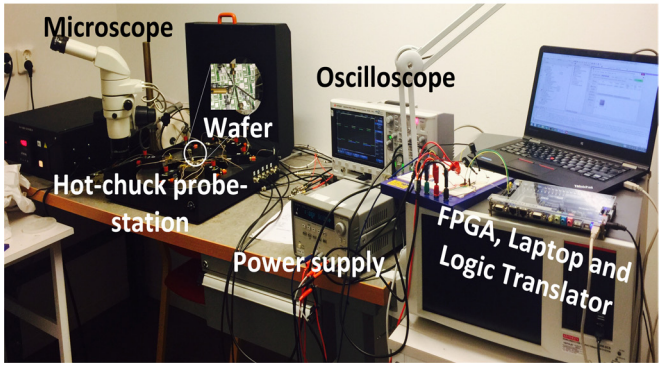

Fig. 3. 2-input NAND gate measurement setup.

called the input stage and it consists of a multi-emitter transistor. The second stage is called the phase splitter. In this stage, the transistor is used as a switch and it splits the phase into two parts i.e. 0 and 1. The third stage is the output stage and it consists of two transistors, both the transistors are on and off in a mutually exclusive way in a totem-pole arrangement. For input combinations (A=B=0) or (A=0, B=1) or (A=1, B=0) the double emitter transistor Q_1 is on and therefore Q_2 is off which splits the phase into logic 1 at the collector and logic 0 at emitter hence Q_3 will be on, Q_4 will be off and the output Y=1. For the input combination A=B=1 the emitter-base junction of Q_1 will be reverse biased and it operates in reverse active mode, this makes the phase splitter Q_2 change the collector to logic 0 and emitter to logic 1, and due to this the transistor Q_3 is off and Q_4 is on hence the final output is at logic 0. The TTL NAND gate has been implemented using a SiC process design kit (PDK) developed for our in-house SiC technology. 4 types of devices have been used to realize the NAND gate i.e. the double-emitter BJT Q_1, single-emitter BJTs $Q_{2,3,4}$, circuit-diode D_1 and resistors $R_{1,2,3,4}$. The micrograph is shown in Fig. 2. A complete TTL digital gate library has been designed and it lays the foundation for complex integrated circuits, such as a microcontroller.

The fabricated circuit was characterized on the wafer by using a hot-chuck probe-station from 25 °C up to 500 °C for 4 hours, the input signals are generated using an FPGA and the logic level is translated by using commercial-off-the-shelf driver circuits. The output signals are analyzed using oscilloscope. The measurement setup is shown in figure 3.

Measurement Results

The transient response from 25 to 500 °C was measured by applying 2 square waves of 10 kHz and 5 kHz and is shown in figure 4. The transient response of 2-input NAND gate as an inverter is shown in Fig. 5 made at 25 to 500 °C by applying the same 10 kHz square wave at both inputs. The measured performance of the NAND gate is summarized in table 1 at 6 discreet temperatures. When the temperature increases up to 200 °C, the output voltage swing remains fairly constant at 11 V, thereafter it increases up to 12.5 V at 500 °C. The delay almost linearly increases with temperature, since the current gain decreases with temperature. The measured output characteristic of the fabricated BJT at different temperatures is shown in fig. 6. The maximum current gain is reduced from 37 at 25 °C to 17 at 500 °C, it is expected that the delay will increase.

Fig. 7 shows the voltage transfer characteristics (VTC) of the TTL 2-input NAND gate at different temperatures. The stable operating points are the highest and lowest intersection points of normal and the inverted VTC curves. The noise margin (NM)

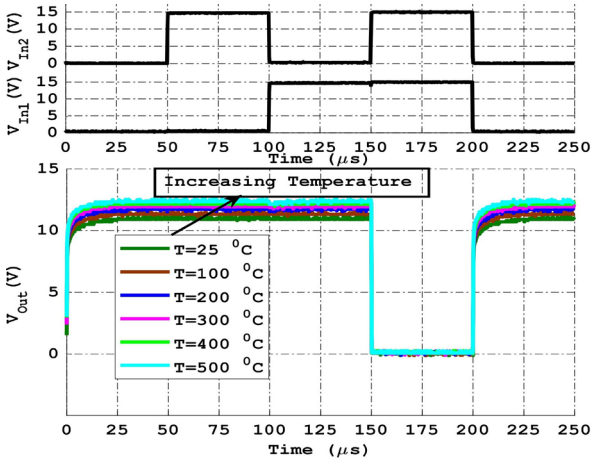

Fig. 4. Measured transient response at T = 25 to 500 °C (f_{In1}= 5 kHz and f_{In2}= 10 kHz).

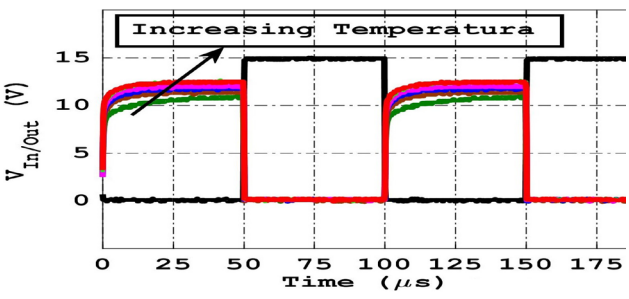

Fig. 5. Measured transient response from T = 25. to 500 °C by applying f_{in}= 10 kHz at both inputs.

is the voltage difference between the stable operating point and the knee of the transfer characteristic, defined as the unity slope point. Fig. 8 shows the variation in NM versus the temperature. As the temperature is increased from 25 to 100 °C, the output-low noise margin NM_L stays fairly constant at 3.7 V after that it starts decreasing down to 2 V at 500 °C. The output-high noise margin NM_H almost linearly increases from 3.5 to 5.5 V, with temperature increased from, 25 to 300 °C thereafter, it increases up to 6.3 V at 500 °C.

Fig. 9 shows the VTC at room temperature and different supply voltages for the 2-input NAND gate, V_{OL} fairly remains constant whereas V_{OH} almost linearly increases with V_{CC}. Fig. 10 shows the variation in noise margins with changing power supply voltage from 11 to 20 V at T = 25 °C. As the V_{CC} increased, the NM_L only increases 0.6 V whereas the NM_H almost linearly increases with V_{CC}. The NM_L increases from 3.4 to 4 V and NM_H increases from 0 to 7.7 V, as V_{CC} goes from 11 to 20 V. As is obvious from Figure 8 and 10, the 2-input TTL NAND gate exhibits adequate noise margins on and above 13 V of power supply.

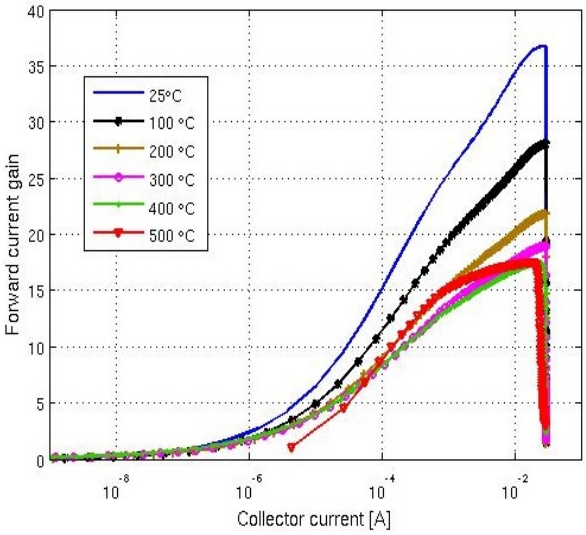

Fig. 6. Measured BJT output characteristics (forward current gain versus collector current at different temperatures).

Table I. Measured performance of TTL NAND gate over wide temperature range.

Temperature [°C]	$V_{OH/OL}$ [V]	t_{rise} / t_{fall} [ns]	t_{PLH} / t_{PHL} [ns]	Power [mW]
25	11 / 0.4	484/250	220/150	30
100	11 / 0.1	426/270	235/170	30
200	11 / 0.2	549/280	245/180	30
300	12 / 0.1	486/290	255/180	25
400	12.5 / 0.1	528/300	265/190	20
500	12.5 / 0.1	593/300	280/200	20

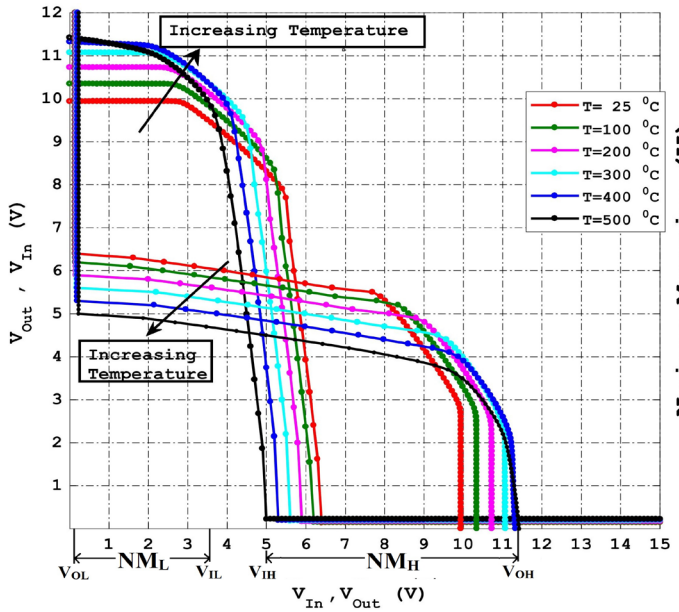

Fig. 7. VTC as temperature increases from 25 to 500 °C at V_{CC} = 14 V.

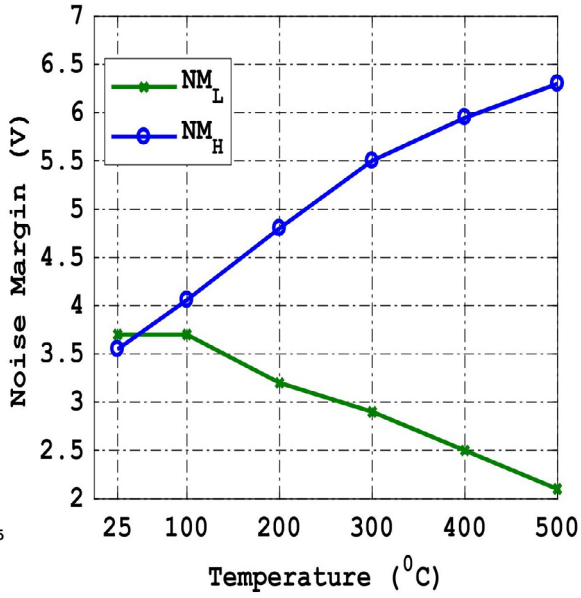

Fig. 8. Noise margins as temperature increases from 25 to 500 °C at V_{CC} = 14 V.

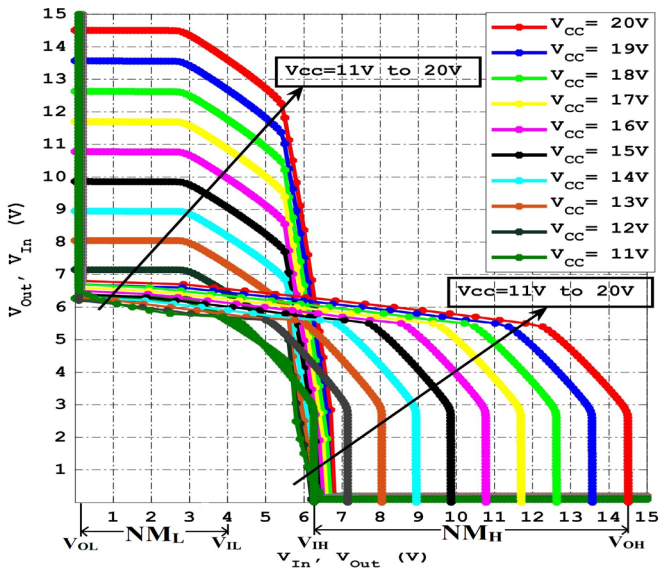

Fig. 9. VTC as supply-voltage goes from 11 to 20 V at T = 25 °C.

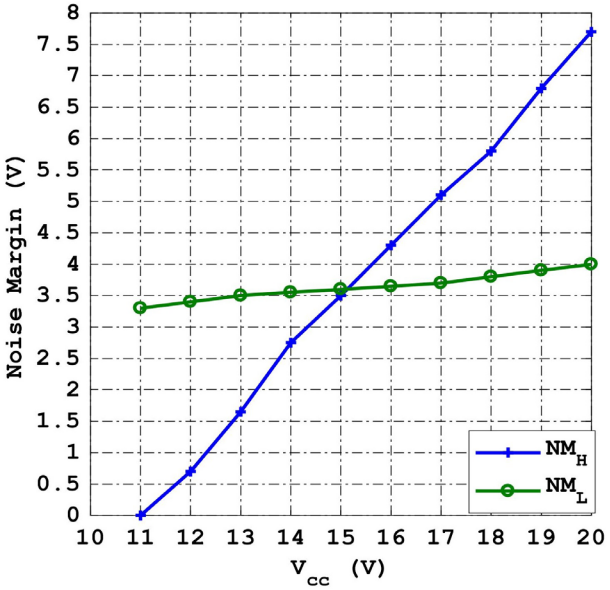

Fig. 10. Noise margins as supply-voltage goes from 11 to 20 V at T = 25 °C.

Summary

A 2-input TTL NAND gate has been successfully designed and characterized over a wide temperature range of 25 to 500 °C. The circuit was also characterized over a wide power supply range. The DC and transient-response demonstrate that this circuit can be used as a basic gate to realize the complex digital systems that can be employed in extreme environments such as the surface of Venus.

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