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Pinch-off effect in p-type double gate and single gate junctionless silicon nanowire transistor fabricated by Atomic Force Microscopy Nanolithography

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Abstract. The spark of aggressive scaling of transistors was started after the Moor's law on prediction of device dimensions. Recently, among the several types of transistors, junctionless transistors were considered as one of the promising alternative for new generation of nanotransistors. In this work, we investigate the pinch-*off* effect in double gate and single gate junctionless lateral gate transistors. The transistors are fabricated on lightly doped (10^{15}) p-type Silicon-on-insulator wafer by using an atomic force microscopy nanolithography technique. The transistors are normally *on* state devices and working in depletion mode. The behavior of the devices confirms the normal

behavior of the junctionless transistors. The pinch-*off* effect appears at $V_G \approx +2.0$ V and $V_G \approx +2.5$ V for fabricated double gate and single structure, respectively. *On* state current is in the order of 10^{-9} (A) for both structures due to low doping concentration. The single gate and double gate devices exhibit an I_{on}/Io_{ff} of approximately 10^5 and 10^6, respectively.

Introduction

Scaling down of conventional metal–oxide–semiconductor field effect transistor (MOSFET), which comprises two p-n junctions, to nanoscale region requires costly and complex fabrication techniques. The junctionless transistor (JLT) is a novel MOS field effect transistor that can be a reliable alternative for the conventional scaled MOSFETs. The JLTs have a constant doping concentration through the source, channel and drain. The lack of doping concentration gradient eliminates diffusion of impurities, high thermal budget and the problem of sharp doping profile formation [1-3]. The conduction mechanism in a junctionless transistor (JLT) relies on the bulk current dissimilar to the conventional MOSFET, which is mainly based on the surface conduction. The device operates by depletion of the majority carriers in the wire and as soon as the channel is depleted, pinch-*off* occurs. Regarding the aforementioned obstacles in MOSFET design and fabrication, finding the new methods of fabrication seem to be essential. Applying AFM nanolithography to fabricate the junctionless transistors (JLTs) is one of the promising methods. The principle of local anodic oxidation (LAO) using AFM nanolithography has been described for the first time by Snow and Campbell et al. [4-6]. In recent years, numerous efforts had been made to improve AFM nanolithography technique [7-9].

In this paper we briefly present fabrication of single and double lateral gate junctionless transistors by AFM nanolithography. The pinch of mechanism based on electric field configuration and carriers' concentration variation along the channel area was demonstrated in single and double gate, which can lead to better understanding the device performance.

Methodology

Fabrication process. The structures were fabricated using the processing steps described in previous works [10-14]. Nanooxidation was done via scanning probe microscope (SPM) machine (SPI3800N/4000). The contact mode tip was coated with Cr/Pt with a resonance frequency and force constant of 13 kHz and 0.2 N/m, respectively. In the fabrication process, after cutting the wafer to the desired dimensions, modified RCA cleaning process was performed in order to eliminate the wafer contaminations.

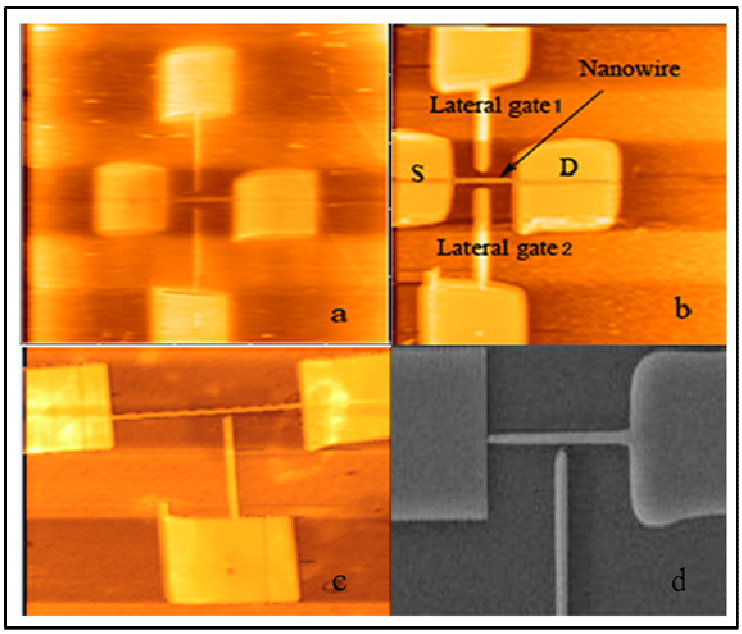

Fig. 1. AFM topography image of DGJLT pattered using AFM-LAO (a) before etching and b) after etching. (c) AFM topography image of SGJLT pattered after etching and (d) SEM image after two successive etching processes.

In the next step, the sample was dipped in a 1% hydrogen fluoride (HF) solution in order to replace the Si–O bonds by low energy Si–H bonds [15]. Hydrogen atoms can be locally removed with an AFM when a negative tip voltage is applied. It leads to a local oxidation of the substrate via a field-enhanced oxidation process by anodization. Fig. 1 (a) shows the created mask by AFM nanolithography using local anodic oxidation technique. After nanooxidation, the wet etching was done by a dilute solution (30% wt) of Potassium hydroxide (KOH) in the de-ionized (DI) water

saturated with 10% (Vol) Isopropyl alcohol (IPA) at 63 °C to remove unproceeded silicon. A silicon dioxide mask with about 3-nm thickness was removed by etching in DI water: HF (100:1) solution. Fig. 1 (b) and (d) indicate single and double lateral gate structure after etching. The physical dimensions for single and double gate junctionless transistors are presented in Table. 1. We named these devices as single and double lateral gate junctionless transistors (S/DGJLTs).

Table 1. Fabricated/simulated device parameters for single gate and double gate structures

	Single/Double gate
Doping	10^{15} cm^{-3}
Length	4.2 [μm]
Width	95-100 [nm]
Thickness	97-100 [nm]
Gate gap	95-100 [nm]
Contact workfunction	5.12 [eV]

Simulation process. The simulation was based on fabrication parameters presented in Table. 1. The structure was doped by boron with a constant concentration of 10^{15} cm^{-3} to create a uniformly doped p-type structure. The contacts work function was taken to be 5.12 eV in all simulation. The electrical characteristics of the device were simulated using a sentaurus software tool as the platform for the 3-D TCAD simulation. The simulations were carried out using hydrodynamic carrier transport model [16]. Besides the fundamental equations, the doping-dependent Masetti model was used for mobility [17] and doping dependence Shockley–Read–Hall recombination-generation [18] was used to account for leakage current.

Results and Discussions

The electrical characterization of the transistor was carried out by Semiconductor Parameter Analyzer (Lakeshore, Desert Cryogenics Agilent HP 4156C). In Fig. 2 drain current versus drain current and transfer characteristics for SG and DG JLTs are presented. It shows that devices were in the *on* state at zero gate voltage and increasing positive gate voltage force the device to *off* state.

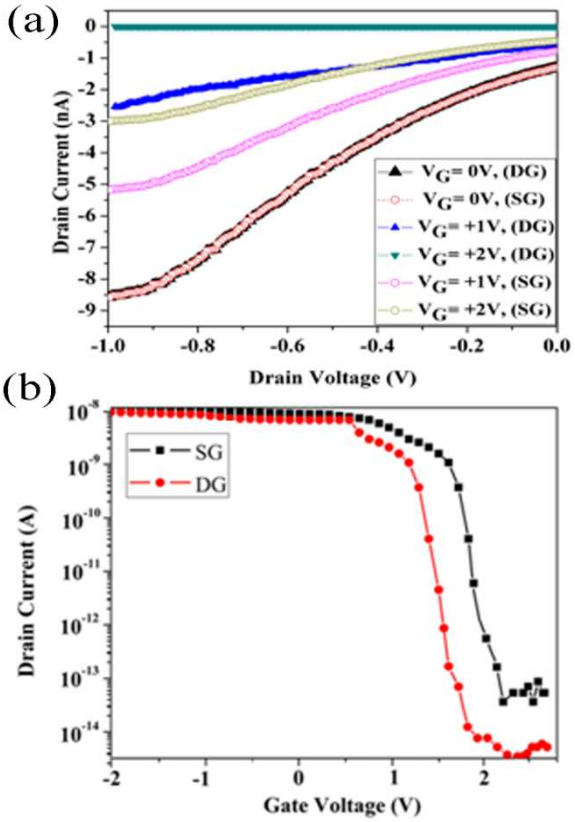

Fig. 2. (a) I_d-V_d and (b) transfer characteristics comparison of single and double lateral gate transistors fabricated by AFM nanolithography.

Junctionless transistors are basically *on* when the device in biased by a small drain voltage and zero gate voltage. However, in the first experimentally fabricated junctionless transistor (gated resistor) the device was in the *off* state at zero gate voltage [2]. JLTs are highly doped semiconductor and according to the MOS structure of the devices and low dimension of channel under the gate the work function difference between gate material and doped semiconductor fully deplete the channel. In order to turn the device *on* a voltage equal to the workfunction difference between channel and gate

material is required. As a result, in the flat band condition junctionless transistor works as a resistor and carriers move in the neutral (undepleted) silicon. It can be seen that, the main operational principle of junctionless transistors is based on the depletion of majority carriers in the channel. The device operates by depletion of the majority carriers in the channel and at a sufficient positive gate voltage as soon as the channel is fully depleted, pinch-*off* occurs [19]. Fig. 3 schematically presents the accumulation and depletion mechanism of device due to the negative and positive gate voltage applied to the lateral gates. Simulation results show that the accumulation of charges mainly located at Si/BOX interface (not shown). By increasing the negative gate voltage this accumulated area cover a small layer on the interface and expand toward the channel surface at the side walls faced to the gates (Fig 3(a)). However, according to the low doping concentration of the channel and source/drain extensions this accumulation is not able to significantly vary the output current. On the other hand, increasing positive gate voltage creates a depletion area in the gated region. According to the design of the device, the depletion process starts from the corners of the channel face to the lateral gates and from Si/SiO_2 interface toward the center and surface of the channel (Fig. 3(b)). It should be noted that the highest depletion occurs near to the drain side of the channel due to the stronger electric field in the drain side [20].

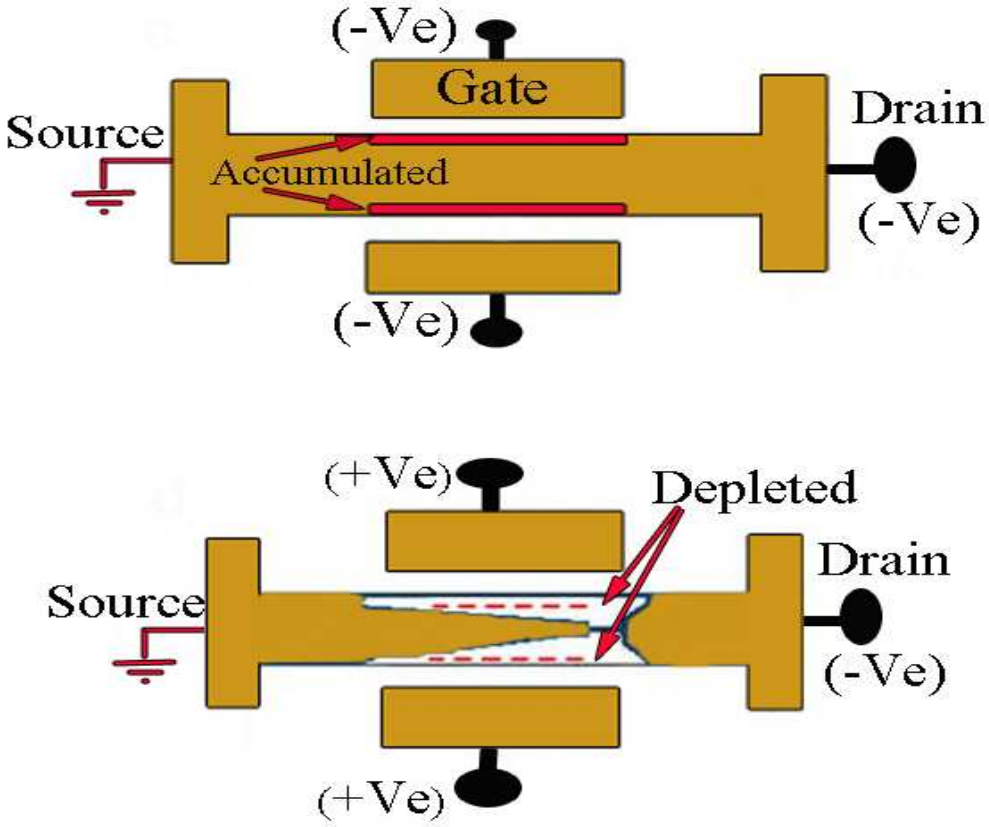

Fig. 3. (a) Schematic operations of DG for (a) negative and (b) positive gate voltage.

In Fig. 4, the location of conduction channels above threshold in the accumulation-mode and DGJLT devices are presented. In accumulation mode devices, in *on* state condition, the majority of the holes were confined in an inversion layers at the sidewalls, with marked peaks at the corners (Fig. 4 (a)). Above threshold voltage, due to the specific shape of the DGJLT and having only one interface with BOX at the bottom, the neutral wire probably formed near to the bottom of the channel and away from the side gate sidewalls (Fig. 4(b)). This area can expand by variation of gate voltage and cover more cross section of the channel.

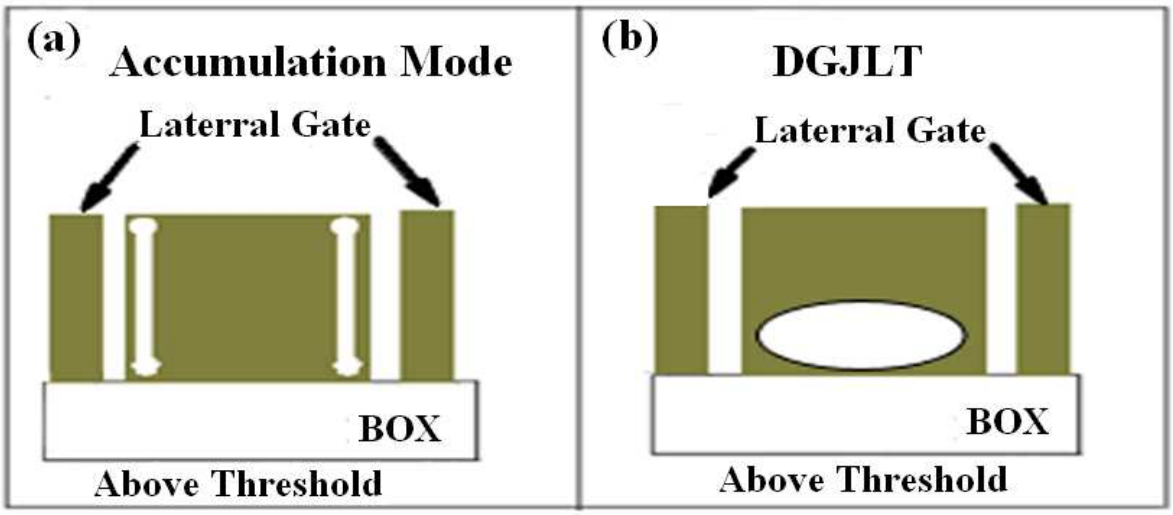

Fig. 4. (a) Location of conduction channels above threshold in the (a) accumulation-mode and (b) DGJLT devices

It is worth noting that in S/DGJLT the electric field originated from the lateral gates was the source of carries depletion in the channel. Fig. 5 shows the electric field in the direction parallel to the majority carriers' movement for single and double lateral gate JLTs.

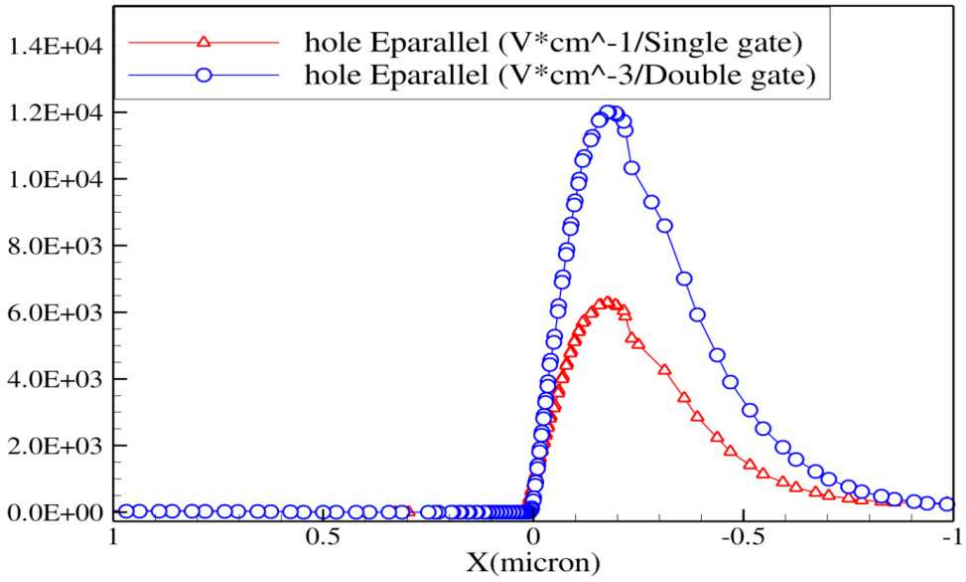

Fig. 5. Simulated parallel electric field along a horizontal cut line at the center of the channel (source side to drain side), V_G= 2.0V, V_{ds}= -1.0 (V)

It can be deduced that, the electrons were attracted to the channel (area under the gates) and holes were repelled by positive gate voltage applied to the lateral gates. Accumulated electrons were increased as the positive gate voltage increased. Attracted electrons by positive lateral gates and repelled by negative drain voltage creates an area of higher electron potential energy in the drain extension of the channel. This potential difference created an electric field in the area under the gates which is shown in Fig. 5. Moreover, the electric field created by double gate structure is stronger than single gate structure due to the symmetry of lateral gates. It shows that the majority carriers (holes) repelled more effectively by double gate structure than single gate structure.

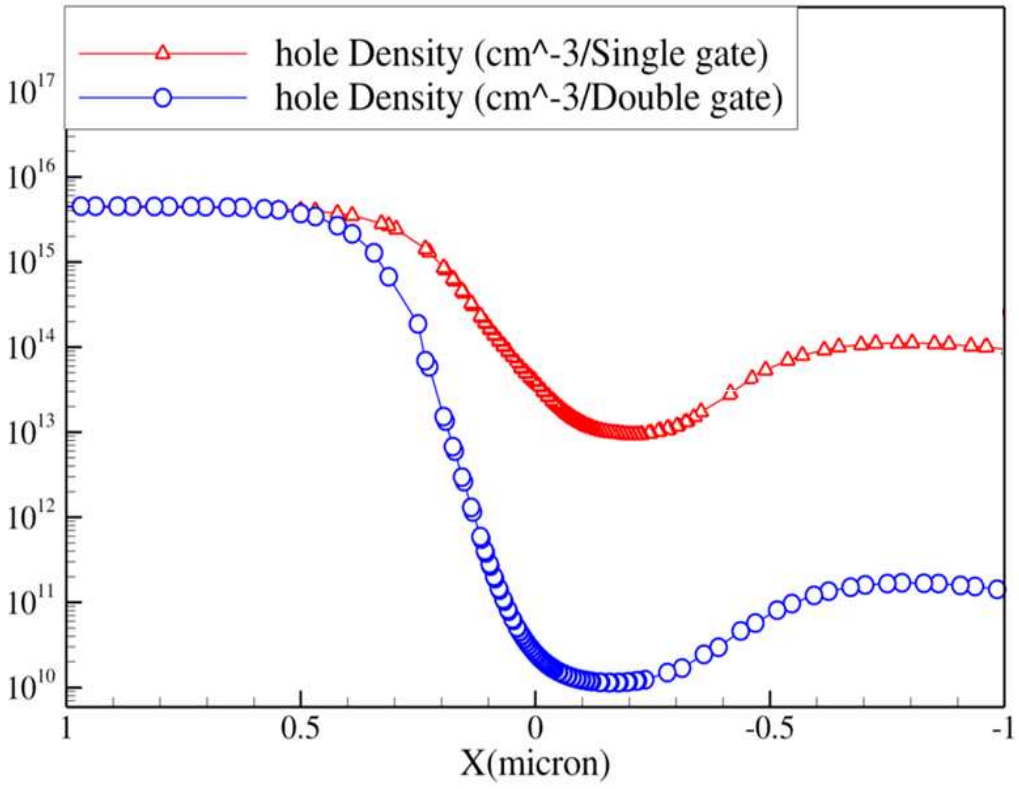

Fig. 6. Hole density distribution along a horizontal cut for single and double gate structures V_G= 2.0 V, V_{DS}= -1.0V

Hole density distribution for single and double gate devices when the lateral gates biased by positive voltage (V_G=+2V) are presented in Fig. 6. It can be observed that in the double gate devices the carriers were depleted more effectively and the device forced to the pinch-*off* state at the lower gate voltage. Since the pinch-*off* mechanism was purely based on electrostatic depletion of carriers by lateral gates the double gate structure shows better control of carriers in the channel and forces the device to the pinch-*off* at lower gate voltage. Moreover, lower leakage current in double gate structure can be explained by small number of majority carriers in the channel when the device is pinched- *off*.

Conclusions

We fabricated single and double lateral gate transistor using AFM nanolithography technique and simulated the same devices using 3D-TCAD simulations. The results demonstrated that both devices working in the pinch-*off* state. These devices were normally *on* at zero gate voltage and the lateral gate electrostatically controls the carriers' concentration inside the channel when a positive gate was applied and force the device to the pinch- *off*. We concluded from the simulation results that the pinch-*off* voltage of double gates transistor was lower than single gate transistor due to the symmetry of the structure and more electrostatic control of the lateral gates on the channel. The leakage current in the double gate structure was more than one order of magnitude smaller compared to the single gate structure. These results suggest that double lateral gate transistors are better candidate compare to the single gate structure, but structural optimization is require to overcome the obstacles in the applications of junctionless transistors.

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