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# Benchmarking Experiment of Substrate Quality Including SmartSiC™ Wafers by Epitaxy in a Batch Reactor

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**Abstract:** The feasibility of thin 4H-SiC layers bonded on an alternative carrier substrate for the application as substrate in SiC epitaxy is investigated. Epitaxial layers grown on such substrates are compared to those on state-of-the-art conventional substrates from different sources. The performance of the substrates is judged by the occurrence of killer defects in the epitaxial layer as analyzed using a PL scanning tool. Additional investigations on the material properties were carried out using X-ray topography and Atomic Force Microscopy, yielding information on the crystallinity, the lattice curvature, and the surface properties of the epitaxial layers.

## Introduction

To produce Silicon Carbide (4H-SiC) power electronic devices, conventional 4H-SiC substrates with 150 mm diameter and 350 µm thickness are currently widely used, which can be purchased from many vendors worldwide. Today, they are still an essential part in the cost structure of power electronic devices as the production of such 4H-SiC wafers is expensive. Therefore, a reduction of material usage for substrates is highly desirable to reduce device costs. Using a very thin 4H-SiC layer could be sufficient for epitaxy and device production. In addition, the device performance can be strongly enhanced thanks to lower device conduction and/or switching losses using ultra high conductivity receiver substrates. SOITEC's Smart Cut™ process [1] yields such a 0.6 µm thin SiC layer, which is transferred to a polycrystalline SiC carrier substrate and bonded thanks to a conductive bonding, called SmartSiC™ substrate.

Substrates contain structural defects, which are inherited to the epilayer and, hence, the active device area. So, they can limit the device performance and production yield [2,3,4]. Thus, the performance of such unconventional substrates must be critically investigated. Defects in epilayers on SmartSiC™ substrates can then have three different origins: 1) inherited from the conventional substrate, 2) originate from the Smart Cut™ and layer bonding processes, and 3) originate from the epi growth itself. This paper aims to investigate the current quality of epilayers grown on SmartSiC™ substrates and identify the origin of defects. For that purpose, SmartSiC™ and conventional 4H-SiC substrates are benchmarked in a comprehensive epitaxial study in the framework of the TRANSFORM EU project.

## Experimental

This benchmark study comprises SmartSiC™ substrates of 4H-SiC donor wafers bonded onto 4H-SiC handler (in this paper named Gen1.1), 4H-SiC bonded onto poly-SiC (in this paper named Gen1.2) and conventional prime grade substrates from STMicroelectronics as partners in the TRANSFORM project as well as other international suppliers (vendor A with prime and engineering grade, vendor B with prime grade). All substrates are n-type and 150 mm in diameter.

All SmartSiC™ substrates contain a conductive bonding layer: the Gen 1.1 substrates a monocrystalline 4H-SiC carrier wafer and the Gen 1.2 a polycrystalline SiC carrier wafer. The SiC top layers of the SmartSiC™ substrates compare well to the conventional substrates although the conventional wafers and the donor wafers are not taken from the same crystal boule. The Gen 1.2 SmartSiC™ wafers contain a top layer from STMicroelectronics donor wafers. Nevertheless, the top layers/donor wafers and the reference wafers have typical defectivities and hence, we can conclude which defects in the epilayer originate from the substrate material. To investigate if the Smart Cut™ process introduces additional defects to the epilayer and if the epi growth process needs further optimization for SmartSiC™ substrates, conventional substrates from different international suppliers are added to the comparison.

All prime grade non SmartSiC™ substrates have been characterized prior to epi growth by x-ray topography (XRT) with a Rigaku XRTmicron [5] and all have been measured with UVPL imaging and surface inspection with a Lasertec SICA88 system. Then, a sequence of epi growth runs has been started in an AIXTRON G5 WW C planetary reactor in 8x150 mm configuration: 1) a standard epi growth process including buffer growth and standard epilayer; 2) a buffer only growth; and 3) a heat-up and cool-down procedure with thermal etching at process temperature. During the epitaxial growth process, in-situ data of temperature profiles and wafer curvature was recorded.

Only those wafers with grown layers were then characterized regarding epilayer thickness and doping concentrations by FTIR spectrometry and mercury probe CV measurements, respectively. All wafers were characterized using UVPL imaging plus DIC/optical microscopy and all full stack epilayers with XRT for defectivity after the epitaxial process or thermal etching.

**Table 1:** Average thickness and doping results for the different structures grown in the epi growth experiments on SmartSiC™ and conventional substrates.

| epi growth experiment | all wafers in experiment (averages) | | | |
|---|---|---|---|---|
| | buffer thickness | buffer doping | drift layer thickness | drift layer doping |
| buffer + drift layer | target 1 µm (1) | 1.20E18 $cm^{-3}$ | 15.2 µm | 1.03E16 $cm^{-3}$ |
| buffer only | target 1 µm (1) | 1.20E18 $cm^{-3}$ | no drift layer | |
| heat up & cool down | no growth in this experiment | | | |

(1) 1µm is below the reliable range of the FTIR thickness measurement system used

These X-ray topography measurements were carried out according to the Lang method using the (0008) reflex of Cu Kα radiation using an anode power of 1.2kW (40kV, 30mA) and a scanning speed of 30mm/min on the full wafer area. A CCD detector with a pixel pitch of 5.4µm and a distance to the sample surface of 60mm was used in time-delay integration (TDI) mode to capture the topograms. Reference samples were analyzed using an in-house TSD counting algorithm to determine the density distribution of this dislocation type in agreement with SEMI M91 [6].

Surface morphology was characterized by atomic force microscopy (AFM) on different measurement areas, e.g., 5 x 5 µm² scans for investigation of growth steps and 50 x 50 µm² scans for large-scale surface characteristics. All scans were performed at the wafer center with 256 points/line and 256 lines/scan. The data were further processed with a second order flattening and Rq value extraction.

## Results

The epi growth results for the epilayer thickness and doping are summarized in Table I. Due to the large batch capacity of the used epitaxy reactor, all different types of substrates were processed in the same run.

**In-Situ curvature measurements.** First in-situ measurements showed a typical concave wafer curvature in process of 50-80 $km^{-1}$ for the reference wafers from international suppliers A and B as well as for the SmartSiC™ Gen 1.1 substrates. The substrates supplied by STMicroelectronics showed slightly lower curvature values in the range around 35 $km^{-1}$. The Gen 1.2 substrates (on the polycrystalline carrier) showed a convex curvature of approximately -40 $km^{-1}$. All these curvatures at high temperature are uncritical and unlikely to impact the process results.

**Lasertec SICA88 defect scans.** The defect scans on the SmartSiC™ wafers were performed with slightly changed settings compared to the conventional substrates. This was done to adopt the defect recognition to the different surface morphology of the SmartSiC™ wafers (see also the AFM results). Main changes were a reduced brightness of the DIC channel and shifted thresholds for the defect recognition algorithm.

Due to this there is no reliable detection of small surface defects like micropits and bumps on Epilayers on SmartSiC™ substrates. For the other prime grade wafers, the substrates by STMicroelectronics showed the lowest number of pits with vendor A and B being similar within statistical variations. Vendor B showed a quite high number of bumps while vendor A is on a very similar level to STMicroelectronics.

Other defects are more reliable to compare and show a relatively even distributions across the wafer. Some defects on some wafers show weak clustering along the wafer edge (Figure 1). The following trends are extracted with an increased edge exclusion zone to not let bonding failures on the edge of the SmartSiC™ wafers impact the results too much.

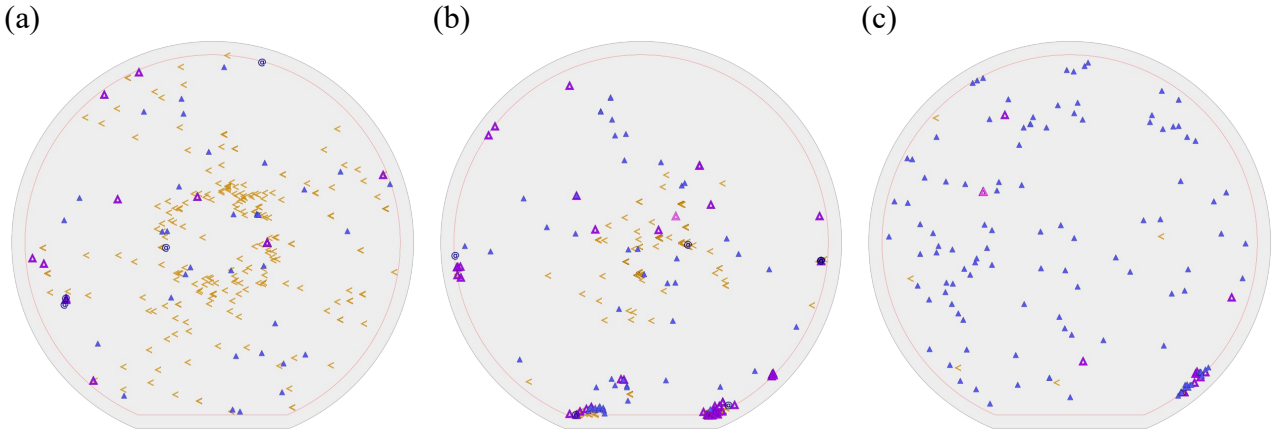


**Fig. 1**: Killer defect map of epilayers on various 150mm substrates: a) standard prime grade substrate of vendor B, b) prime grade substrate of STMicroelectronics, c) SmartSiC™ substrate on a monocrystalline carrier (<=stacking fault with surface signal, Δ=triangle defect, O=particle, ▲ stacking fault without surface signal)

- For micropipes we see a group of similar performance consisting of STMicroelectronics, SmartSiC™ Gen 1.2 and vendor B. Vendor A shows a significantly higher number of micropipes while the SmartSiC™ Gen 1.1 shows a very low number.
- Stacking faults with a surface signal (e.g., carrot defects) are very low on both SmartSiC™ generations with all bulk substrates performing significantly worse.
- A similar situation shows up for polytype inclusions (e.g., triangle defects) and basal plane dislocation. Here as well the SmartSiC™ substrates perform better than the tested bulk wafers.

- Regarding stacking faults without a surface channel (PL_SF in Figure 2) and propagated or bar-shaped stacking faults, the bulk substrates perform best. In these cases, especially the SmartSiC™ Gen 1.2 shows higher defect densities while STMicroelectronics and vendor B performing the best with densities lower by about a factor of 5-10.

The increased number of stacking faults without a surface channel signal combined with the decreased number of stacking faults with a surface channel signal on the SmartSiC™ can point towards a problem in the defect recognition by the Lasertec SICA88 software due to the different surface morphology with increased roughness (see AFM results). When looking at the sum of all stacking faults with and without a surface signal component SmartSiC™ substrates perform very close to the STMicroelectronics substrates with vendor B close behind. Vendor A shows an increased total number of stacking faults.

The engineering grade wafers by vendor A (not included in Figure 2) mainly showed a higher density of basal plane dislocations compared to all other substrate types.

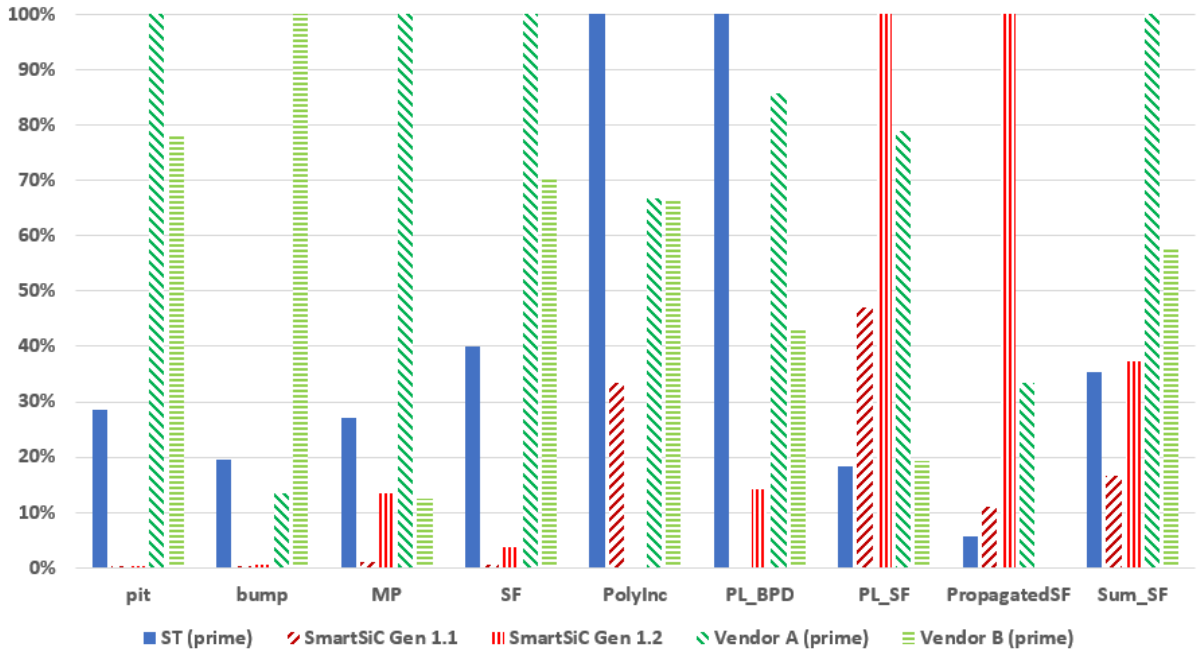


**Fig. 2:** Comparison overview of defect numbers extracted from the Lasertec Sica88 scans on samples with the full epi layer stack. All results normalized to the highest defect count per category. Pit and bump numbers on SmartSiC™ substrates are unreliable due to surface roughness. (MP=micropipe, SF=stacking fault with surface signal, PolyInc=triangle defect, PL_BPD=basal plane dislocation, PL_SF=stacking fault without surface signal, Sum_SF=sum of stacking faults with and without surface signal)

**X-Ray Topography:** Analysis of the reference wafers using XRT did not reveal any abnormalities. For example, we observe the propagation of almost all TSDs into the epitaxial layer with the expected small reduction of TSD density after epitaxy [7] (see Figure 3). The lattice curvature changed slightly towards a more convex shape. Since the reference wafers were provided by different manufacturers featuring different initial curvature, this means that an originally slightly concave-curved lattice became slightly convex while the convex lattice deformation became stronger if the lattice curvature of the substrate was already convex.

Topograms of epitaxial layers on SmartSiC™ substrates are completely different than those on the reference wafers. Instead of dislocations, the contrast is dominated by larger scale structures, which strongly differ between Gen 1.1 and Gen 1.2 substrates.

In Figure 4a, the topogram of a representative epitaxial layer on a Gen1.1 substrate contains mainly two visible patterns: Concentric, slightly curved stripes emerging from a circular structure in the wafer center and, more dominantly, a periodic, wave-like pattern of curved lines with an apparent

center outside on the top left side of the wafer. The former structures are very likely related to grinding structures.

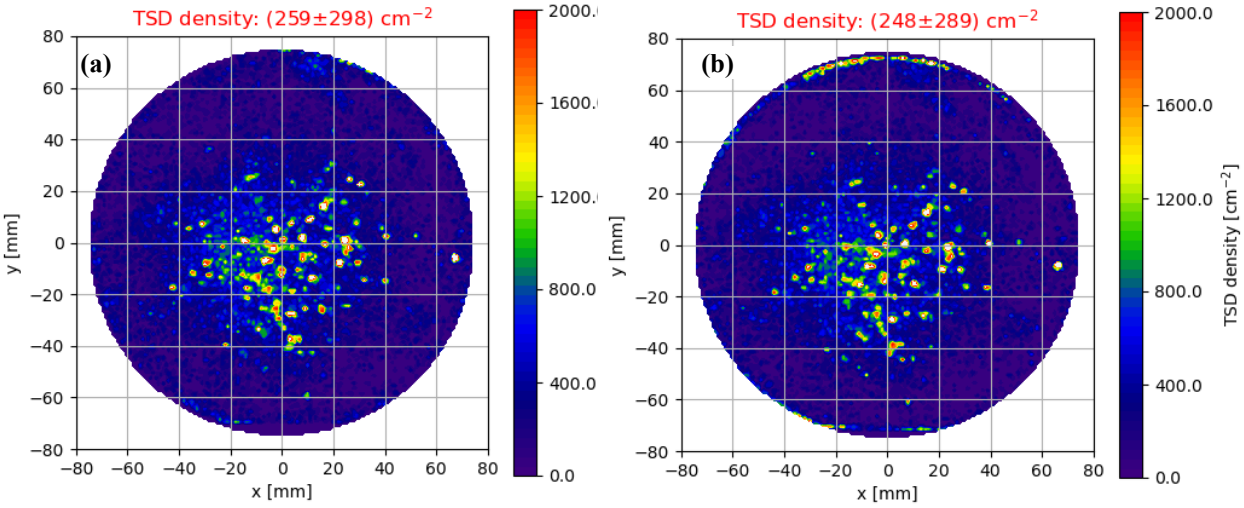


**Fig. 3**: Comparison of the TSD density mappings of one reference wafer (a) before and (b) after epitaxy. The large signal in the top region of the processed wafer is an edge effect which does not contribute to the average values due to an edge exclusion of 5mm.

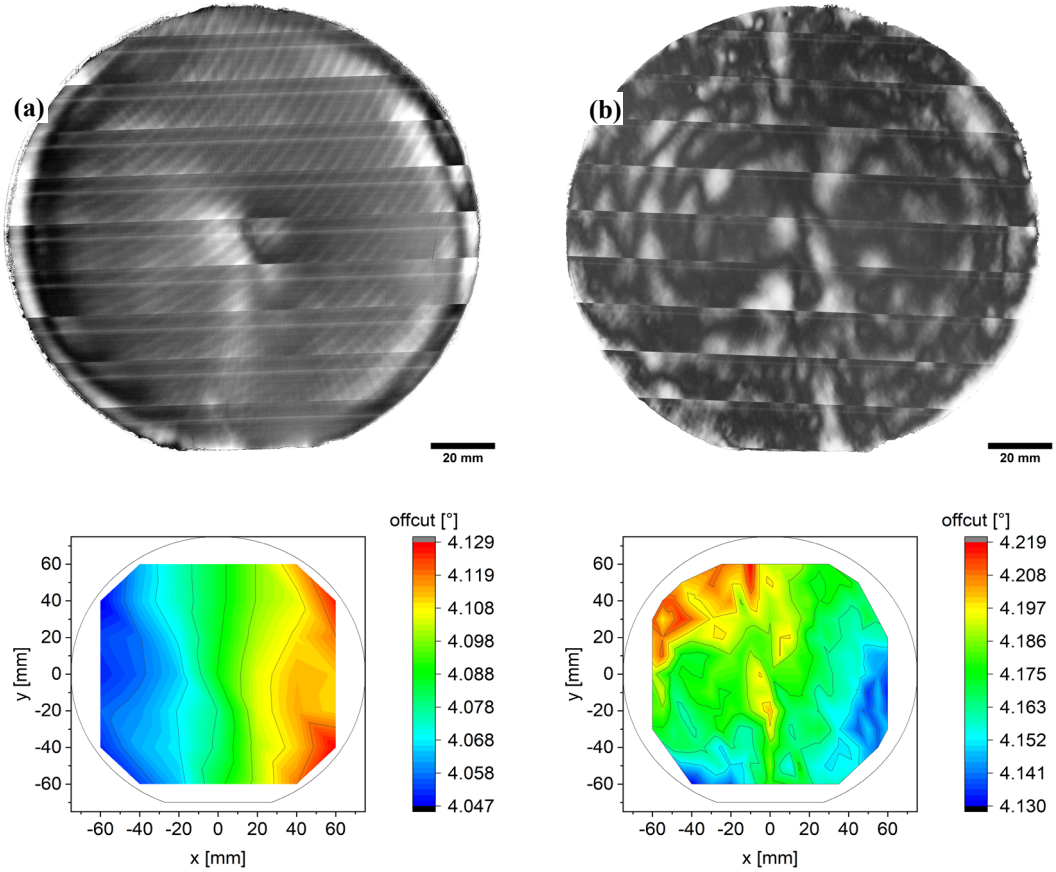


**Fig. 4**: X-ray topograms of epitaxial layers on SmartSiC™ substrates of (a) Gen 1.1 and (b) Gen 1.2. The respective curvature mappings showing the lateral offcut variation are depicted below the topograms.

From the other results it can be excluded that this is due to grinding damage on the front side of the wafer. Rather, this is either the damage on the backside of the SmartSiC™ layer which also contributes to the diffraction contrast, or the layer may also be affected by grinding damage and thus

surface roughness on the carrier wafer, which is propagated to the SmartSiC™ layer in the form of a slight lattice bending. The lattice curvature of this wafer is moderately convex.

The topogram of the Gen1.2 sample (Figure 4b) is dominated by local contrast variations over the wafer. The origin for that becomes clearly visible when inspecting the wafer curvature: The epitaxial layer exhibits strong local lattice bending. This causes strain in the lattice resulting in increased contrast for the Lang method and in strong intensity variations due to the Bragg condition not being fulfilled perfectly at all positions within the measurement beam. As this variation is not seen for the Gen1.1 sample, the origin are likely inhomogeneities of the poly-SiC substrate affecting the curvature of the SmartSiC™ layer.

This local bending of the lattice is on a scale of ±0.05°, which is still well in spec for substrates. Based on the results of the crystalline defects as seen by the Lasertec surface inspection and PL mapping, these variations do not seem to have a significant impact on the epitaxial growth. An impact on further device processing steps can at the moment not be excluded though and is in the scope of further investigations.

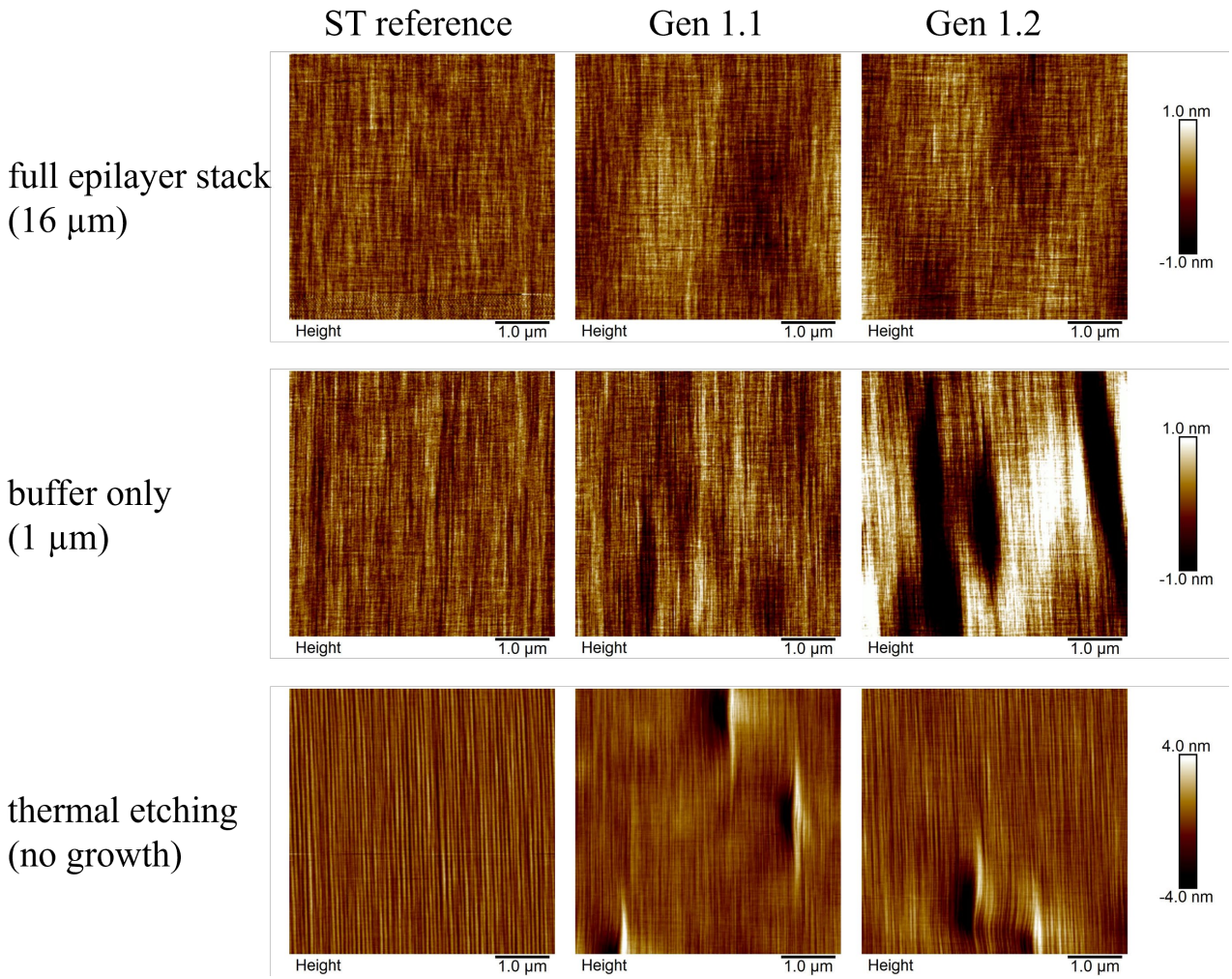


**Figure 5**: Compilation of small-area AFM scans (5 µm x 5 µm) showing the step morphology of benchmark wafers after growth of the full epilayer stack (upper row), after buffer layer growth (center row) and after thermal etching (lower row) for STMicroelectronics reference and SmartSiC™ Gen 1.1 and 1.2 wafers.

**AFM measurements** have been done to investigate the step flow growth and to clarify open questions regarding the surface morphology and waviness of the surface indicated by XRT and SICA measurements. Therefore, step flow was investigated on 5 µm scans and large-scale waviness on 50 µm scans. Figure 5 shows a compilation of 5 µm x 5 µm AFM scans of full epilayer stacks, buffer layer and after thermal etching of STMicroelectronics reference wafers and SmartSiC™ Gen 1.1 and

1.2 wafers. All samples show well-defined growth steps, proving that the steps are dominating the surface morphology on small scale. Additionally, surface defects are detected on SmartSiC™ wafers (both Gen 1.1 and 1.2) after thermal etching and buffer growth. The surface roughness, characterized by the Rq value, is below 0.25 nm for all epiwafer surfaces with growth steps; those having steps and defects show higher Rq values of 0.85 nm.

Large-area scans of the benchmark wafers are shown in Figure 6. On STMicroelectronics reference wafers, the surface morphology is characterized by steps and does not show remarkable waviness (please consider the small range of height scaling of ± 1.2 nm). Contrarily, all SmartSiC™ wafers show large-scale roughness in form of large pits/defects after thermal etching and buffer growth or "wormy" waviness after growth of the full epilayer stack. The nature of the large pits or defects is not clear yet. The large-scale waviness fits well to the findings with SICA and XRT methods. As this is recognizable in the AFM scans, the waviness is indeed also present at the top surface of the SmartSiC™ wafers.

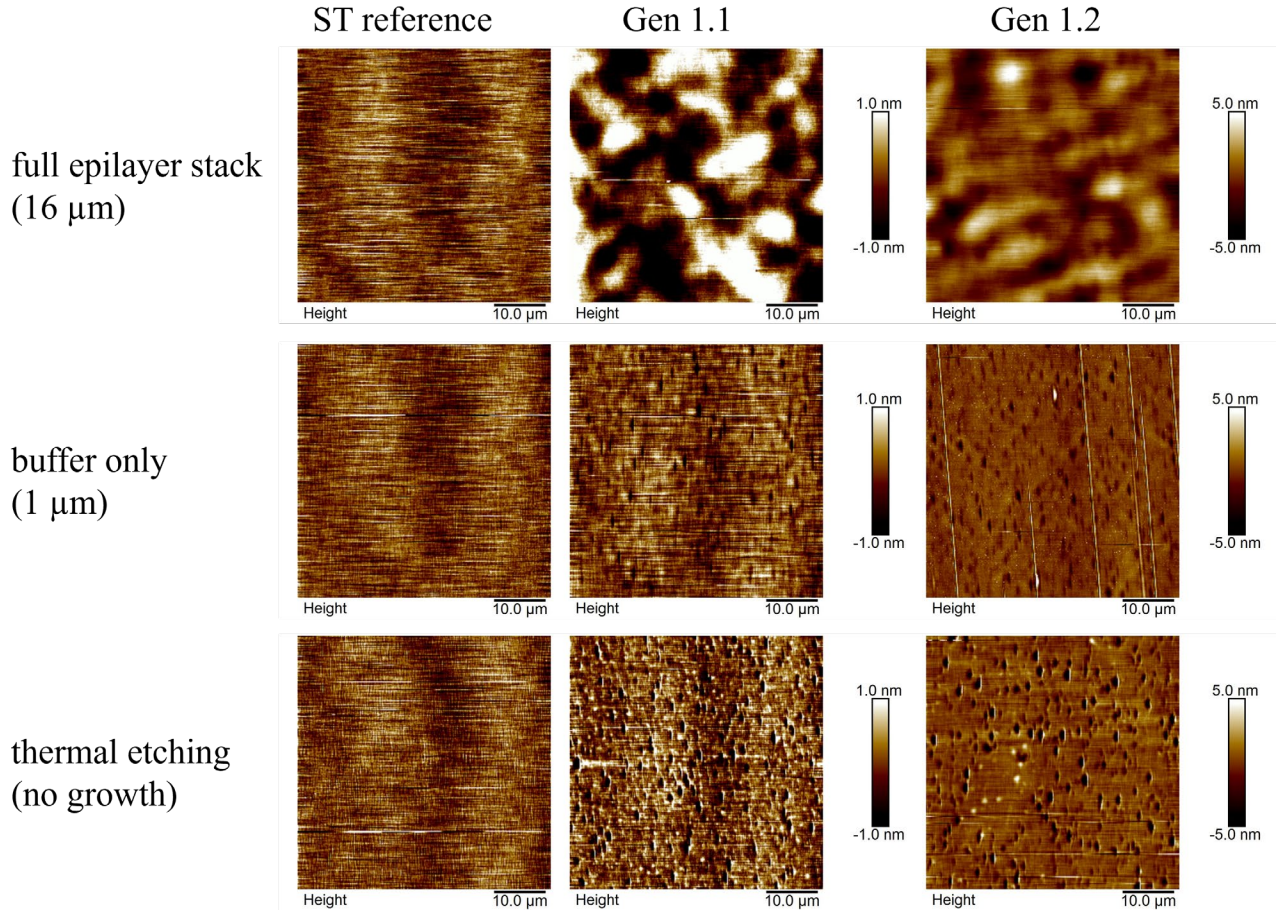


**Figure 6**: Comparison of surface morphologies of benchmark wafers after growth of full epilayer stack (upper row), of buffer layer (center row) and after thermal etching (lower row) for STMicroelectronics reference wafers and SmartSiC™ Gen1.1 and Gen1.2 wafers. Horizontal lines are artefacts from measurement. Rq values are extracted from full measurement area except for areas with artefacts.

**Summary**

We investigated the performance of SmartSiC™ substrates compared to conventional ones in SiC epitaxy. The morphology of the SmartSiC™ substrates shows to be distinctly different regarding both bulk properties as well as the surface. Nevertheless, PL scans showed that only few defects form during epitaxy, yielding an epilayer quality at least on par with prime grade bulk substrates. This observation gives reason for assuming a good performance of this material also in devices, which will be subject of future studies.

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