

## Effect of Sub-Surface Damage Layer Removal by Sublimation Etching of 4H-SiC Bulk Wafers on PL Imaging of Crystal Defect Visibility

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**Abstract.** Improving the visibility of defects in nitrogen-doped 4H-SiC (0001) bare wafers by photoluminescence imaging (PLI) is essential for improving the epitaxial growth process and device yields. This study proposes sub-surface damage (SSD) introduced during the mechanical process of SiC wafers as a new factor in reducing defect visibility in PL images. To verify the effect of SSD, we observed the surface of a SiC wafer, which was thermally etched at about 3  $\mu\text{m}$ . As a result, dramatic defect visibility improvement was observed when the surface roughness was sufficiently flat ( $R_a < 0.3 \text{ nm}$ ) after thermal etching. Thus, the results suggest that defect visibility in PL images can be improved by controlling SSD and surface roughness. Using the background noise reduction effect of the SSD removal, not only PLI but also many other wafer surface inspections are expected to be improved.

### Introduction

Visualizing crystal defects in bulk 4H-SiC bulk wafers by photoluminescence imaging (PLI) significantly improves the conditions of bulk and epilayer growth. In 4H-SiC bulk wafers, crystal defects such as micro-pipes, threading screw dislocations (TSDs), threading edge dislocations (TEDs), Basal plane dislocations (BPDs), and stacking faults (SFs) cause surface roughness during epitaxial growth and device yield loss. In verifying the behavior of crystal defects before and after epitaxial growth, it is necessary to determine the density, distribution, and type of defects while maintaining the surface topography of the bulk wafer. Therefore, a combination of PLI and machine learning has been considered to inspect the crystal defects of large-diameter SiC bulk wafers [1,2]. However, one critical problem with PLI is that detecting crystal defects in the nitrogen doping density of the  $10^{18} \text{ cm}^{-3}$  range is considered difficult, which is typical for n-type bulk wafers [3,4]. Generally, this is attributed to the fact that the background luminescence intensity is increased by the reduction of carrier lifetimes [5]. Meanwhile, Mahadik *et al.* observed BPDs with PLI in a buffer layer with a nitrogen-doped concentration of  $3 \times 10^{18} \text{ cm}^{-3}$  [6]. This result suggests that factors other than high nitrogen doping may make it challenging to observe crystal defects in PL observation of bulk wafers.

Bulk wafers differ from highly nitrogen-doped buffer layers in the presence of sub-surface damage (SSD) layers that are introduced during the mechanical processing from ingot to disc shape [7,8,9]. Since SiC is a hard and brittle material and requires diamond components for mechanical processing, such as slicing, grinding, and polishing, a damage layer is introduced on the sub-surface of the wafer. Due to this damaged layer, the instability of the background emission spectrum and intensity in PLI observation may make it difficult to observe crystal defects in the bulk wafer.

In general, hydrogen etching has been used for SSD removal, which can be performed using a CVD furnace [10]. However, due to the difficulty in controlling the surface C/Si ratio, a macro-step bunching forms on the surface as the etching amount increases [5]. The impact of the macro-step bunching on PLI has not been verified. Therefore, we have developed Dynamic AGE-ing® (DA) as a thermal sublimation etching method that enables control of surface roughness along with SSD removal. DA sublimation etching is a technology that enables non-contact etching of the substrates

by annealing polycrystalline SiC and single-crystalline SiC substrates facing each other, using a temperature gradient as the driving force [11]. This method controls the C/Si ratio in the gas phase by the thermodynamically stable equilibrium vapor pressure at 1200-2100°C. Thus, materials introduced into a confined environment can selectively establish stable C- or Si-rich phase equilibrium environments. This stable environment allows the etching and growth process using DA to control surface roughness independent of etching depth. In this study, we performed PLI observations on 4H-SiC wafers with and without SSD and surface roughness controlled by DA etching to identify the difficulty of observation of crystal defects.

## Experiments

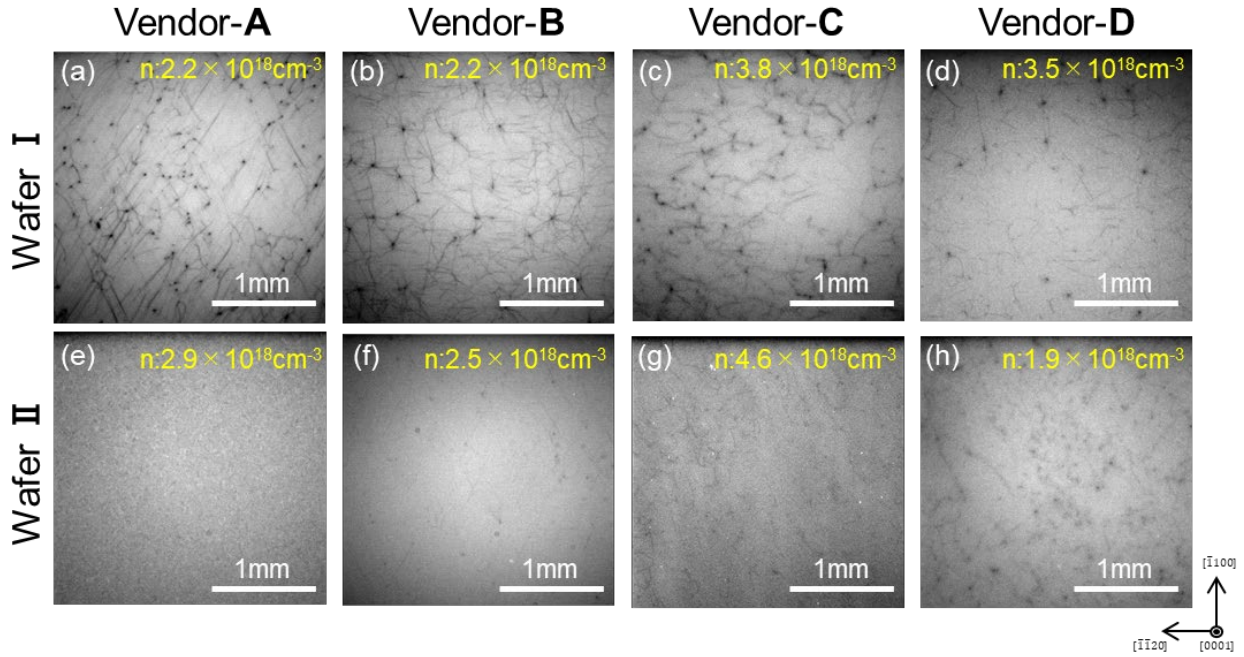
The samples were a CMP or MP-finished single crystal n-type 4H-SiC (0001) wafer tilted 4° from (0001) to <11-20>. A total of eight 6-inch wafers, two each from four different Vendor A-D, purchased after 2020 were used. These samples were etched by the DA sublimation etching of about 3 μm at 1600°C to 1800°C. A KGX-2000 ultra-high temperature high vacuum furnace manufactured by EpiQuest inc. was used for DA sublimation etching. The surface morphology was controlled by setting the DA etching environment to Si-rich and C-rich. The bare surfaces of these samples and the surfaces after DA sublimation etching were observed using PLI. The PLI-200 from PHOTON Design Corporation was used for PLI. For the PLI excitation light conditions, the light source was a Hg-Xe lamp, and the filter was a 313 nm bandpass filter. On the receiving side, the receiving filter was a 750 nm high-pass filter, a CCD camera captured the image, and the exposure time was 1 sec. The sample temperature was set at room temperature. PLI observations were squares with 2.6 mm on a side per image, which were tiled up to 6 inches. Raman spectroscopy was used to measure the carrier concentration of the samples. The surface topography was observed using low-energy electron channeling imaging (LE-ECCI) [12] at 1 kV in the SEM and AFM. For the purpose of comparison with PLI, the etch-pit method, which is a destructive inspection but is considered the most reliable for defect detection, was also performed. For the etch-pit method, the samples were soaked in KOH melt, a strong alkali, at 500°C for 6 min 20 sec. A laser microscope was used to observe the etch pits.

## Results and Discussions

A total of eight 6-inch SiC wafers, two from each of the four vendors (A, B, C, and D), were observed by PLI to investigate how different the defects visibility was seen from wafer to wafer. Fig. 1 shows the PL images of a relatively high-contrast area of defects in a wafer. The wafers from the same vendor with stronger defect contrast on the PL image were designated Wafer I, and those with weaker defect contrast were designated Wafer II. The carrier concentration of these wafers, measured using Raman, is shown in the upper right corner of each PL image. Figs. 1 (a)-(c) show clear visible dark dots of threading dislocations (TDs) and dark lines of BPDs. Fig. 1 (d) shows less contrast than Figs. 1 (a)-(c), but they are still quite visible. In Fig. 1 (h), the dislocations appear thicker and more blurred than in previous images. Fig. 1 (f) shows barely visible defects due to weak contrast. Fig. 1 (g) has significant noise in the background region where no defects exist, making it difficult to see them. In Fig. 1 (e), the contrast of the background noise is so significant that nothing resembling a defect could be observed.

These results indicate that each bulk wafer has its characteristics regarding the visibility of defects in PL images. A comparison of wafers made by the same vendor also shows that defect visibility in the PL images is very different. We also found that wafers with low defect visibility tended to have more significant noise in the background region. There was no correlation between defect visibility and carrier density. This result is inconsistent with the assertion that the reduced defect visibility of bare SiC wafers, in general, is due to too high a nitrogen doping concentration.

Next, the variation in defect visibility within a single wafer is verified. The PL images of the areas of low defect visibility within and outside the C-facet of Wafer I of Vendor-B are shown in Fig. 2. The PL image outside the C facet shows the morphology of the defects but weak contrast with the background (Fig. 2 (a)). In the PL image inside the C-facet shown in Fig. 2 (b), the background noise

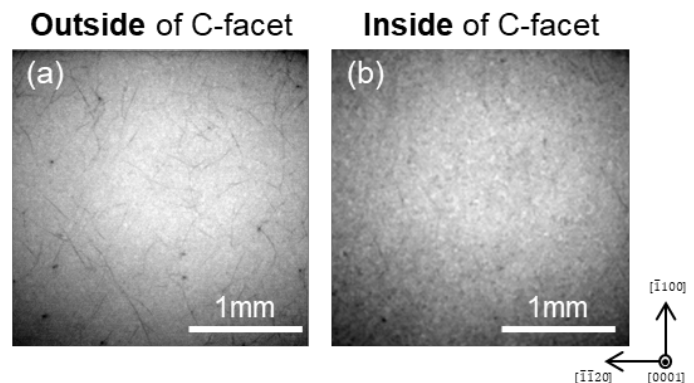


**Fig. 1.** PL images of areas with high defect visibility among 6-inch 4H-SiC wafers purchased from Vendor- (a) (e) A, (b) (f) B, (c) (g) C, and (d) (h) D. Out of the two SiC wafers from each vendor, the one with higher defect visibility was designated Wafer I, and the one with lower defect visibility was designated Wafer II.

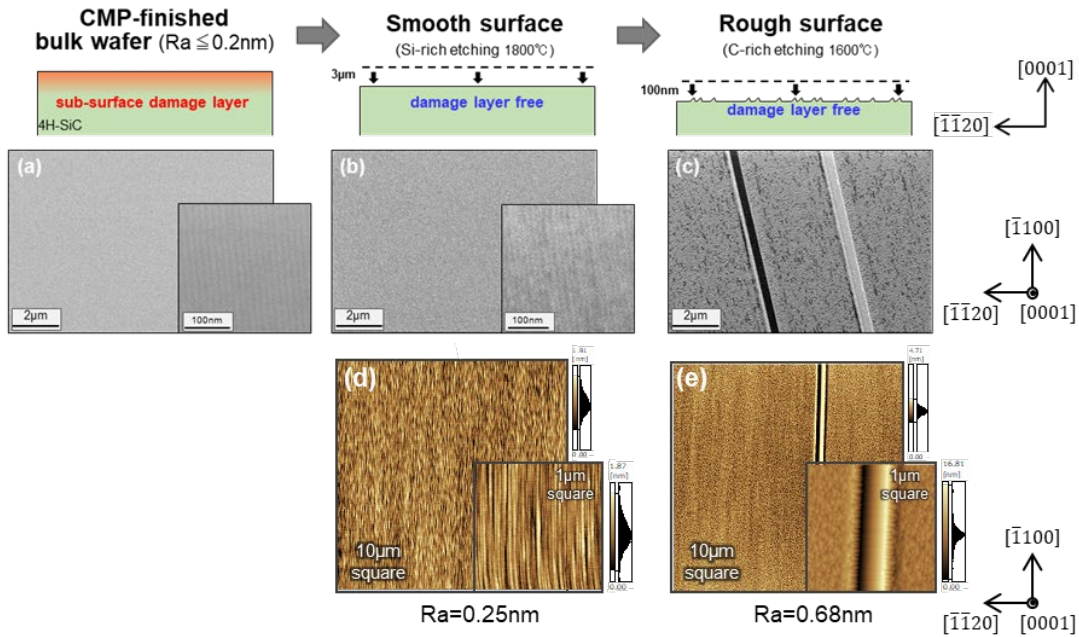
is extensive, and the contrast between defects and background is almost unnoticeable. These results show that defect visibility in the PL images varies from vendor to vendor, wafer to wafer, and even within a single wafer.

Next, the effects of SSD and surface roughness on defect observation in the PL image are examined. For the 6-inch diameter Wafer I manufactured by Vendor-B, approximately  $3 \mu\text{m}$  etching was performed by DA sublimation etching at  $1800^\circ\text{C}$  in the Si-rich environment. In addition, a  $100 \text{ nm}$  DA sublimation etching was performed at  $1600^\circ\text{C}$  in the C-rich environment. Surface SEM images of the CMP finished and after each DA sublimation etching, and AFM images after each DA sublimation etching are shown in Fig. 3. Surface SEM images after CMP and Si-rich etching showed a terrace width of about  $14 \text{ nm}$ . The SiC wafer used in this study has an off angle of  $4^\circ$ , indicating that the step height is  $1 \text{ nm}$ , the full-unit-cell height of 4H-SiC. On the other hand, macro step bunching with a terrace width of about  $500 \text{ nm}$  and moderate step bunching of  $14$  to  $60 \text{ nm}$  was formed on the surface after DA sublimation etching in the C-rich environment. AFM measurements of the surface after CMP and Si- and C-rich DA sublimation etching showed  $R_a$  values of  $< 0.2 \text{ nm}$ ,  $0.25 \text{ nm}$ , and  $0.68 \text{ nm}$ , respectively. PL images will be observed on these samples to verify the effects of SSD and surface roughness on the visibility of PLI.

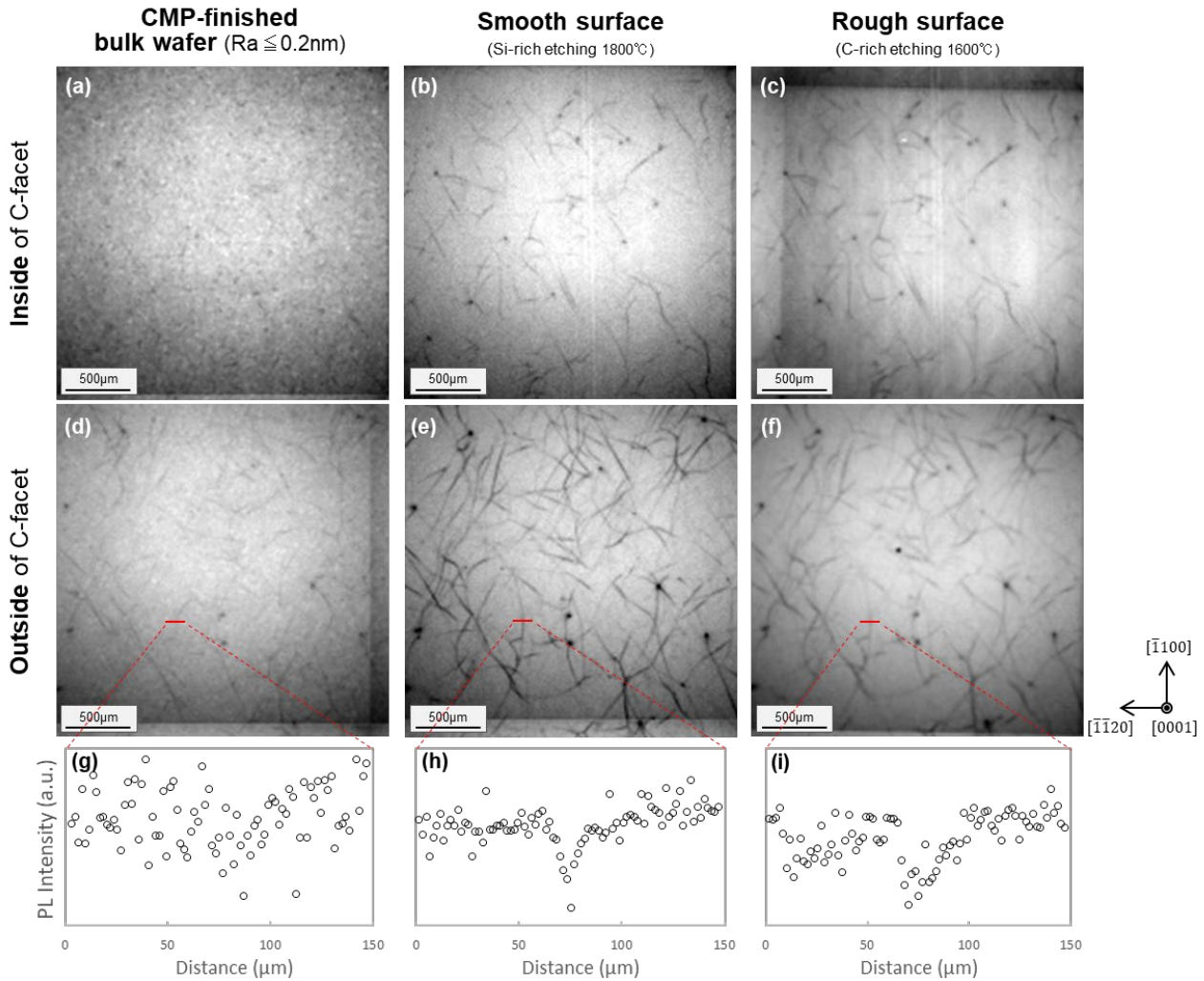
Figs. 4 (a)-(f) show the results of PLI observation after CMP and each DA sublimation etching for the inside and outside of the C-facet area of the Wafer I made by Vendor-B, cut out to be the same



**Fig. 2.** PL images of the (a) outer and (b) inner regions of the C-facet in Wafer I of Vendor-B. The areas with particularly low defect visibility are selected.



**Fig. 3.** SEM images of Wafer I from Vendor-B after (a) CMP, (b) Si-, and (c) C-rich DA-sublimation etching. AFM images of the same wafer after (d) Si-, and (e) C-rich DA-sublimation etching.



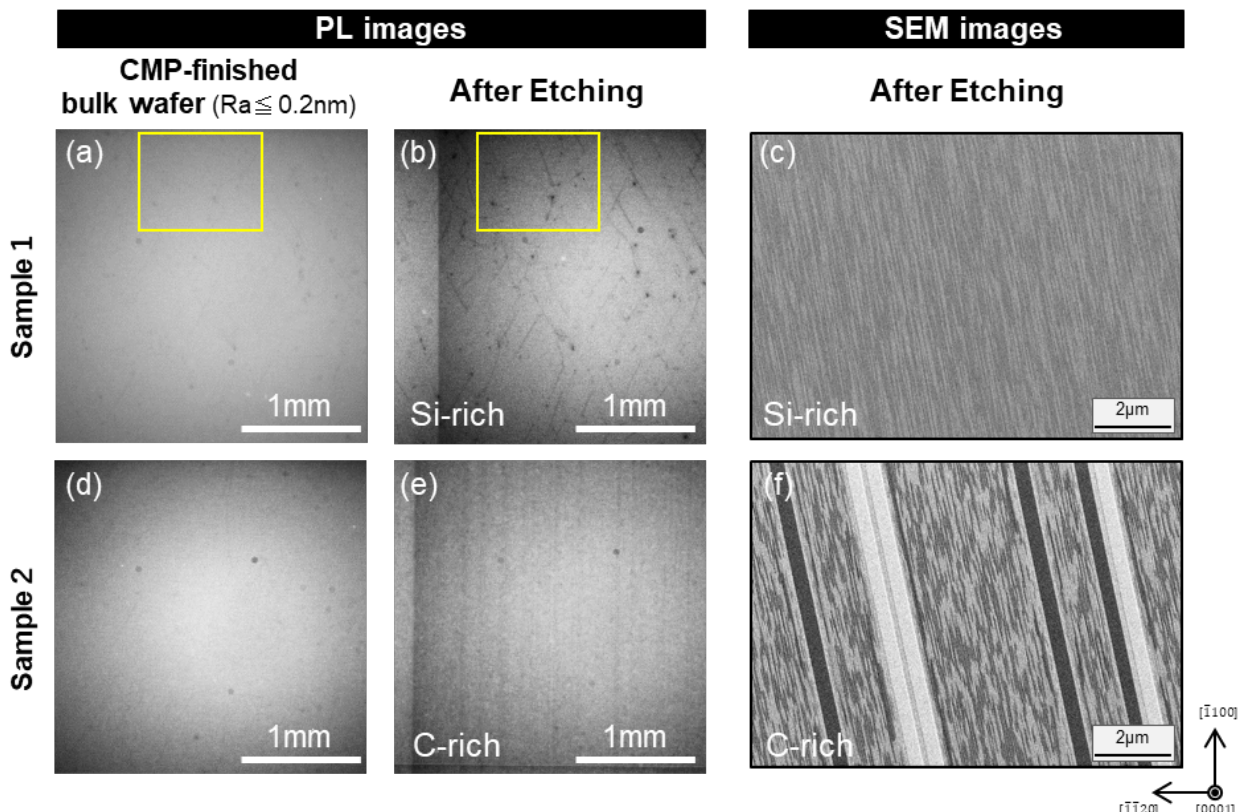
**Fig. 4.** PL images of SiC wafer after CMP, Si-rich etching, and C-rich etching at the same points inside (a)-(c) and outside (d)-(f) of C-facet, respectively. (g)-(i) is PL emission intensity profiles measured across the same BPD in (d)-(f), respectively.



point observation. The luminescence intensity profile of the PL image in the C-facet outer region, vertically straddling a particular BPD and indicated by the red line, is shown in Figs. 4 (g)–(i). The vertical scales of the luminescence intensity profiles are aligned. The PL image after CMP shows more significant background luminance fluctuations, defect-derived morphology cannot be observed within the C-facet, and defects are blurred even outside the C-facet. The luminance profile of the post-CMP PL image shows a significant variation in values in the defect-free region. The variation that appeared in the brightness profiles was also observed in the PL images on other wafers, where defect visibility has been unfavorable.

On the other hand, observation of the surface after Si-rich DA sublimation etching in Figs. 4 (b) and (e) shows a drastic reduction of background noise inside and outside the facets. This background improvement also allowed observing TDs and BPDs morphology clearly. Fig. 4 (h) after Si-rich DA sublimation etching shows a V-shaped luminance profile with a width of about 20  $\mu\text{m}$ , indicating the presence of BPD centered at 75  $\mu\text{m}$  on the horizontal axis. A comparison of the PL images after CMP and Si-rich DA sublimation etching shows that both TDs and BPDs have significantly increased defect-induced contrast and sharpened morphology inside and outside the C-facet. By comparing the luminance profiles in Figs. 4 (g) and (h), it can be seen that the decrease in luminescence intensity in the BPD areas is almost the same. However, there is a significant difference in the variation of the background luminescence intensity. The results suggest that the variation of background luminescence intensity caused by the SSD introduced on the SiC surface, which produces disorder in carrier recombination center density and crystal distortion, is responsible for the reduced defect visibility of PLI. In other words, the SSDs present on the SiC bulk wafers creates non-uniformly distributed recombination centers and distortions, suggesting that removing this layer will allow defects to be observed with PLI.

Next, with the aim of controlling only the surface topography while minimizing changes in the amount of SSD removal, wafers that had been DA sublimation etched in the Si-rich environment were further etched in the C-rich environment. The etching was performed at 1600  $^{\circ}\text{C}$  for approximately 100 nm. The PL images and luminance profiles after the etching are shown in Figs. 4

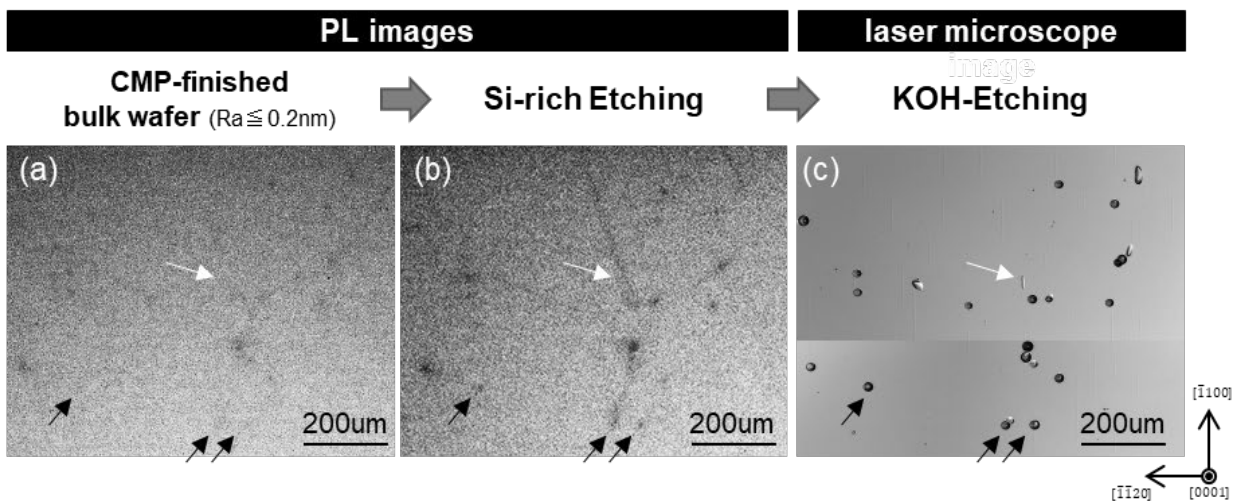


**Fig. 5.** PL images after (a) (d) CMP, (b) Si-, and (e) C-rich DA sublimation etching and surface SEM images after (c) Si-, and (f) C-rich DA sublimation etching.

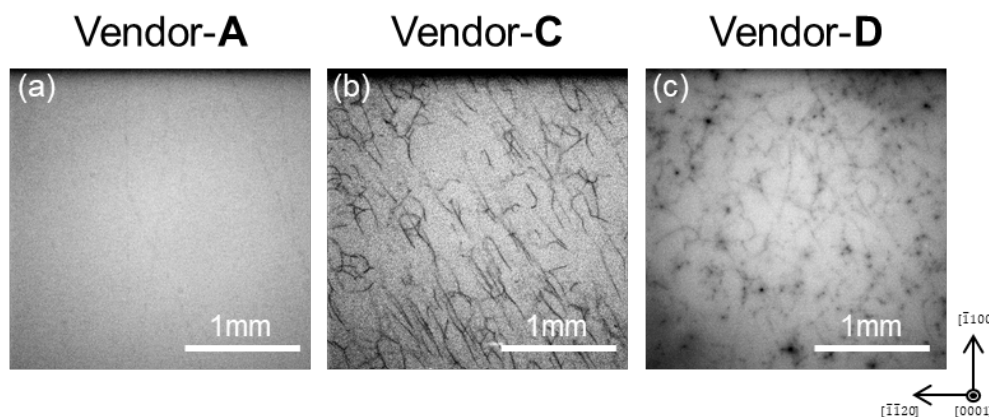
(c), (f), (i). Defect visibility inside the C-facet was not significantly different from that in the Si-rich environment, but a stripe morphology parallel to  $\langle 1-100 \rangle$  was observed in the background, which is considered to be macro-step bunching. On the other hand, outside the C-facet, the morphology of TDs and BPDs is slightly blurred, indicating that defect visibility has decreased. Two possible causes of this reduced defect visibility are differences in surface roughness and final processing temperature, which are difficult to determine based on these results alone.

Therefore, a substrate was cut out from two locations on Wafer II of Vendor-B, where the visibility of defects by PLI was close to each other. DA sublimation etching was then performed on each substrate in the Si- or C-rich environment at a processing temperature of 1800 °C and an etching depth of approximately 3  $\mu\text{m}$ . PL images before and after DA sublimation etching and surface SEM images after etching are shown in Fig. 5. SEM images of the substrate surface after DA sublimation etching in each Si- and C-rich environment showed an atomically flat surface (Fig. 5 (c)) and a surface with large and medium step bunching (Fig. 5 (f)), respectively. Figs. 5 (a) and (d) show that the PL image after CMP has equally low defect visibility for both substrates. Here, the 60  $\mu\text{m}$  diameter circular morphologies observed in Figs. 5 (d) and (e) and some others are not essential because they are dust particles adhering to the CCD camera. Fig. 5 (b) shows the PL image of a substrate subjected to DA sublimation etching in the Si-rich environment, and it can be observed that the visibility of defects has improved. On the other hand, in the case of the C-rich environment shown in Fig. 5 (e), the defect visibility remained poor despite the same temperature and etching depth with Si-rich DA sublimation etching. Surface roughness after thermal etching, even if the damaged layer is removed, may not improve the visibility of defects in the PL image or may instead degrade it. These results indicate that surface topography has a significant effect on PL images.

Next, we compare the results of defects observed by the etch-pit method with PL images, where the visibility of defects is improved by SSD removal and surface control. Solution etching was performed at 500°C for 6 minutes and 20 seconds in a KOH molten solution on samples 1 and 2, which were cut from Vendor-B Wafer II and thermally etched with DA sublimation etching. The etch-pit method revealed 190-210 BPDs and 30-40 TDs in both of the PL image areas (6.8  $\text{mm}^2$ ) shown in Figs. 5 (b) and (e). In other words, Fig. 5 (e) shows that about 230 defects that actually existed were not captured in the PL image at all. Figs. 6 (a) and (b) show magnified images of the yellow square area in Figs. 5 (a) and (b), respectively. Fig. 6 (c) shows a laser microscope image of the etch pit at the same point. The arrows indicate defects that were not visible in the PL image on the CMP surface but became visible after etching. The white arrows are BPDs, and the black arrows are TDs. Compared to the laser microscope image after KOH etching, it was found that all of the crystal defects observable by the etch pit method were observed in the PL image after Si-rich DA



**Fig. 6.** (a), (b) Enlarged view of the yellow rectangle area in Figs. 5 (a) and (b), respectively. (c) The same point laser microscope image after KOH etching at 500 °C for 6 min 20 sec.



**Fig. 7.** PL images of Wafer II of Vendor- (a) A, (b) C, (c) D after 1800°C DA sublimation etching in the Si-rich environment with etching depth of 3  $\mu\text{m}$ .

sublimation etching. Although the etch-pit method is a destructive inspection, it is one of the most reliable defect detection methods. Therefore, it is suggested that using DA sublimation etching to remove SSD on the CMP surface while maintaining surface flatness will enable reliable defect detection on PLI observation.

So far, we have used Vendor-B wafers to show the defect visualization function in the PL image by SSD removal. In order to investigate whether the same effect could be obtained on wafers made by another vendor, PLI observation was performed on Wafer II of each vendor (Vendor-A, C, and D) that was DA sublimation etched. The conditions for DA sublimation etching were a Si-rich environment at 1800°C with an etching depth of approximately 3  $\mu\text{m}$ . PL images of these wafers are shown in Fig. 7. The PL images after the etching are not precisely the same points as Figs. 1 (e), (g), and (h), but the misalignment is within 3 mm. The Vendor-A wafer, for which no contrast due to defects could be observed on the surface after CMP, remained completely invisible after etching, as shown in Fig. 7 (a). However, background noise shows significant improvement. In the case of the Vendor-C wafer, the defects were only faintly visible initially, but as shown in Fig. 7 (c), an improvement in defect visibility was observed after etching. In the case of the Vendor-D wafer, the morphology of the defects is blurred compared to the others. However, the contrast of the defect area is more significant, making it easier to distinguish individual defects (Fig. 7 (d)). In summary, defects could be visualized in the PL images for wafers made by Vendor-B, C, and D by removing the SSD layer and controlling surface roughness, but not for wafers made by Vendor-A. This result could be due to a deep damage layer on the wafer and insufficient etching depth. There are also cases where defects are difficult to observe due to factors other than the SSD.

## Summary

In this study, PLI observation was performed after thermal sublimation etching to investigate the cause of defect visibility degradation in nitrogen-doped 4H-SiC (0001) bulk wafers. In the PL image of purchased wafers with CMP finish, the visibility of BPDs and TDs varied from wafer to wafer and vendor to vendor. Predicting that SSD was one of the factors deteriorating the visibility of these defects, we performed DA sublimation etching to remove SSD while maintaining surface flatness and then performed PLI observation. As a result, the visibility of defects was significantly improved compared to the CMP-finished wafer. It was also found that surface roughness adversely affects observing defects in the PL image. As for the effect of SSD removal, defect visualization was confirmed on three out of four wafers from each vendor, but one wafer had no visible defects. Therefore, a future task is to search for the causes that make it challenging to observe defects other than SSDs. In the future, we hope to combine PLI with AI to assess the number and distribution of defects more accurately, regardless of which wafer vendor is used.

## Acknowledgments

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