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Tailored Polycrystalline Substrate for SmartSiC™ Substrates Enabling High Performance Power Devices

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Abstract. Silicon Carbide (SiC) Power Devices have emerged as a breakthrough technology for a wide range of applications in the frame of high-power electronics, notably in the 600 to 3,300V. The last decades have shown a continuous and impressive improvement in both 4H-SiC wafer size and quality. Nevertheless, the availability of such wafers remains a challenge for the SiC power industry. In the last three years, Soitec has successfully adapted the Smart Cut™ technology to Silicon Carbide, resulting in the integration of a thin layer of high quality 4H-SiC on an ultra-low resistivity 3C p-SiC handle wafer. The so-called SmartSiC™ offers a drastic yield improvement for the whole industry thanks to the multiple times re-use of the 4H-SiC donor wafer, as well as an improvement of the device's electrical performance, especially thanks to the ultra-low resistivity polycrystalline silicon carbide (p-SiC). The latter being specially developed to enhance the new SmartSiC™ substrate capabilities. In this paper, we present the work done by Mersen and Soitec to tailor the p-SiC properties, and thus the SmartSiC™ ones including such material.

Introduction

Silicon carbide is a wide band gap material with outstanding properties, including high electric field breakdown strength and high thermal conductivity that make SiC a material of choice for power devices. The latter are emerging as a key component of high-power electronics, including DC/DC converter, on board or charging station, and traction inverter for automotive among other applications [1]. SiC power electronics devices have been developed using 4H bulk wafers produced using PVT (modified Lely method) in which boules are grown at temperatures as high as 2400°C for more than a week. Such a process is known to be energy intensive, and difficult to upscale for larger wafer diameter. Also, electrical resistivity is limited to values greater than around 15mΩ.cm to limit stress and number of defects during growth and cooling.

The Smart Cut technology developed by Soitec allows the transfer of a thin layer of commercially available monocrystalline Silicon Carbide (mSiC) on a polycrystalline Silicon Carbide (pSiC) substrate, resulting in the SmartSiC™ product, see Fig. 1. The bonding interface being electrically conductive, it is thus possible to use the wide band-gap properties of the mSiC on a substrate having a ultra-low electrical resistivity, high thermal conductivity, and mechanical compatibility with the device processing such as drift epitaxy and anneal for dopant activation. One can thus understand the major importance of the p-SiC and the need to tailor its properties to enhance the SmartSiC™ substrates capabilities.

In this paper, we present several obtained 3C p-SiC microstructures obtained from different growth conditions, starting with the importance of the graphite handle substrate. We explore the importance of the microstructure for thermal conductivity, electrical resistivity, warpage and warp stability during the packaging part. For each of them, deposition conditions and Scanning Electron Microscopy (SEM) cross section are shown. While several of them show interesting behaviour and attest to a fine control of the Chemical Vapour Deposition (CVD), ultimately a regular stable and

repeatable micrometre grain size microstructure is selected for its advanced properties: high thermal conductivity, ultra-low electrical resistivity, controlled warpage during backside grinding, and suited with Soitec integration process. Finally, we show SmartSiC™ wafers characterization produced with Mersen p-SiC wafers, and the perfect compliance with SmartSiC™ final expectations in High Volume Manufacturing.

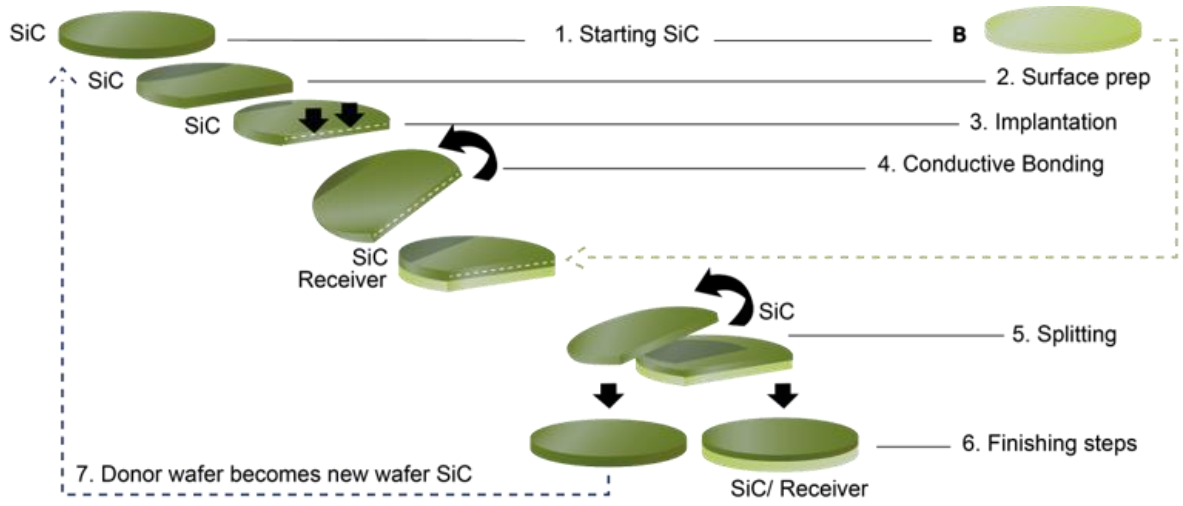

Figure 1: Smart Cut™ process description [2].

Graphite for tailored polycrystalline Silicon Carbide

The key step in the manufacturing process of the p-SiC wafer is a CVD deposition on a fine-grained and purified isostatic graphite substrate, to avoid any contamination and degassing of impurities during the deposition. To obtain a wafer with a diameter of 150mm or 200mm, the deposition is usually carried out on a graphite cylinder with a near-by diameter.

The coefficient of thermal expansion of the isostatic graphite is chosen judiciously in Mersen's portfolio to be compatible with the layer of SiC during cooling after deposition.

Graphite cylinders are loaded into the CVD deposition furnace. It consists of an enclosure which makes it possible to reach low pressures down to a minimum of a few tens of mbar by pumping gases up to an effluent treatment device. The deposition furnace is heated by induction of a magnetic field in a graphite susceptor, inside which the precursor gases (potentially silanes, alkanes, methyl-chlorosilanes), the carrier gases (potentially Hydrogen, Argon), the doping gases (potentially NH_3, amines, N_2) are introduced.

The graphite substrates are placed in thermal equilibrium inside the furnace heated by the susceptor to a temperature less than 1500°C measured by a thermocouple. The gas mixture is introduced through nozzles allowing a homogeneous distribution of the gas flow in the enclosure. In this temperature range, the deposition rates can vary widely from a few µm/h to more than 100µm/h.

When the deposition thickness on the surface of the graphite substrate is reached, the injection of the precursor gases into the furnace is stopped and the furnace is cooled down to ambient temperature to be unloaded. The graphite discs coated with a layer of SiC deposit are then processed to remove any graphite residue. A raw SiC disc is obtained from each side.

Tailored polycrystalline Silicon Carbide.

Using an usual CVD recipe, the growth morphology was typically grains with an increasing diameter as the layer was growing, thus creating a gradient of intrinsic stress capable of bending the SiC layer as it is removed from its graphite substrate. Far from reaching an acceptable flatness, the measured warp was too high, for a millimetre deposition. Thus, different paths are explored in the following to get a usable warp from a millimetre thickness deposition. In all cases, the electrical resistivity is measured with 4PP (four points method), while the thermal conductivity is extracted using a high frequency LFA (Laser Flash Anneal) at Netzsch. For the latter, low, acceptable and high

values respectively refers to values lower than 150W/(m.K), around 200-220W/(m.K), and higher than 250W/(m.K).

As described in the patent JP 3648 112 B2, alternating multiple layers with different growth conditions may create an alternated stress across the wafer thickness and thus reducing the stress moment close to zero, the deformation being strongly reduced. We applied this structure, as shown in Fig. 2a with ABABA configuration, considering A large grain size texture with a compressive intrinsic stress and B very fine texture with a tensile intrinsic stress. The multilayer structures enable it to reach low deformation, compatible with further processing. We assess the resistivity to be two times higher than a monolayer with the same doping. Thermal conductivity is measured far below the target. Because of these drawbacks, and the uncertain behaviour during backside grinding, we focus on mono-layer solutions with new growth conditions.

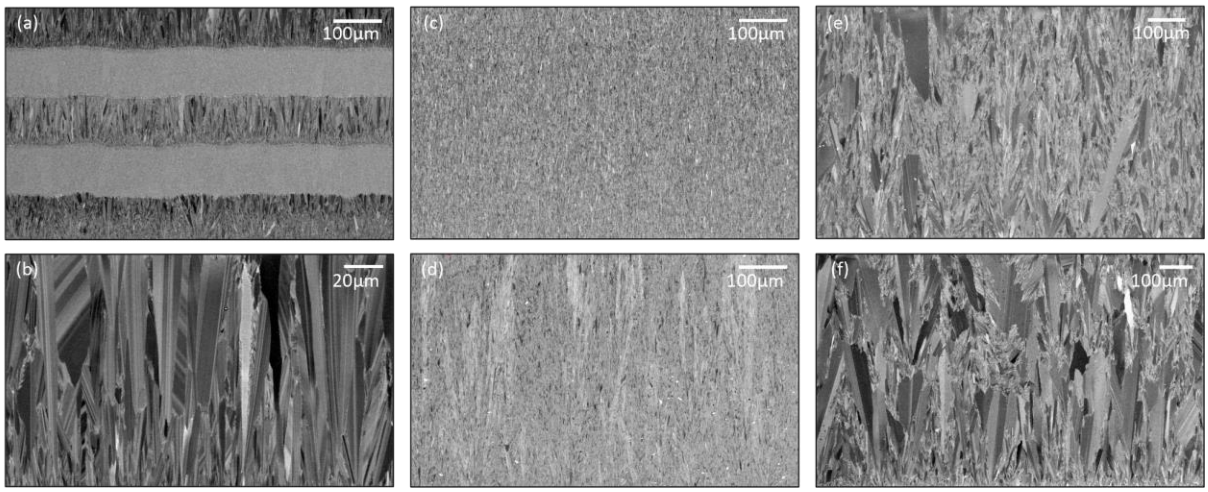

Figure 2: Cross section microstructure obtained by SEM of backscattered electrons performed (BSE) at SIMaP laboratory, on six different microstructures. In each example, the substrate is at the bottom of the image and thus the growth from bottom to the top.

In the next example, key parameters of the CVD process are modified (temperature, partial pressure of the precursor, percentage of doping gas), and it is possible to change the orientation of the deposited layer and its texture. The latters have an impact on the gradient of intrinsic stresses of the deposit, making it possible to obtain a warp on the rough disc blank conforming to the objective.

In the microstructure depicted in Fig. 2b, a layer is deposited on a graphite substrate. It was observed a continuous increase in the diameter of the grains over the first 200µm. The electrical resistivity is measured at 16mΩ.cm, and an acceptable thermal conductivity was extracted. Despite physical properties consistent with the target objective, the deformation measured on several discs is much higher than the target objective. Hence, this path was abandoned.

In the next two cases, we explore microstructures with regular grain size over the thickness. In the microstructure shown in Fig. 2.c, a layer is deposited on a graphite substrate. As wanted, grain size, in the form of fine rods very oriented along the normal to the plane of the substrate, does not increase as the growth of the p-SiC layer progresses. The deposit electrical resistivity is measured at 1.1mΩ.cm, and a low thermal conductivity is extracted, far below the target objective, as this type of fine-grained structure appears to severely limit the latter. The deformation measured on the raw disks is on the other hand very good. Another fine and regular grain size texture is explored and shown in Fig. 2d. A 5mΩ.cm resistivity, and a high thermal conductivity is obtained despite the relatively small grain size and high doping level in the p-SiC layer. Moreover, the deformation measured on the raw disc is also very good, before any wafering proceeding, showing a good compatibility with p-SiC warp below 50µm.

Two other cases are explored, one with a texture with predominantly fine grain mixed with coarse grain, and the other with texture with a majority of coarse grains mixed with a fine texture of small grains. The first case is depicted in Fig. 2e, a layer was deposited. One can observe two grain size populations: the fine grains have a diameter between 1µm and 10µm, while coarser grain

populations have a conical shape whose diameter can increase up to 50µm. As the large grains remain a minority in the texture, the average grain size stabilises rapidly. An electrical resistivity measured at 3.3mΩ.cm, while an acceptable thermal conductivity is obtained. The average raw disc warp is compatible with the ultimate warp target for p-SiC wafers. The second case presents, see Fig. 2f, a deposited layer on a graphite substrate. We observe very large grains of conical shape with diameters that can reach up to 100µm, and in a minor proportion few small grains of size less than 10µm. Moreover, a continuous increase in the grain size, and thus an unstable microstructure is observed in the first 500µm. The resistivity is measured at 0.9mΩ.cm through 4PP, and we obtain a low thermal conductivity. The average deformation was incompatible with further processing.

Finally, this work enables a tailored polycrystalline silicon carbide microstructure, with an ultra-low resistivity and a high thermal conductivity that is to say <5mΩ.cm and a thermal conductivity above 250W/(m.K). Furthermore, a particular attention was put on selecting a stable and repeatable microstructure compatible with HVM manufacturing.

A tailored material for SmartSiC™.

The wafer obtained with this tailored polycrystalline silicon carbide material was then investigated through different angles. The first of them was the local flatness of the wafer after a standard wafering at NovaSiC™. We observe an improved property on such property, as shown with the max in the Fig. 3a comparing the SFQR 95% of p-SiC vs. standard 4H-SiC m-SiC wafers.

Another important aspect of the p-SiC wafers is their geometry stability during backside grinding. In fact, once the epi-drift is done and the devices made on the m-SiC side of the SmartSiC™ wafers, the packaging can require a thinning to 180µm if not less. In Fig. 3b, we present the average warpage of p-SiC and m-SiC wafers at 350µm and 180µm. One can observe a warp reduced by more than two of the ultra-low resistivity p-SiC wafer, conferring an advantage for the packaging steps of the SiC industry.

Geometry stability of the wafers during the process were also investigated. In Fig. 3c, we demonstrate with the warp values of the incoming p-SiC wafers and the corresponding SmartSiC™ wafers that the warp is constant, if not slightly decreasing for the highest values.

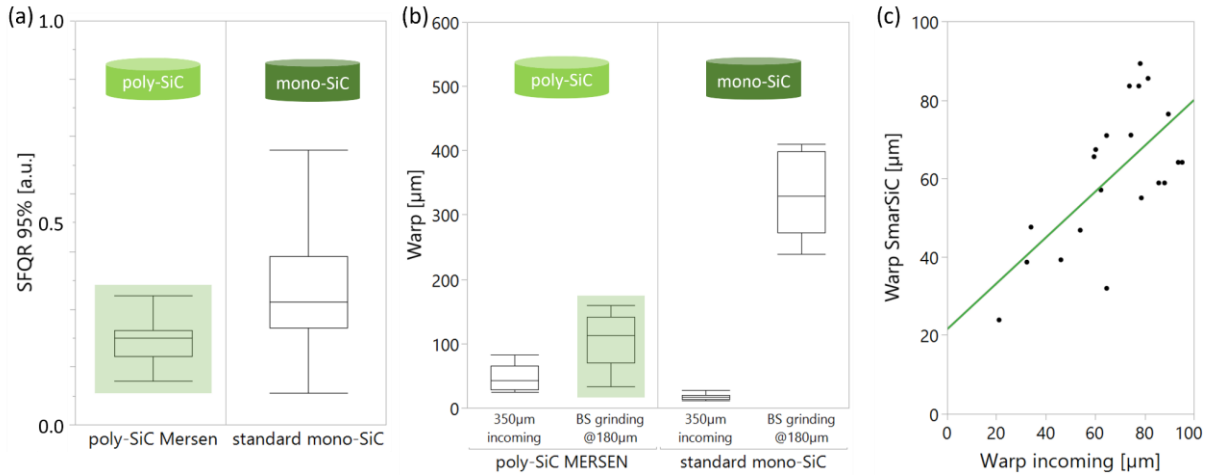

Figure 3. (a) MaxSFQR 95% measurements on p-SiC Mersen vs. standard m-SiC wafers, using 10x10mm² spot size. (b) Warp evolution during BS grinding from 350µm to 180µm on Mersen p-SiC wafers on the left, and on standard mono-SiC wafers on the right. (c) Comparison of the p-SiC incoming warp at 350µm and the corresponding SmartSiC™ product warp.

SmartSiC electrical characterization.

As explained above, ultra-low electrical resistivity of the poly-SiC wafers are a key added value of our SmartSiC™ product, as it results in a major value, that is the decrease of the Ron of the SmartSiC™ wafer, and thus less conduction loss. Moreover, when considering a 20mΩ.cm standard 4H-SiC wafers and a 5mΩ.cm p-SiC wafer, with a bonding interface <0.05mΩ.cm², the total specific

resistance is decreased by more than 3, going from 0.36mΩ.cm² to <0.10mΩ.cm². For the SiC power industry, the outcome is the ability to get higher current rating devices, or smaller dies for the same current. Resistivity mapping of state-of-the-art 150mm and 200mm Mersen p-SiC wafers are depicted in Fig. 4.

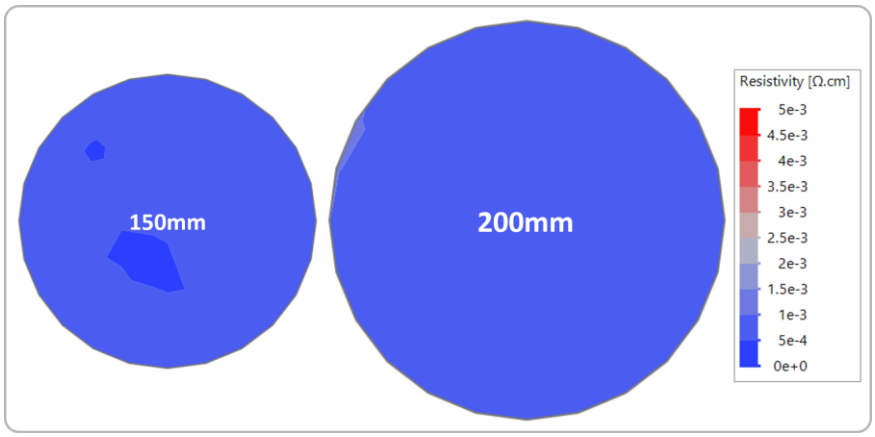

Figure 4. 150mm and 200mm p-SiC bulk substrate resistivity mapping. Measurements were done using 4PP.

Another outcome of the ultra-low resistivity of the p-SiC part of the SmartSiC™ wafers is the simpler backside contacting after metallization, as shown in Guiot et al. [3]. We observe that without any laser annealing on the back side of the substrate, the back side sheet resistance on p-SiC is 10 times lower.

Electrical characterizations were performed on SmartSiC™ substrates including Mersen p-SiC wafers, using the same methodology as in [4]. As shown in Fig. 5b, the I(V) characterization demonstrates an ohmic contact in the 4H SiC and 3C p-SiC interface. For a bulk interface resistivity extracted to be between 2.2 – 2.7 mΩ.cm on this p-SiC, the interface is in between 7.10^{-6} – 1.10^{-5} Ω.cm². Thus, ultra-low electrical resistivity is confirmed, showing the excellent compatibility of this composite substrate with the power application for which it is intended.

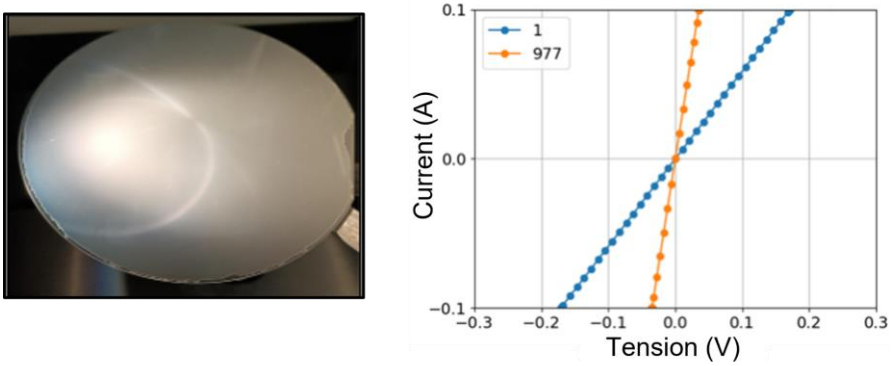

Figure 5. (a) Photography of a SmartSiC™ wafer with Mersen p-SiC wafer. (b) I(V) measurement showing Ohmic behaviour and resistivity <0.05 mΩ.cm².

Conclusions

We have demonstrated that the SmartSiC™ engineered substrate is key assets for the SiC power industry, with a proven high crystal quality and ultra-low electrical resistivity. Moreover, the multi time re-use of the standard 4H m-SiC substrate, keeping its crystal quality, enables cost-effective manufacturing, as well as a drastic increase of the supply for the industry. Finally, a pilot line is currently producing 150mm and 200mm, and a new fab will be running live 2023 at Soitec to produce such products [5].

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