Solid State Phenomena
ISSN: 1662-9779, Vol. 344, pp 53-57
doi:10.4028/p-qymc38

Submitted: 2022-10-14
Revised: 2022-11-10
Accepted: 2022-11-25
Online: 2023-06-06

Study on Estimation of Device Yield in Non-Epitaxial 4H-SiC Material Relating to Defect Densities Influencing Bipolar Degradation with XRT- Measurements

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Keywords: Bipolar Degradation, Semi Insulating, Yield, XRT, BPDs

Abstract: Commercially available 4H-SiC substrate quality has improved over time, and this has extensively reduced defect concentrations in the active epitaxial layer, during epi growth conditions at the interface. The objective of this work is to investigate bulk crystal quality for the purpose of future vertical power device fabrication in exfoliated, non-epitaxial, undoped material layers. Mathematical estimations on the device yield fraction, that is immune to bipolar degradation for the suggested future process were calculated based on XRT measurements to detect BPD and TSD densities on donor substrates. The full wafer BPD density maps of on-axis semi-insulating wafer substrates from two vendors were compared.

Introduction and Motivation

The basic motivation for this study originates from our proposal to fabricate a novel type of engineered substrate, which is fully device-ready rather than just epi-ready. The process steps of fabrication of such type of substrates are illustrated in Fig 1. The necessary voltage sustaining active layer is made of a vanadium free semi-insulating (SI) substrate wafer to subsequently form an engineered substrate, step 1 in Fig. 1. The key aspect of the suggested process is to use energy-filtered high energy ion implantation (EFII) [1] for doping the device's active voltage sustaining layer with high precision and customized vertical dopant profiles, step 2 in Fig. 1. This layer is then exfoliated using deep hydrogen implants and then bonded to a highly conductive substrates that is termed here as acceptor wafers, steps 3 and 4 in Fig. 1. Device reliability depends on the defect structure of the active region that is exfoliated form the donor wafer. It is suggested to utilize semi-insulating SiC substrates or ultra-high quality, unintentionally doped 4H-SiC substrates as a potential alternative material for replacing epitaxial processes. SI 4H-SiC material has shown promising material characteristics capable of fabricating SiC power devices using ion implantation by doping drift regions [2][3]. Extending this approach to MPS-diode and MOSFET production, would significantly reduce manufacturing time, energy consumption and cost per wafer. This work intends to motivate from defect concentration point of view the feasibility of an epitaxy-free engineered substrate by using SI material. In this approach, to exfoliate the useful material from substrates, such defect concentration per unit volume is necessary to be well understood. Conventionally, defect densities in bulk substrate materials are quantified in terms of area density in [cm^{-2}]. In this paper we explore and estimate the device yield corresponding to on-axis cut SI material based on killer defect densities like

basal plan dislocations (BPDs) [4] and threading screw dislocations (TSDs). With respect to the suggested (0°-off axis) novel engineered substrate, defect concentrations are to be quantified with respect to standard (4°-off axis) vertical active device dimensions. Rather than just using the conventional defect concentration quantification per unit area, volume concentrations are measured by transmission XRT and normalized to [$cm^{-2}*\mu m^{-1}$]. Since BPDs will be geometrically arranged parallel to the substrate surface, which is illustrated in the Fig 2. The effective defect density per cm^2 after exfoliation will be a function of defect distribution over the wafer thickness. Hence the defect concentration in each exfoliated layer for a given voltage class (layer thickness) is lower than the overall areal density that is conventionally measured. Most common SiC power devices like PN diodes and MPS diodes (merged PN-Schottky) active region thickness correspond to their respective voltage class. In this paper 600V devices are considered for estimations.

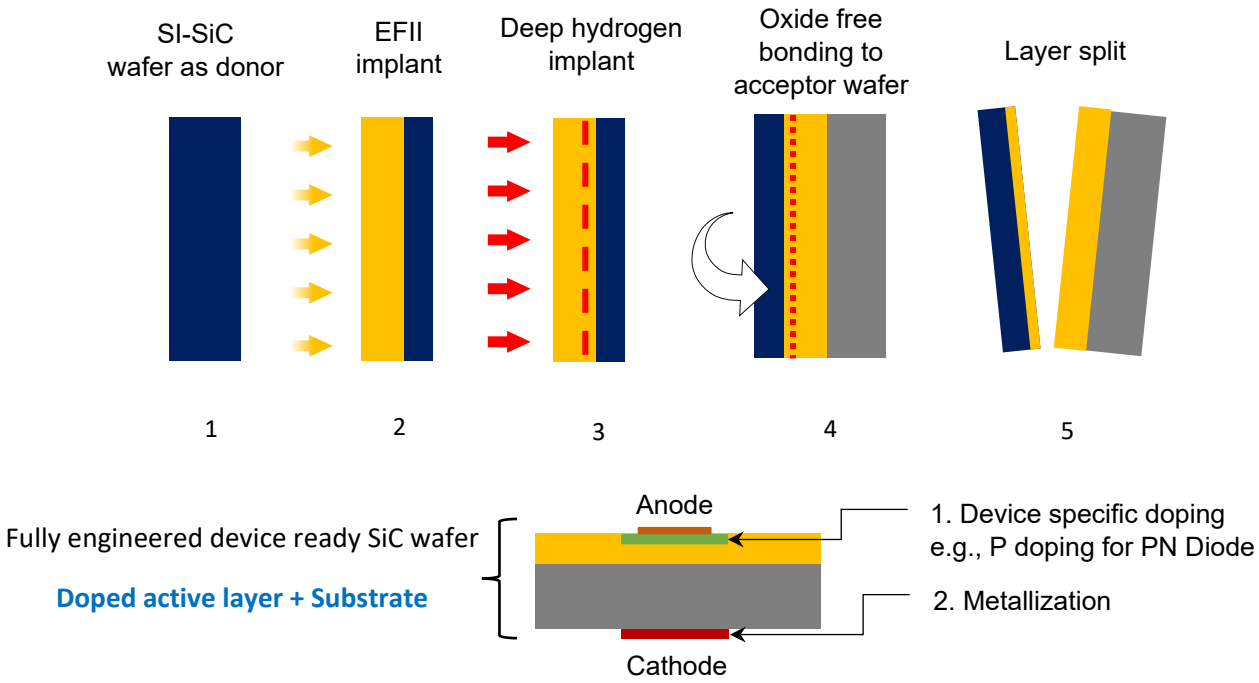

Figure 1. Top: Illustration of the fabrication process for Fully Engineered Device Ready SiC Substrates. Bottom: Example of simple p-n diode device on Fully Engineered Device Ready SiC Substrate.

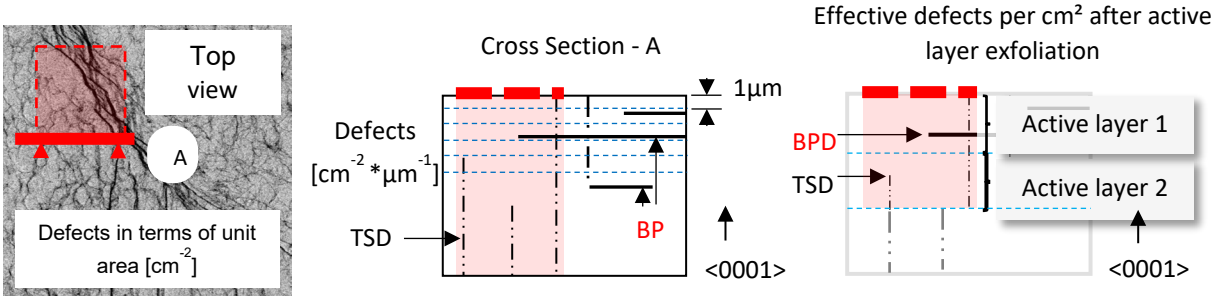

Figure 2. Illustration of need for converting areal defect densities into volumetric density.

Mathematically device yield can be estimated based on standard yield models, which consider the defect distribution in the wafer. Establishing a relationship between defect densities which influence bipolar degradation and considering the practical chip size can be used to obtain the yield calculation model that can act as a guiding information for yield analysis in this study. The yield equations that are used in this work are mentioned below, where Eq. 1 is taken from the theoretical model of Seed [5] and Eq. 2 is the empirical model of Moore [5]. A is the area of chip in cm^2 and D is defect density in cm^{-2}.

$$Y_{Seed} = \frac{1}{1+AD}. \quad (1)$$

$$Y_{Moore} = e^{-\sqrt{AD}}. \quad (2)$$

Measurement and Samples used

X-ray topography (XRT) was used to measure BPD as well as TSD densities and their lateral distributions on 150 mm substrates with edge exclusion of 5 mm. XRT was performed in transmission mode with (11-20) reflex to obtain BPDs and (0008) reflex to obtain TSDs. Transmission XRT measurements yield information about the volumetric BPD density, which can be transformed into the more common etch pit density using a constant factor depending on the offcut of the wafer [6]. Two types of wafers were considered for the measurement. On-axis semi-insulating 4H-SiC wafers. The on-axis wafers were compared between two vendors A and B. BPD defect maps of both vendors are represented in Fig. 3 below.

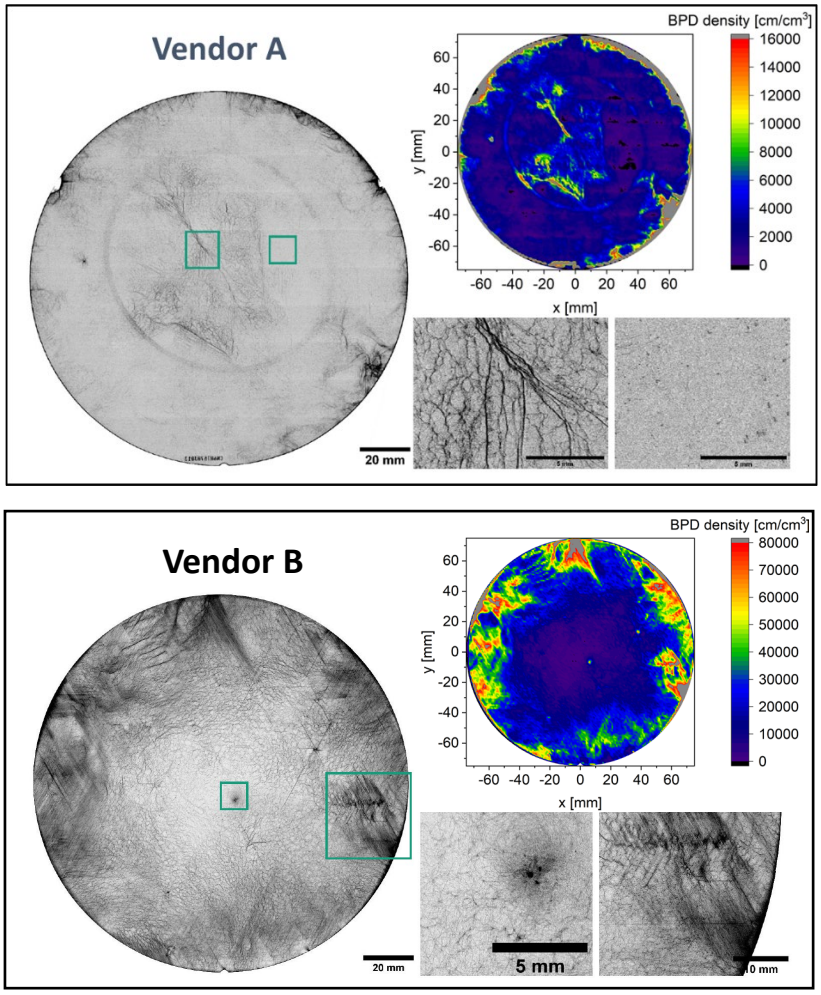

Figure 3. XRT measurements of full 150 mm wafer from Vendor A and B showing mean BPD densities of 3500 cm/cm³ and 27160 cm/cm³ respectively and lateral defect distribution in the wafer. The scales are normalized to unit cm³.

The BPD measurements of whole wafer and their lateral distribution map reveals the defect clustering and networks. In case of TSDs they have significantly lower influence on bipolar degradation in comparison to BPDs and the average TSDs in all the wafers were in similar range of 300-500 cm^{-2} and are hence excluded for yield calculations [7][8].

Results and Discussion

We witness the defect distribution is different among the vendors but similar within each vendor. The estimation of yield was calculated using both Seed's yield model and Moore's yield model. The former is a theoretical model whereas the latter is an empirical model which considers realistic practical cases. Hence, Seed's yield model was chosen for calculations and compared with empirical Moore's yield model. Fig.4 is plotted by converting areal defect concentration to volume concentration [$cm^{-2}*\mu m^{-1}$] with the chosen yield models. Chip sizes ranging from 0.01 cm^{-2} to 1 cm^{-2} are plotted to obtain the practical estimations.

The obtained mean BPD measurement values were input in Eq. 1 and Eq. 2. This results in the estimation of yield in percentage of chips that are immune to bipolar degradation caused due to the presence of BPDs. Practically the power device active area is ranging from approx. 0.05 cm^{-2} to 0.8 cm^{-2}, with suitable trade-off in designing device dimensions during the fabrication process. We can see that Seed's yield model result in higher percentage yield compared to Moore's model as the defects are strongly clustered and majority of wafer area has significantly lower defect concentration which was revealed in XRT defect maps. Thus Seed's model is more in line with the XRT images of the wafer.

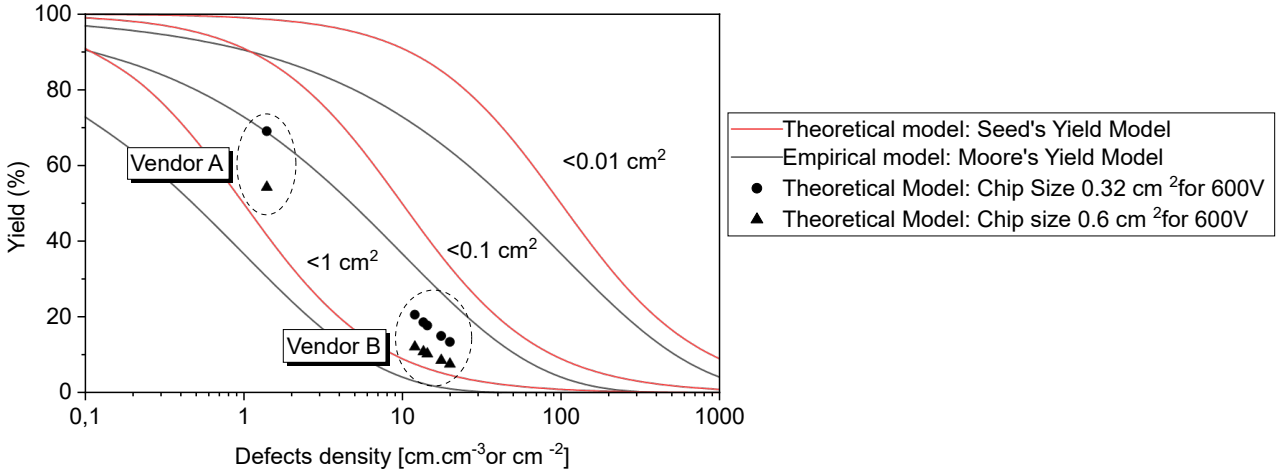

Figure 4. Normalized conversion of 2D defect density to 3D defect density gives a realistic yield estimation of power devices based on calibration data from off-axis wafers per exfoliated layer of 4µm thick.

The calculations imply that, there exist ~**0.35** cm BPD per (cm^2.µm) volume as mean value in the 500µm thick SI wafer. When the areal defect densities in the top 4µm of the wafer is compared to its full 500µm wafer XRT image, certain regions have higher and other regions show lower density post exfoliation illustrations. This proves that these planar dislocations are non-uniformly distributed along the thickness of the wafer.

Table 1. Yield calculation on two wafer vendors considering 4µm of exfoliated layer.

Wafer Vendor	Mean BPD density [cm/cm³]	BPD Density [cm/(cm²µm)]	Die Area [cm²]	Device Yield [%]	No. of wafers measured
Vendor A	3500	0.35	0.32	~69.03	1
Vendor B	27160	2.71	0.32	~22.3	5

The comprehensive data of measured defect densities and calculated yield corresponding to die area is tabulated in Table 1. The chips from best quality wafers with 4µm material will statistically consist of 1.4 cm^{-2} BPDs. This brings up the question on the threshold length of BPDs that results in bipolar degradation, which stays unanswered.

Summary

Overall, the measurements clearly show that the wafer of vendor A is nearly free of BPDs in large areas. The XRT measurements reveal this fact accordingly. Based on the yield results we see better quality on-axis wafers from Vendor A yields over 65% on reliable power device corresponding to bipolar degradation that are manufactured with the novel process for engineered substrates. These results will be used as a reference in development of the epitaxy-free device ready engineered 4H-SiC substrates for future work.

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