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Investigation of Potential Impact of Nitridation Process on Single Event Gate Rupture Tolerance in SiC MOS Capacitors

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Abstract. Single Event Gate Rupture (SEGR) is one of the catastrophic failures caused by heavy ions in power MOS devices. In this study, n-type SiC MOS capacitors representing the gate structure generally used in SiC power MOSFETs were used to conduct heavy ion irradiation tests to clarify the SEGR mechanism. The Linear Energy Transfer (LET) dependence of the critical electric field (E_{cr}) for these capacitors was evaluated with two different oxidation processes in accumulation to confirm whether the oxidation process affects SEGR tolerance. We found that the E_{cr} value and slopes of the LET dependence for SEGR between DRY samples and DRY + POA samples were approximately consistent. We also simulated SEGR and studied its mechanism. The simulation results suggested that SEGR for SiC MOS capacitors is caused by carriers in electron-hole pairs generated by a heavy ion instead of gate electric field fluctuation.

Introduction

SiC power devices have been expected for various rad-hard applications recently due to their excellent physical properties [1]. SiC devices have inherently higher radiation tolerance than Si devices because the electron-hole pair creation energy (E_{eh}) of SiC is more significant ($E_{eh(SiC)}$ = 6.88 eV) in comparison to that of Si ($E_{eh(Si)}$ = 3.63 eV) [1]. However, as a matter of fact, several issues have been associated with SiC MOS devices under harsh radiation environments. In particular, a catastrophic failure caused by heavy ions in power MOS devices is known as Single Event Gate Rupture (SEGR). This event occurs after a single energetic particle collides with the gate, resulting in dielectric breakdown and conducting a path through the gate oxide. SEGR in Si MOS devices have been studied in the past [2-4]. Regarding SEGR in SiC MOS devices, Deki *et al.* has conducted research on SEGR susceptibility for SiC MOS capacitors as a function of Linear Energy Transfer (LET) with different conditions of gate oxides [5, 6]. The study suggests that SEGR susceptibility was affected by the semiconductor material. However, it remains unclear specifically how heavy ions give rise to SEGR.

Lately, post-oxidation annealing (POA) in nitric oxide (NO) atmosphere has been the standard process in SiC MOS devices. Such an atmosphere reduces interface state density and improves effective channel mobility [7]. In this paper, we investigated the effect of gate nitriding annealing on the critical electric field (E_{cr}) for SiC MOS capacitors to confirm the influence of oxide qualities for SEGR and carried out two-dimensional simulations for SEGR to examine the physical phenomenon in the capacitors.

Experimental

Devices under the test. MOS capacitors on n-type SiC material fabricated in the National Institute of Advanced Industrial Science and Technology (AIST) [8] were used in this study as shown in Fig. 1. An epitaxial layer of 10 µm was grown on an n-type 4H-SiC substrate with a doping level of 1.0 x 10^{16} cm^{-3}. A gate oxide layer was thermally grown on the epitaxial layer to a thickness of 40 nm by two different processes: 1) dry oxidation at 1,200 °C (hereinafter called "DRY samples"); 2) dry oxidation at 1,200 °C and post-oxidation annealing in NO atmosphere at 1,350 °C (hereinafter called "DRY + POA samples"). Finally, an n-type poly-Si film of 0.3 µm was deposited on the gate oxide to form the gate electrode with a diameter of 600 µm. This structure is representative of the gate structure generally used to fabricate the planar type of SiC MOSFETs.

Figure 2 shows the typical capacitance-voltage characteristics of the SiC MOS capacitors used in this research. The flat-band voltage (ΔV_{FB}) was estimated from High-Low C-V measurements: the ΔV_{FB} of the DRY sample was -1.2 V and that of the DRY + POA sample was +0.35 V.

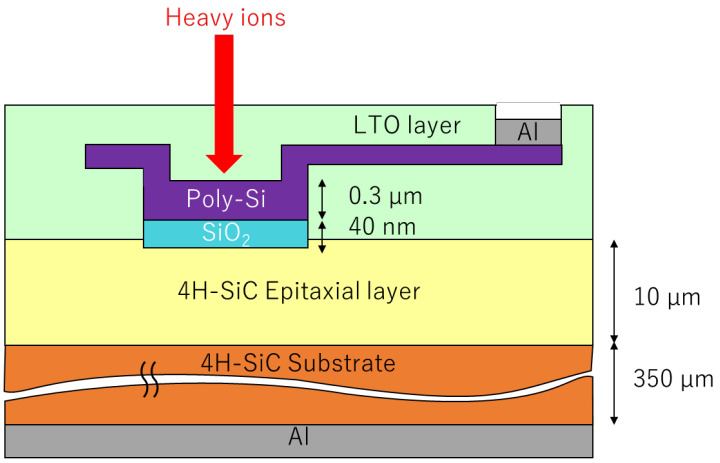

Fig. 1. Simplified cross-sectional view of SiC MOS capacitor used for this study.

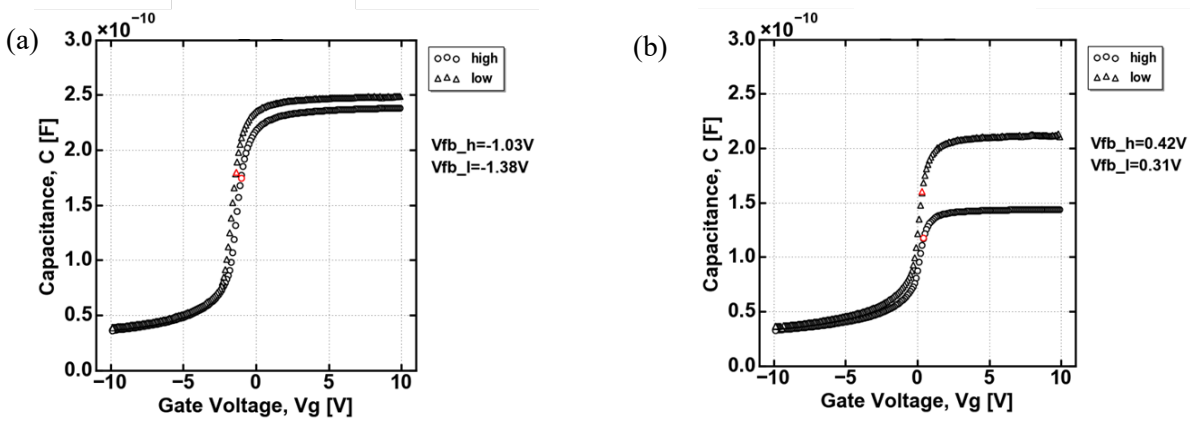

Fig. 2. Typical initial C-V curves of (a) DRY sample and (b) DRY + POA sample in this study.

Accelerator Facilities and Heavy ions. Mono-energetic heavy ions were obtained from the Cyclotron at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA), the National Institutes for Quantum Science and Technology (QST). The characteristic parameters for the ions

incident on the capacitors were calculated using SRIM [9] and are shown in Table I. The ion ranges are sufficient to pass through the oxide and epitaxial layers of the MOS capacitors.

Test conditions. The leakage current was continuously monitored and recorded during irradiation. The applied voltage was increased in 0.2 V steps from 10 V up to a cumulative leakage current density over 1 A/cm^2. The ions were irradiated normally to the device chip surface, and their fluence at each voltage step was adjusted to approximately 700 cm^{-2} (the flux was around 100 cm^{-2}s^{-1}) in order to avoid accumulation effects and allow more than one shot of heavy ions to enter the device at each voltage step. All these experiments were performed at room temperature.

Table I. Ion characteristics incident on SiC calculated by SRIM.

Facility	Ion species	Energy [MeV]	LET of SiC surface [MeV/(mg/cm^2)]	Range in SiC [μm]
TIARA	Xe	398	73.0	23.3
	Kr	289	42.7	24.8
	Ar	137	16.7	23.9

Results and Discussion

Irradiation test results. Figure 3 shows the leakage current density as a function of the electric field for the MOS capacitors under non-irradiation and irradiation with several ions in accumulation conditions. Note that the effect of ΔV_{FB} was considered in electric field values in Fig. 3. The initial leakage current density of DRY samples irradiated with Xe and Kr ions was higher than the non-irradiation characteristics due to the difference in the measurement system, not the effect of irradiation. It is notable that no difference in breakdown voltage due to different measurement methods has been confirmed. The values of the E_{cr} for DRY samples irradiated with Xe and Kr ions were similar to prior work [6].

Two surges in the leakage current density were observed in both DRY and DRY + POA samples when irradiated with high LET Xe and Kr ions; an increase in current density was confirmed with Ar ions. To elucidate which surge is SEGR, we carried out a failure analysis of the capacitor irradiated with Xe ions until the leakage current suddenly increased for the first time (the leakage current

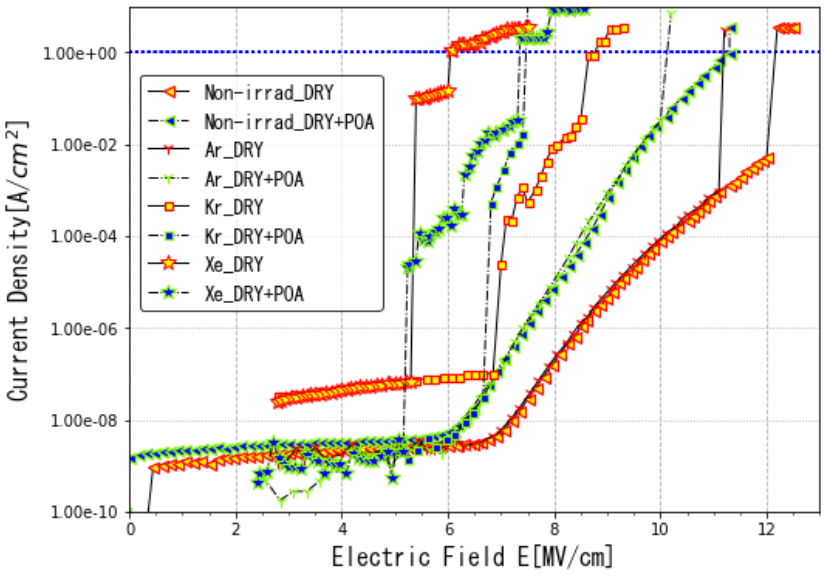

Fig. 3. Leakage current density as a function of electric field for the capacitors with and without nitriding annealing.

reached around 1.5 uA). As a result, the gate rupture in SiO_2 was confirmed inside the capacitor as shown in Fig. 4 (the details will be described later); the result provides the evidence that first current increase is SEGR in the capacitors. After the first current surge namely SEGR occurred, the leakage

current increased depending on the applied voltage. Eventually, the current density of the gate electrode reached a sufficient value for thermal destruction (approximately 10 mA/cm^2 or more), resulting in the second current increase.

Although the E_{cr0}, which is the electric field of non-irradiation capacitors of the DRY sample was higher than that of the DRY + POA sample, the E_{cr} of SEGR was comparable with the DRY + POA samples as shown in Fig. 3. This indicates that the nitriding annealing processes have little or no effect on the tolerance of SEGR. Figure 5 is the plot of the inverse electric field ($1/E_{cr}$) at several LET values for the SiC MOS capacitors in this study in the same manner as [6]. Linear proportionality of $1/E_{cr}$ - LET and the same slope was obtained for both capacitors. The above is a representation that the LET dependence of E_{cr} was consistent regardless of the oxidation process, supporting the conclusion that SEGR susceptibility would be affected by semiconductor material rather than oxide in previous studies [5, 6].

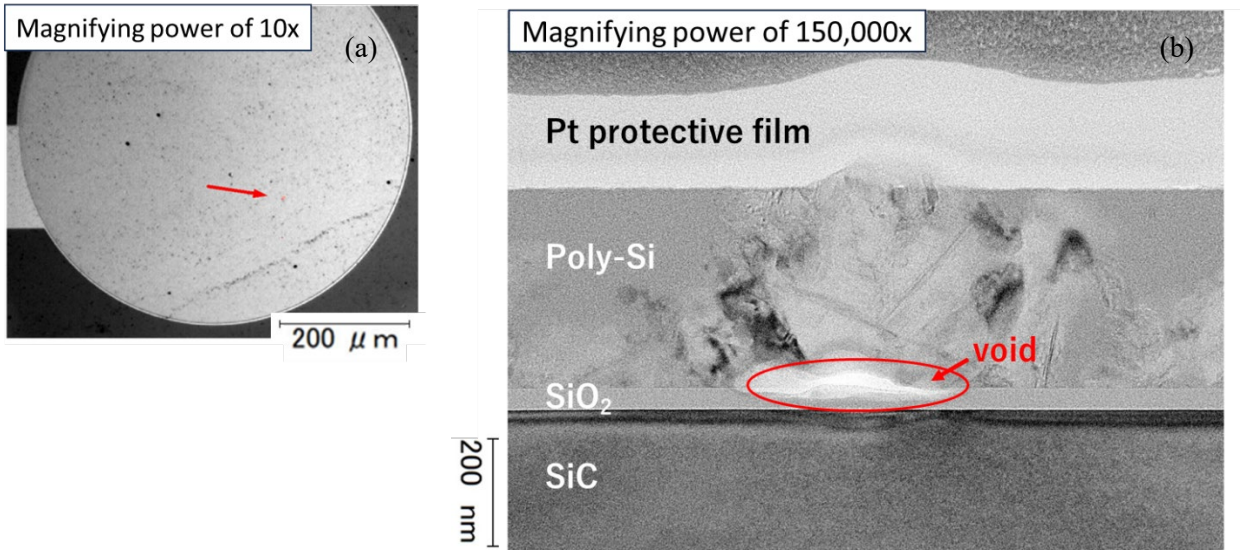

Fig. 4. Failure analysis of the capacitor after irradiated Xe ion until the current suddenly increased for the first time. (a) Emission analysis image inside the capacitor and (b) TEM image at the spot of destruction.

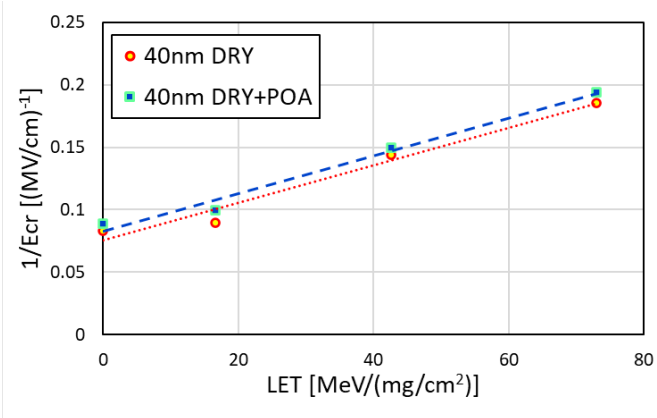

Fig. 5. LET dependence of electric field of SEGR for the SiC MOS capacitors in this research.

Failure analysis. A failure analysis by Transmission Electron Microscope (TEM) at the emission point inside the capacitor in Fig. 4(a) showed no failure in the SiC layer. However, a void was formed at the interface between the poly-Si and SiO_2 layers, as shown in Fig. 4(b). These results suggest that melting occurred at the Poly-Si / SiO_2 interface due to localized high temperature by heavy ions. The SiC layer did not melt because SiC has a high melting point. Figure 4(b) also shows that the crystallinity of the Poly-Si layer at the damage site was better than that of the non-destructive Poly-

Si layer, and the center of the damaged Poly-Si layer was raised because the Poly-Si layer was locally heated to a high temperature as previously stated.

This analysis suggests that the stress caused the Poly-Si / SiO_2 interface to generate cavities when the SiO_2 layer melted, and the Poly-Si layer was raised. At the same time, the SiO_2 layer on the side of the void was compressed and became thinner, resulting in increased tunneling gate leakage current. It is necessary to clarify the process that led to such destruction after heavy-ion irradiation through simulations.

Simulation for SEGR. The simulator used in this study was TCAD by Sentaurus. The transient response when a heavy ion hit the SiC MOS capacitor applied positive gate voltage was calculated. Figure 6 shows the simulation results of the gate electric field, the electron-barrier tunneling and the hole-barrier tunneling as the function of elapsed time, respectively. Figure 7 also shows the gate leakage current as the function of elapsed time. Input parameters of the simulator were set based on the condition when SEGR occurred in the test samples. Because no increase in the gate electric field was observed in Fig. 6, SEGR is considered not to be caused by gate electric field fluctuation. On the other hand, the gate leakage current increased immediately after being irradiated by a heavy ion in Fig. 7, suggesting that SEGR occurs due to the tunneling current. As shown in Figure 6, a rapid increase in the amount of hole-barrier tunneling due to a heavy ion was confirmed, indicating that the hole-tunneling current contributes to the increase in the gate current. An Ar irradiation test of DRY + POA samples in the same manner as in Fig. 3 was performed at a fixed 42 V, near the breakdown voltage of Ar. SEGR occurred when 60 shots had been done. These results suggest that the SEGR mechanism is similar to time-dependent dielectric breakdown. Besides, Fig. 7 also shows the value of tunneling gate leakage current with avalanche was the same as without the use of avalanche mode at the gate Poly-Si, SiC, and anywhere in the capacitor. Therefore, the tunneling current was attributed only to carriers in electron-hole pairs generated by the heavy ion regardless of avalanche effect.

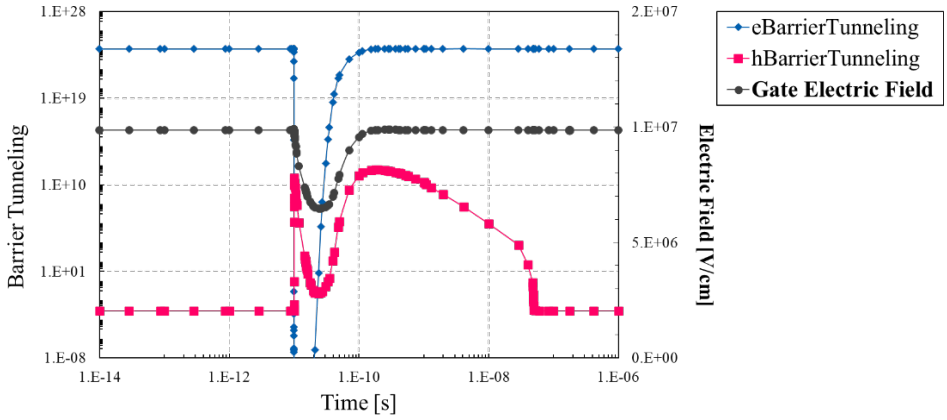

Fig. 6. Transient response of the gate electric field strength, electron barrier tunneling and hole barrier tunneling by simulation.

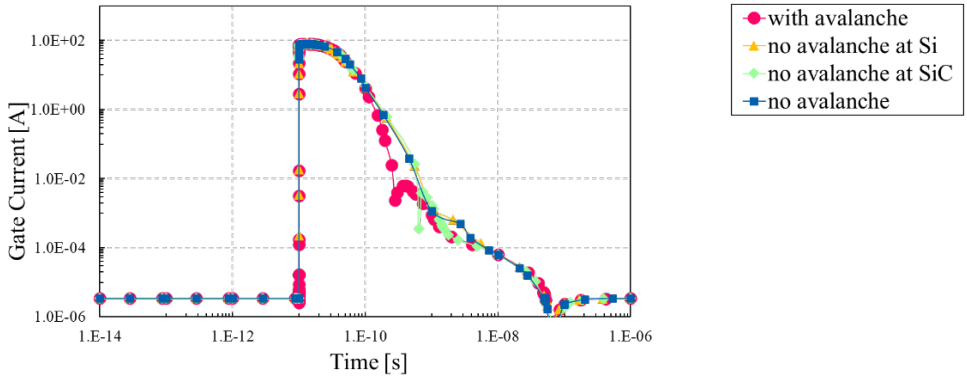

Fig. 7. Tunneling gate leakage current versus time with and without the avalanche mode by simulation.

Conclusion

This paper discusses the difference of E_{cr} for SEGR in SiC MOS capacitors with and without POA in an NO atmosphere, investigated by two-dimensional simulation of SEGR. No effect on the E_{cr} of different oxidation processes was observed, and thus SEGR susceptibility would not be affected by the oxide quality. In addition, simulation results suggested that SEGR for n-type SiC MOS capacitors was due to carriers in electron-hole pairs generated by heavy ions, regardless of avalanche effects.

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