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Fail-to-Open Short Circuit Failure Mode of SiC Power MOSFETs: 2-D Thermo-Mechanical Modeling

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Abstract. The short-circuit (SC) performance of Silicon Carbide (SiC) power MOSFETs has been extensively characterized in recent years. During a SC event, a SiC power MOSFET experiences a thermo-mechanical (TM) stress originating from a high temperature change during the SC event and the different coefficients of thermal expansions (CTEs) of source metallization, polySilicon gate, SiC and gate-source insulator. High temperature and TM stress cause the aluminum source metallization to melt, and a crack to form and grow within the gate-source insulation, leading to a short connection between the gate and source terminals typically referred to as fail-to-open (FTO) failure mode. This paper presents a 2-D thermo-mechanical (TM) model of a 2-D MOSFET half-cell for assessing the TM stress in the gate-source insulating layer during SC including the phase change behavior and the temperature-dependent properties of the source metallization. The developed modeling approach allows to assess how different metallization thicknesses and materials affect the TM stress of the gate-source insulation and, hence, enables the development of device design guidelines for improving SC withstand time of SiC power MOSFETs.

Introduction

During SC events of SiC power MOSFETs, two failure modes have been distinguished: fail-to-open (FTO) and fail-to-short (FTS). FTS is described by a significant reduction of drain-source resistance after the SC event, it is attributed to thermal runaway of SiC due to hotspots causing localized heating and typically occurs for dc-link voltages $V_{DC} \geq 0.5\ V_b$, where V_b is the rated blocking voltage. [1]. On the other hand, FTO failure leads to a short connection between the gate and source terminals and it is typically observed in the SC events at $V_{DC} \leq 0.5\ V_b$. FTO is often non-destructive to the package housing itself and hence, regarded as soft-failure. It was observed that FTO can occur before FTS under $V_{DC} \leq 0.5\ V_b$. For example, a gate failure was identified in the SC test of a reference 80 mΩ 1.2 kV SiC power MOSFETs under V_{DC} = 400 V for the SC duration of t_{SC} = 18 µs. FTO footprint is a decrease of V_{GS} visible after certain time of SC event, which leads to a gate-source failure after switching off the MOSFET. For a SC test with t_{SC} =18.5 µs, a decrease of V_{GS} similar to the SC test with t_{SC} = 18 µs was measured. However, after the device was switched off applying $V_{GS,off}$ = -5 V, a large residual current and the voltage initiated not only a FTO, i.e. the gate-source short-connection, but also thermal runaway.

As the FTS failure mode of a SiC power MOSFET is caused my thermal runaway, it can be modelled by device-circuit electro-thermal simulations. On the other hand, the cause of the FTO failure is described by the thermo-mechanical (TM) stress originated from a high temperature change during the SC event and the different coefficients of thermal expansions (CTEs) of source metallization, polySilicon gate, SiC and gate-source insulator. This has motivated a work on multi-physics modeling approaches [2-5] for evaluating the TM stress within a SiC MOSFET die during the SC event. However, the accuracy of these modeling approaches strongly depends on material properties, the physics of heat propagation being included as well as the geometry simplifications adopted to alleviate the computational complexity such as e.g. 1-D heat propagation [6-7]. Phase change is one

of the aspects that should be considered, to describe the melting of source metallization at higher temperatures [6, 8]. This physics-based approach is typically omitted in 2-D TCAD simulations of a MOSFET cell due to computational complexity. In a recent work [8], 2-D FEM electro-thermal model of a SiC power MOSFET developed in COMSOL Multyphysics was used to assess the impact of the latent heat caused by the melting process of source metallization on the temperature distribution within the MOSFET cell. It was shown that the maximum temperature within the semiconductor is reduced by up to 100 K when the phase-change physics is included, leading to a higher current density within the MOSFET cell and hence, higher power dissipation. However, modeling the melting of the source metallization is even more important for an accurate TM stress evaluation within the MOSFET cell. Namely, the CTE increases and the elasticity modulus of the aluminum source metallization decreases at high temperatures [9-10], which influence the TM stress in the gate-source insulating layer. Additionally, as long as the source metallization is in solid state, it experiences elastoplastic behavior [11]. In state-of-the-art publications [2-5], it is not evident that temperature-dependent properties and elastoplastic behavior of the source metallization were accounted for when assessing the TM stress during the SC event of SiC power MOSFET. The aim of this paper is to evaluate by modeling an impact of the source metallization on the TM stress within a SiC power MOSFET during a SC event at lower dc-link voltage, which typically leads to a FTO failure mode.

2-D Thermo-Mechanical Modeling of SiC Power MOSFET Half-Cell

The thermo-mechanical (TM) modelling of a SiC power MOSFET during a SC event, presented in this paper, is based on the 2-D model of a reference 80 mΩ 1.2 kV SiC Power MOSFET [12]. The 2-D geometry used in the electro-thermal 2-D TCAD simulations is shown in Fig. 1a). The simulated drain current and the maximum temperature of the aluminum source metallization are shown in Fig. 1b) for a SC event with V_{DC} = 400 V, the initial temperature T_{init} = 27 °C, and the duration t_{sc} = 14 µs, i.e. from *time* = 6 µs to *time* = 20 µs. As the aluminum melting point $T_{melt,Al}$ = 660 °C is typically assumed to be the first stress mechanism during SC (even though the device can recover from the partial melting of the metallization), $T_{melt,Al}$ is highlighted in Fig. 1. It should be noted that the phase-change behavior of the source metallization is not modeled in TCAD simulation to reduce computational complexity. Accordingly, there is an error of approximately 10% in the evaluation of total losses. In the next step, the time- and position-dependent power density $P(t, x, y)$ is imported from a 2-D TCAD simulation of the reference device [12] and used as the input of the TM simulation.

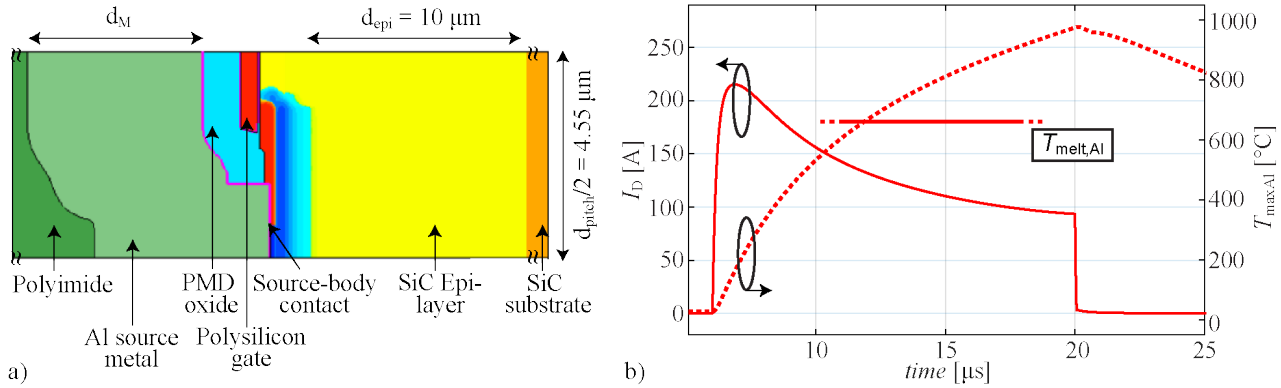

Fig. 1. a) Half-cell-pitch 2-D TCAD model of a reference 80 mΩ 1.2 kV SiC Power MOSFET. b) Simulated electro-thermal SC event with V_{DC} = 400 V: drain current (I_D) and maximum temperature in the source metallization (T_{maxAl}).

The 2-D TM model implemented in COMSOL Multiphysics and the power loss input $P(x, y)$ for *time* = 12 µs are shown in Fig. 2. The TM model includes the phase change behavior and the temperature-dependent elastoplastic behavior of the aluminum source metallization. Phase change is modelled based on *Apparent Heat Capacity Method*, provided by COMSOL Multiphysics, assuming that the phase transition occurs between $T_{melt,Al} - T_{trans}/2$ and $T_{melt,Al} + T_{trans}/2$ with T_{trans}= 50 K and the latent heat $C_{L,Al}$ of 396 kJ/K taken from [13]. The temperature dependent elasticity E_{Al} and CTE_{Al} of

aluminum are taken from literature [9-10]. The bilinear kinematic hardening model defined by the yield stress σ_s and kinematic modulus $E_{k,Al}$ is used to model elastoplastic behavior of the aluminum source metallization. As the temperature-dependent parameters σ_s and $E_{k,Al}$ are provided in literature only until approx. 250 °C, the values at higher temperatures are extrapolated. For preventing convergence problems when reaching melting temperatures, the Activation Node of COMSOL Multiphysics is used, which allows deactivating the physics of plasticity in all mesh elements within the source metallization, reaching $T_{melt,Al}$ and modeling them as linear with the material properties of liquid, i.e. low elasticity modulus and high CTE. The layer of gate-source insulation marked as PMD oxide in Fig. 1 is implemented in COMSOL by using constant material properties of silicon dioxide (SiO_2) due to a lack of knowledge on the material properties of the actual pre-metal dielectric (PMD) layers.

The model is parameterized and the thickness of the source metallization d_M can be adjusted. The first study is performed to evaluate the impact of the thickness of source metallization on the stress within the gate-source insulator layer, comparing $d_{M,Al}$ = 4 µm and 10 µm. Copper source metallization can increase the electro-thermal die performance due to its higher electrical conductivity, higher yield stress, and higher melting temperature. Furthermore, copper bond wires are then used instead of aluminum bond wires for the top die connection, increasing power-cycling capability of the package and hence, ensuring higher reliability under actual operating conditions [14]. Therefore, the second study is run with $d_{M,Cu}$ = 4 µm using the copper material properties provided by COMSOL and from [15] for the source metallization material.
The total loss model $P(t, x, y)$ is extracted for each study separately from the corresponding TCAD ET simulations.

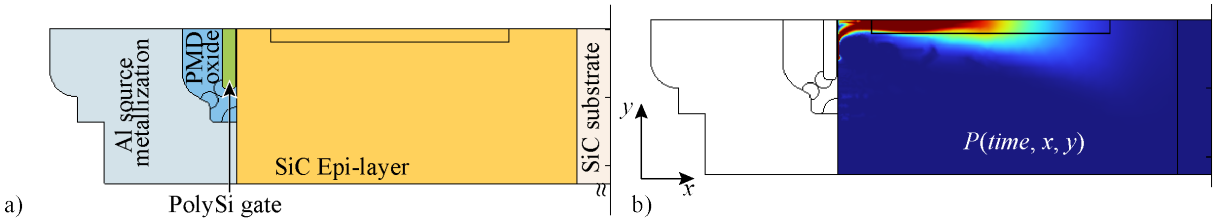

Fig. 2. 2-D TM model built in COMSOL Multiphysics: a) 2-D half-cell-pitch modelled geometry of a commercial 1.2 kV SiC power MOSFET, and b) time- and position-dependent heat dissipation extracted from the 2-D TCAD simulation (shown at *time* = 12 µs, cf. Fig. 1) and used as input to evaluate the TM stress distribution.

Modeling Results

The results from the COMSOL TM simulations for a $d_{M,Al}$ = 4 µm thick aluminum source metallization are shown in Fig. 3. The temperature distribution, cf. Fig. 3a), and the Young modulus, cf. Fig. 3c), within the MOSFET cell, the phase change fraction of the source metallization, and von Misses stress in the gate-source insulating layer, cf. Fig. 3b), are presented in three time points during the SC event shown in Fig. 1b): 1) 10 µs, 2) 12 µs, and 3) 14 µs. At *time* = 10 µs, the melting of aluminum is not yet started; the partial melting is shown for *time* = 12 µs, while at *time* = 14 µs, the metallization is in a molten state. The stress within the gate-source insulating layer is shown to increase with the temperature. A higher stress is located in the corners of the gate-source insulating layer, however, also at the top interface between the source metallization and the gate oxide marked in Fig. 4a). These results agree to the experimentally detected cracks initiated at a corner of the gate oxide towards the polysilicon gate as shown in [3, 4, 8, 16].
Increasing the metallization thickness provides larger heat capacitance from the top and hence, reduces the temperature rise as shown in Fig. 4b). On the other hand, a thicker metallization induces more stress in the gate-source dielectric layer. However, when comparing the simulated von Misses stress for $d_{M,Al}$ = 4 µm and $d_{M,Al}$ = 10 µm (see Fig. 4), the stress reduces for the thicker metallization

as the lower temperature due to the thicker metallization is the dominant factor. The effect is more pronounced in the pockets denoted as corners compared to the top of the metallization.
The melting does not occur in the depicted time period of the simulation with the copper metallization $d_{M,Cu}$ = 4 µm, as indicated also in Fig. 4b). The phase change state equals zero due to a significantly higher melting temperature of copper, i.e. $T_{melt,Cu}$ = 1085 °C. The temperature is not reduced by replacing the aluminum with the copper metallization as shown in Fig. 4b), which can be explained by a smaller heat capacity of copper. Accordingly, the stress is higher than for $d_{M,Al}$ = 4 µm, cf. Fig.

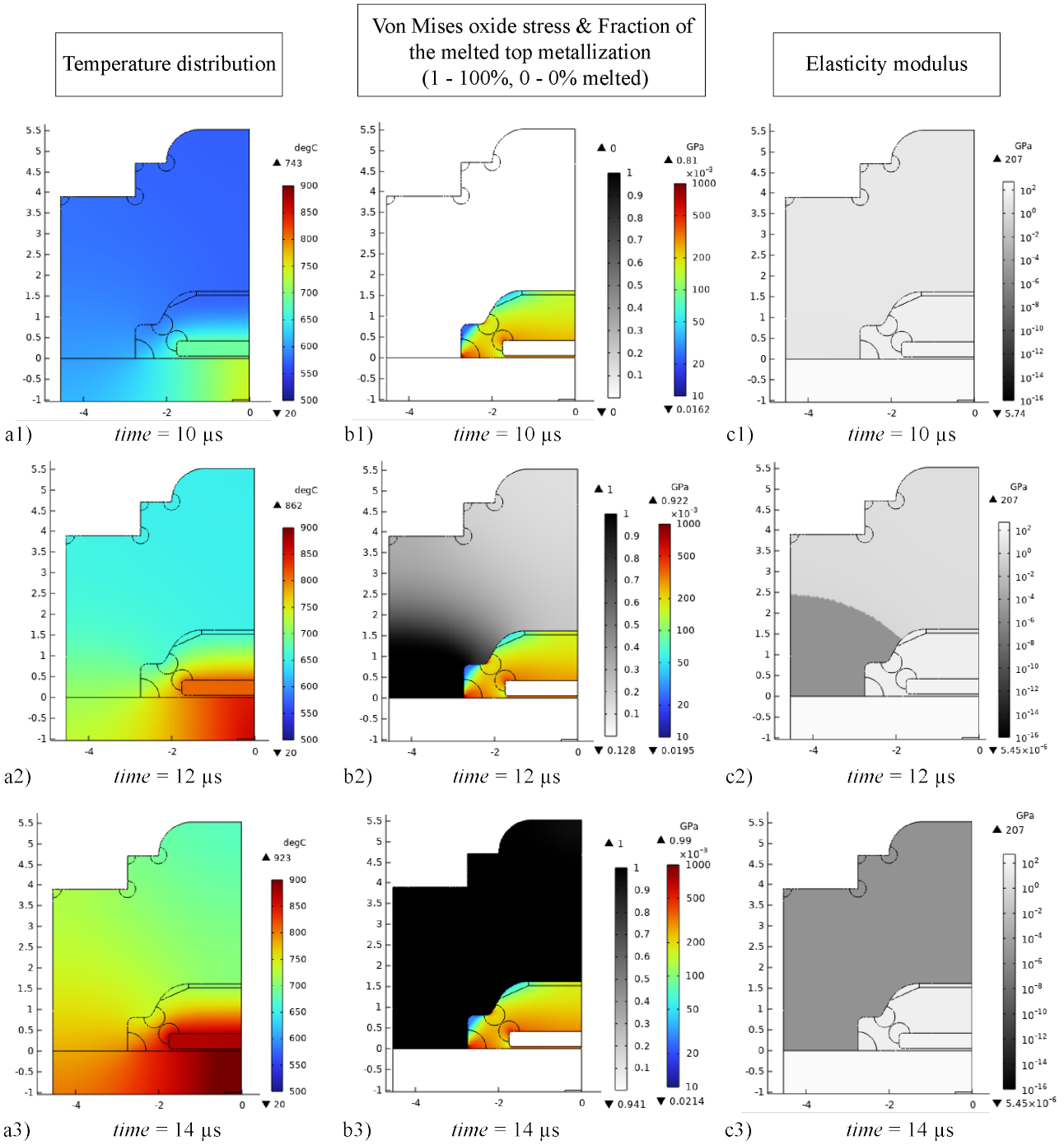

Fig. 3. Thermo-mechanical simulations in COMSOL of the 2-D half-cell-pitch MOSFET model shown in Fig. 2: a) the temperature distribution, b) von Mises stress in the gate oxide domain shown together with the fraction of the melted source metallization, where 1 - 100% melted, 0 - 0% melted, and c) the elasticity modulus within the structure showing smaller values in the regions with higher temperature, for 1) *time* = 10 µs, 2) *time* = 12 µs, and 3) *time* = 14 µs.

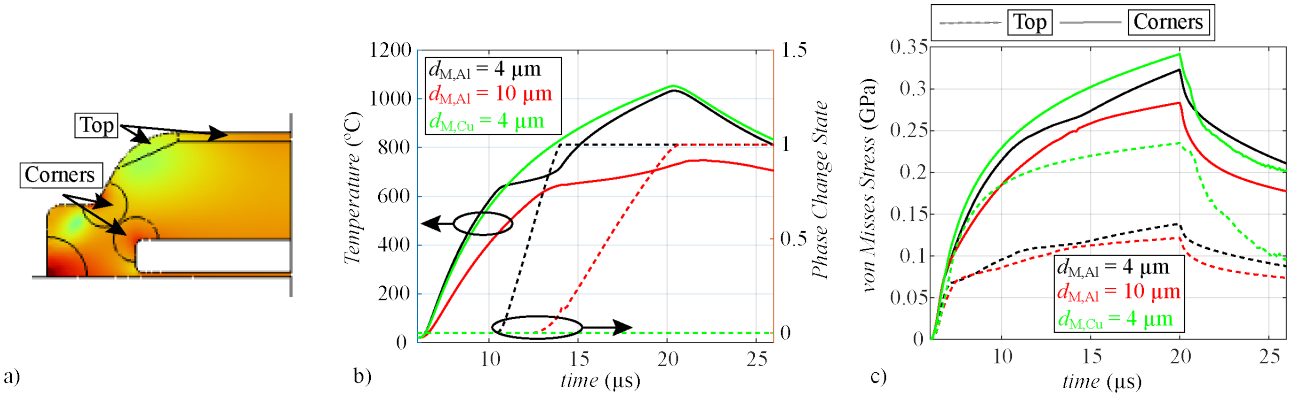

Fig. 4. Thermo-mechanical simulations in COMSOL of the 2-D half-cell-pitch MOSFET model shown in Fig. 2 : a) the selected regions within the gate-source insulation layer marked as corner and top, b) the maximum temperature evaluation in the source-metallization and the average phase change state i.e. the fraction of the melted source metallization, and c) von Mises stress in the corner and top regions of the gate-source insulation layer, for the simulations with $d_{M,Al}$ = 4 µm, $d_{M,Al}$ = 10 µm and $d_{M,Cu}$ = 4 µm.

4c) and the copper source metallization can initiate the cracks in the gate-oxide during SC events; however, without melting there should be no leaking of metal in the crack forming the short connection between the gate and source. Experimental evidence would be necessary to verify these simulation findings. Fabricating SiC power MOSFETs with the top copper metallization is foreseen for future investigations and it is not in the scope of this work.

Summary

The aim of the presented work is to show how the thickness and material properties of the source metallization can affect the thermo-mechanical stress in the gate-source insulating layer and to correlate the simulation results to the failures of SiC power MOSFETs observed in the short-circuit experiments. The presented modeling shows that the failures such as the cracks in the corner and the top of the gate dielectric stack of SiC power MOSFETs, observed under the SC events at lower dc link voltages and leading to gate-source low resistive path, can be linked to high die temperature, the thickness and mechanical material properties of the source metallization. Accordingly, the developed modelling approach represents a baseline for evaluating how different material properties can affect potential failures of SiC power MOSFETs at very high internal device temperature.

References

[1] B. Kakarla, *et al*. *Materials Science Forum*, vol. 924, Trans Tech Publications, Ltd., June 2018, pp. 782–785.

[2] F. Loche-Moinet, *et al*., in Proceedings of 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2023, pp. 1-7.

[3] K. Yao, *et al*., *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4328-4334, 2020.

[4] J. Liu, *et al*., *IEEE Electron Device Letters*, vol. 41, no. 1, pp. 103-106, Jan. 2020.

[5] Kailun Yao, *et al*., *Microelectronics Reliability*, vol. 122, 2021, 114163

[6] F. Richardeau, F. Boige, *Microelectronics Reliability*, vol. 100–101, 2019, 113501.

[7] Y. Pascal, *et al*., in Proceedings of IEEE International Workshop on Integrated Power Packaging (IWIPP), 2019, pp. 137-142.

[8] E. Sarraute, *et al*., in Proceedings of 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2023, pp. 1-8

[9] Rex B. et al., *Journal of Physics and Chemistry of Solids*, vol. 48, no. 7, pp. 603-606, 1987.

[10] Leitner, M., *Metallurgical and Materials Transactions A*, vol. 48, pp. 3036–3045 (2017)

[11] I. Kovacevic-Badstuebner *et al*., in Proceedings of IEEE International Reliability Physics Symposium (IRPS), 2023.

[12] A. Tsibizov *et. al.*, *IEEE Transactions on Power Electronics*, vol. 35, pp. 1855-1865, 2020.

[13] M. Leitner et al., *Metallurgical and Materials Transactions A*, vol. 48, no. 6, pp. 3036–3045, 2017.

[14] Frank Hille et al., *Microelectronics Reliability*, vol. 64, 2016, pp. 393-402.

[15] Shengde Zhang, et al., *Procedia Engineering*, vol. 10, 2011, pp. 1497-1502.

[16] Xi Jiang, et al., *Microelectronics Reliability*, vol. 88–90, pp. 593-597, 2018.