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Gate Resistance Integration in SiC MOSFETs: Performance Simulations under Different Implementation Methods

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Abstract. This paper proposes performance evaluation of SiC MOSFETs power devices introducing in the device layout some specific design to achieve desired value of intrinsic gate resistance. This aspect can be helpful to eliminate external components such as gate resistance, saving space and cost, considering the application of the gate driver directly connected to the power device. Description about the layout modification of the device die is presented and dedicated simulation approach is set and exploited to predict the signal propagation on the die while verifying the gate resistance defined by the new layout structure. Experimental results including switching losses evaluations performed with double pulse tests sequence with half-bridge converter realized with new SiC MOSFETs devices, are also reported in the paper.

Introduction

Thanks to their intrinsic properties, SiC MOSFETs characteristics can be easily exploited to improve efficiency of all types of power converters based on these devices [1], [4]. Performance improvement is related to many factors, such as the switching frequency, thermal dissipation, breakdown limit voltage, R_{dson}·Area. Among these, switching frequency is also related to the switching speed in terms of “slope” of voltage and current. Drain-source voltage slope and power loop current slope can be easily regulated acting, basically, on the gate resistance connected between device gate and gate-driver circuit.

It is well known that different configurations of gate resistance connection can be realized to speed up or to slow down the waveforms slopes of device under test for turn on and/or turn off transients.

Typically, for each converter applications dv/dt and di/dt can be defined as desired operating conditions to optimize overall performance, consequently for these parameters suitable value of gate resistance will be used to drive the SiC MOSFET [5].

Instead of applying external gate resistances, during device design process, specific intrinsic gate resistance value can be considered, acting on device structure with appropriate layout or by using specific production process. Currently, the modification or inclusion of suitable intrinsic gate resistance is receiving more and more attention and also some technics are defined to evaluate this parameter as reported in [6]. [7].

In this paper is presented and investigated a solution to target the desired intrinsic gate resistance supported by Spice-like simulations to preliminary evaluate the gate signal propagation of the proposed structure. The effectiveness of the proposed device layout will be also experimentally verified providing information about switching losses performance.

Modeling Flow Description and New SiC MOSFET Layout Proposal

Simulation approach

A modelling strategy based on the concept of system complexity reduction has been applied to SiC power MOSFET [2], [3]. The modelling flow is founded on the idea of discretization of the die

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active area and allows to reproduce by simulation all the electrical effects peculiar to the large silicon area and to easily describe the phenomena occurring inside the device.

The proposed model is able to reproduce a Pspice-like equivalent circuit of the Power MOSFET which takes into account the impact of the device layout. Many simulation outputs can be extracted by this model and, among them, the most relevant and mainly requested for this analysis are the intrinsic gate resistance and the gate signal propagation which can be provided as 2D animation. Of course, in the document, some pictures at specific time instant are reported to describe the signal propagation.

The workflow starts directly at importing the device mask-set library and converting it into a service layer, then through a discretization process based on a mesh partition of the original layout a numerical matrix is generated. Each index of that matrix describes a physical/electrical function of the various parts of the layout.

The second step, done by means of a customised tool developed by STMicroelectronics, involves the translation of the numerical matrix into an equivalent big spice netlist where the active and passive parts are electrically modelled. The active part consists in the elementary cell which, depending on the level of discretization used, is represented by a scaled spice model (also self-heating if it is necessary to evaluate the thermal propagation on the layout). Each passive part, which in this case consists of parasitic contributions due to the resistivity and capacitances of the metal and polysilicon, is modelled by an RC scale to account for delays due to the layout's interconnections. Each node in the netlist is associated with an index containing information on the cell's position within the original structure; in this way, after a simulation, it is possible to construct a 2D animation capable of reproducing the transients on the device's internal electrical behaviour and any faults or hot spots that might occur within the layout. As application case, the described methodology has been applied for optimizing the layout performances of a SiC Power MOSFET device, basing on intrinsic gate resistance (Rg) evaluation.

The described methodology is applied to choose the right strategy of die design in order to achieve the requested intrinsic gate resistance for specific applications such as traction inverter for electric vehicles.

The schematic workflow of the proposed methodology is reported in Figure 1 [2], [3].

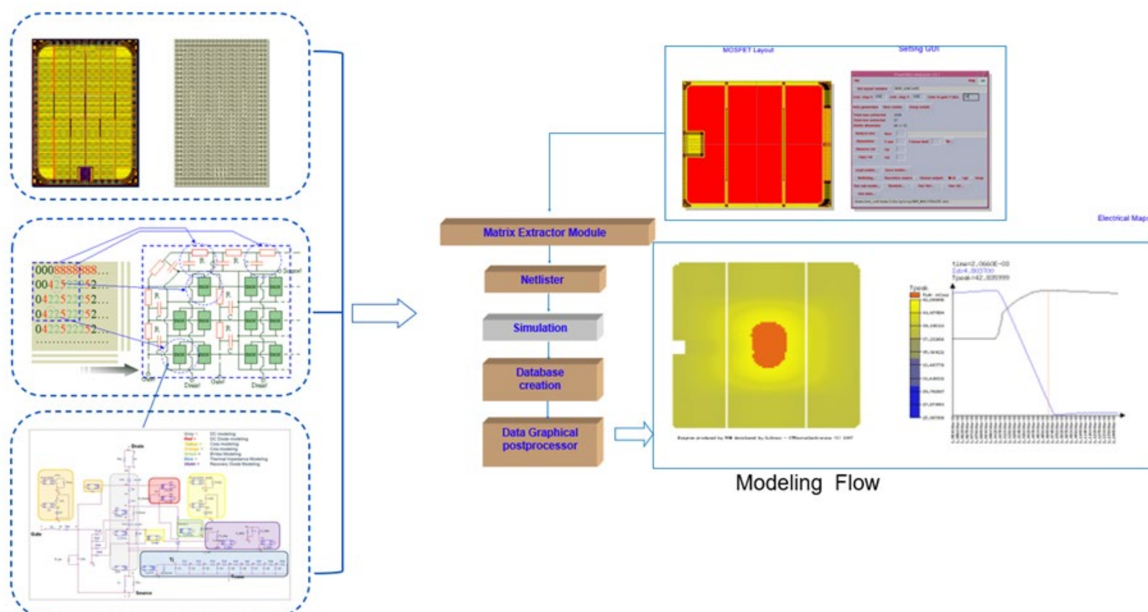


Fig. 1 Schematic workflow of the simulation methodology that combine a Pspice equivalent circuit of the elementary SiC MOSFET cell and customised STMicroelectronics tool for 2D animation of transients of the device's internal electrical signals.

New Layout proposal to set specific intrinsic gate resistance

A case study is presented comparing the integration of gate finger inside active area trimming transient speed. The cases with different layout and different gate finger localization is discussed in the next, and relative structure is shown in Figure 2.

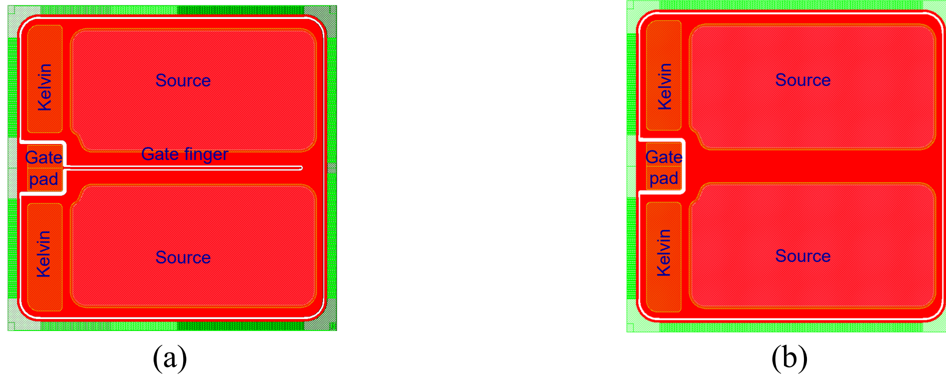


Fig. 2. Comparison of devices structure (a) standard layout (b) proposed layout without gate finger.

For the standard case, device die layout is reported in Figure 2(a) where the gate finger pass through the entire structure having a single metal source since it is connected in the opposite area of the gate pad. In the new proposed layout, Figure 2(b), the gate finger is removed defining active area wider than standard one and lowering on state resistance, R_{dson} of 5%.

Simulation Results and Experimental Tests

The comparison between two different layouts, aforementioned discussed, is shown in the following figures, relative to the gate voltage propagations during switch off transient, referred to the same time-step. The SiC MOSFETs test vehicle is a 650V, 13mΩ device.

First of all, standard device layout is simulated as reference, which includes gate finger in the die structure and presenting an intrinsic gate resistance of 1.35Ω@1MHz instead with the new proposed layout an intrinsic gate resistance of 4.24Ω has been achieved. Figure 3(a) and Figure 3(b) show two frames describing the propagation of the gate signal during the turn-off at the same time instant respectively for the standard layout and the new proposed one.

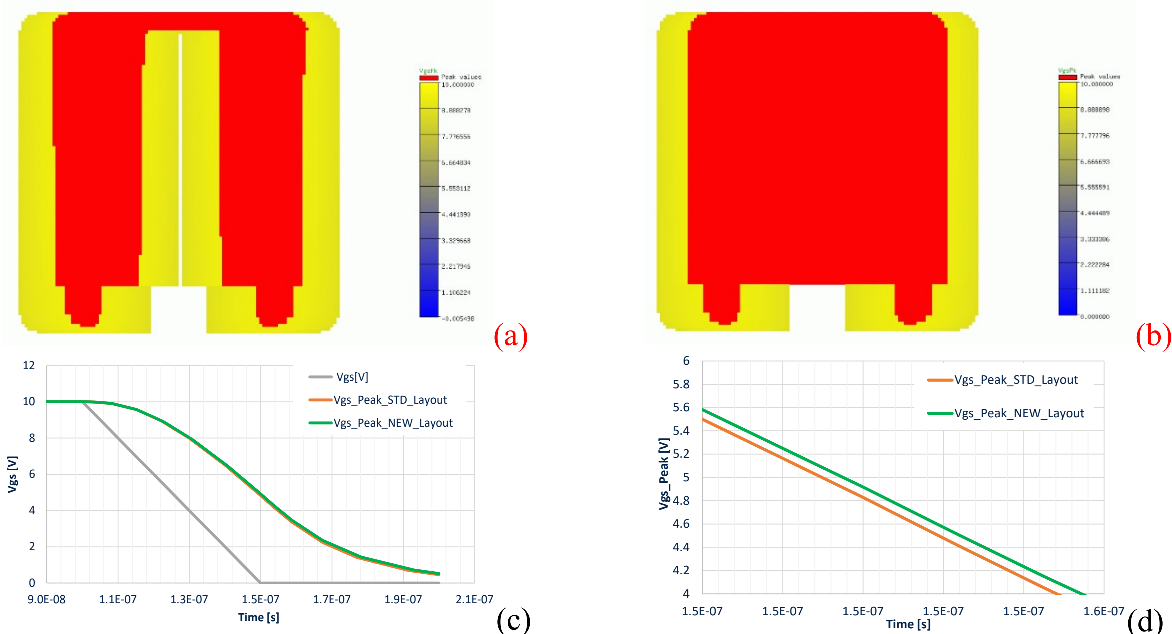


Fig.3. V_{gs} signal propagation for (a) standard layout (b) proposed layout without gate finger at the same time instant. Comparison of Vgs profiles as function of the time (c) and zoomed view (d).

As can be noted in the standard layout of Figure 3(a), the final gate-source voltage peak is reached in a concentrated area near the gate finger, instead in the new proposed layout, Figure 3(b), the peak voltage is uniformly reached in all the cell of structure. Figure 3 (c) and Figure 3(d) show V_{gs} profile monitored as function of the time for both layouts.
The green and orange curves represent the peak gate voltage for both investigated layouts probed instant by instant. They are compared with the grey curve representing the reference V_{gs} for the ideal case in which all cells switch uniformly. A zoom view is shown in Figure 3(d) to amplify the differences that basically can be considered negligible between the proposed layout without gate finger and the standard one. Hence, the gate finger removal does not impact on the gate signal propagation inside the die.

SiC MOSFETs performance of the vehicle under test with standard layout and with the proposed new one has been also experimentally evaluated, by means of a half-bridge converter as illustrated in the equivalent electrical circuit of Figure 4 (a).
The double pulse tests method is used to evaluate turn-on and turn-off energy losses with the setup shown in Figure 4 (b), considering the devices assembled in HiP247-4L® package that also includes Kelvin-source pin.

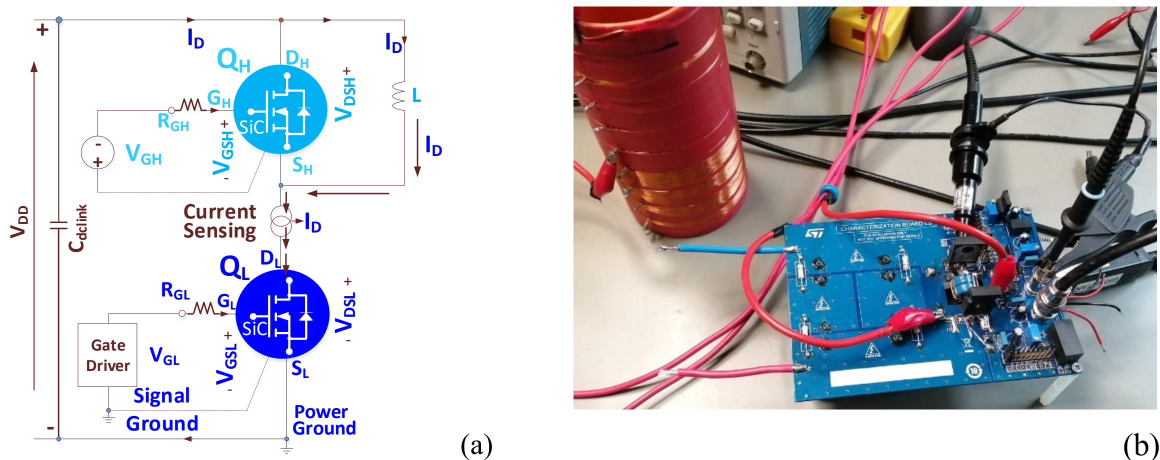


Fig. 4. Equivalent half bridge configuration for switching losses evaluation (a), printed circuit board of the half bridge, load inductor and probes to measure voltages and current (b).

Switching losses at turn-on and turn-off of the standard layout and the new one have been performed as function of drain current, considering V_{DD}=400V, V_{GS}=-3V/18V, and case temperature of 25°C and 200°C.

The object of these experimental tests is to compare the performance of these devices which have basically different intrinsic gate resistance, respectively of 1.35Ω and 4.24Ω, hence to do so, a suitable gate resistance has been added externally, to be sure that the gate driver operate with both devices with similar equivalent gate resistance and therefore providing the same gate current profile, achieving specifically for these tests, voltage and current slopes respectively of 6V/ns during turn-off and 1.4A/ns during turn-on at typical operating conditions of 50A at 25°C.

Numerical evaluation of Eon and Eoff and relative indication of di_{ON}/dt, dv_{OFF}/dt and V_{DSPEAK} are reported for 25˚C and 200˚C in Table I and Table II respectively. It is important to specify that for high temperature tests, both high side and low side devices are heated. Figure 5(a) and Figure5(b) show the trend line of Eon and Eoff as function of the current of the proposed device with new layout that are aligned to the standard one. This means that the new layout does not introduce abnormal switching losses behaviour.
Finally, experimental waveforms of new device with the proposed layout are shown in Figure 6 and Figure 7, they represent the profile relative to V_{GSL}, V_{DSL} of the active device, (Q_L considering the schematic of Figure 4), V_{GSH} and V_{DSH} of the passive device (Q_H considering the schematic of Figure 4) used as freewheeling diode and current I_D, during turn on Figure 6 (a) and turn-off Fig.6(b) at

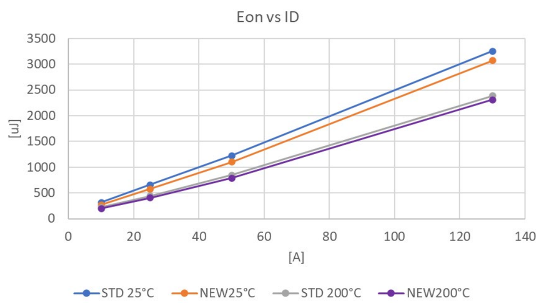
25°C, V_{DD}=400V, I_D=50A V_{GS}=-5V/18V, instead Fig.7(a) and Fig.7(b) show the waveforms achieved at the same voltage and current conditions of Fig.6 but with T_c=200°C. As can be noted the transient responses show very limited oscillations, thanks to the intrinsic gate resistance value of 4.35Ω, as expected during development of this type of SiC MOSFET.

Table I Switching losses data for STD and new layout at 25°C

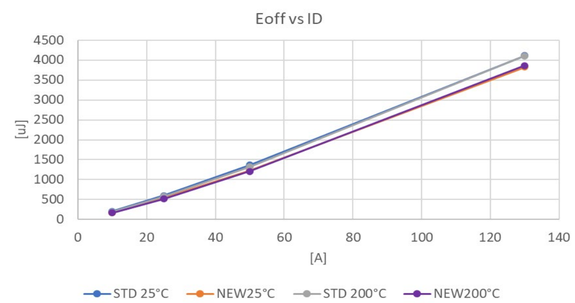
	I_D [A]	E_{ON} [µJ]	di_{ON}/dt [A/ns]	E_{OFF} [µJ]	dv_{OFF}/dt [V/ns]	$V_{DS\ peak}$ [V]
STD 25°C	10	318	0.7	207	4	429
	25	658	1.1	604	4	461
	50	1222	1.4	1365	5	491
	130	3256	2.1	4114	6	543
New 25°C	10	268	0.7	176	5	431
	25	578	1.1	537	6	467
	50	1102	1.4	1234	6	500
	130	3071	2.1	3822	7	562

Table II Switching losses data for STD and new layout at 200°C

	I_D [A]	E_{ON} [µJ]	di_{ON}/dt [A/ns]	E_{OFF} [µJ]	dv_{OFF}/dt [V/ns]	$V_{DS\ peak}$ [V]
STD 200°C	10	222	0.9	190	4	426
	25	438	1.3	575	5	456
	50	845	1.7	1318	6	481
	130	2385	2.5	4103	6	530
New 200°C	10	201	0.8	171	5	429
	25	402	1.3	521	6	460
	50	786	1.7	1207	6	487
	130	2310	2.4	3862	7	541

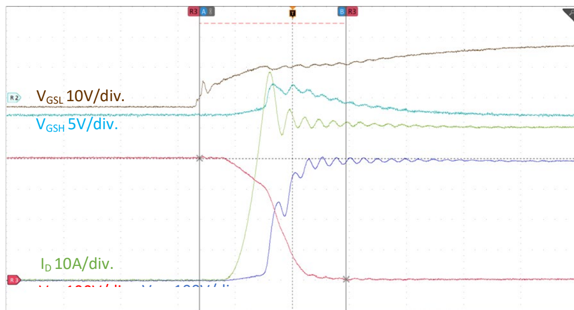


(a)

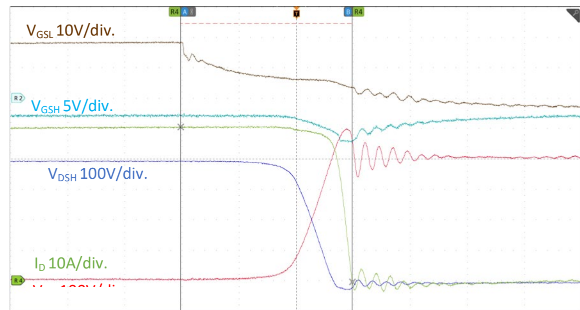


(b)

Fig. 5. Switching losses vs I_D for STD and New proposal layout at 25°C and 200°C (a) Eon trend line, (b) Eoff trendline.

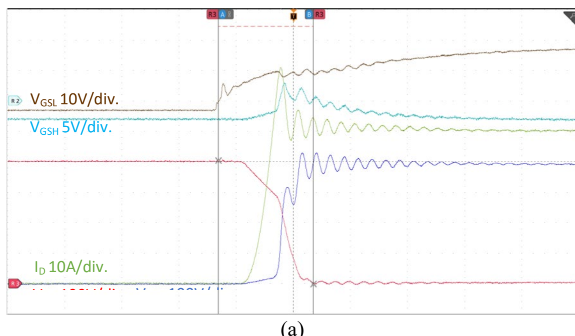


(a)

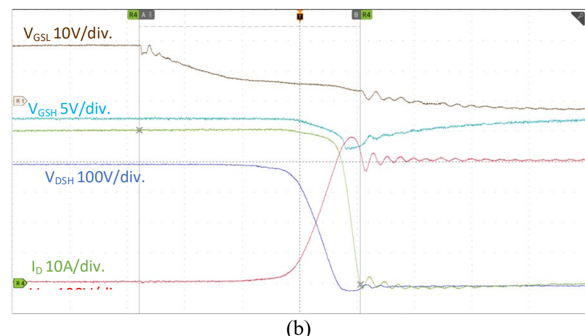


(b)

Fig. 6. Switching losses for new proposal layout at V_{DD}=400V, I_D=50A V_{GSL}=-5V/18V, V_{GSH}=-5V, T_c=25°C representative waveforms for tur on (a), turn off (b).



(a)



(b)

Fig. 7. Switching losses for new proposal layout at V_{DD}=400V, I_D=50A V_{GSL}=-5V/18V, V_{GSH}=-5V, T_c=200°C representative waveforms for tur on (a), turn off (b).

Conclusions

In this paper, the design of a SiC MOSFET with new layout has been presented to modify the intrinsic value of the gate resistance without modifying other device performance. The main object of the proposed device is the mitigation of undesired electrical oscillations during switching transients, without adding external components. Simulations and experimental tests have been reported verifying the expected behaviour.

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