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Concept and Technology for Full Monolithic MOSFET and JBS Vertical Integration in Multi-Terminal 4H-SiC Power Converters

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Abstract. New and original medium power multi-terminal SiC monolithic converter architectures are investigated with vertical switching cells based on SiC JBS diodes and VDMOS transistors. 2D TCAD and mixed-mode Sentaurus^{TM} simulations are performed to optimize switching structures as Buck, Boost, H-bridge high-side row chip common drain-type and low-side row chip common source-type. The proper operation in the turn-on and turn-off of each cell is also studied and validated. To fabricate these new monolithic integrated architectures, two main technological bricks have been developed, for vertical insulation and the integration of a top Ni metal via. To achieve the vertical insulation deep trenches are necessary combining dry plasma and wet KOH electrochemical etching through the thick N^+ substrate.

Introduction

For electric vehicles, there is a growing interest for the monolithic integration of dedicated power conversion functions in SiC dies [1]. Nowadays, power converters are realized using multiple dipole VDMOS chips that are bonded on a power substrate and interconnected using multiple bond wires [2]. This constitutes an expensive operation, time-consuming and source of aging problems [3]. In silicon carbide, few works were reported on the monolithic integration of power functions built with vertical VDMOS, most of them focused on the integration of auxiliary low-voltage functions [4].

The present paper explores the monolithic integration in SiC, within a single chip, of vertical switching cells based on JBS diodes and VDMOS. It proposes new and original medium power multi-terminal SiC monolithic converter architectures: Buck, Boost, H-bridge high-side row chip common drain-type and low-side row chip common source-type. This proposed ultimate efficient power vertical integration, using a minimum number of multi-terminal chips [5,6], will improve further the performance, reliability and reduce cost of the currently used discrete-dies-based switching cells.

The proposed monolithic multi-terminal chips require mutualizing as many semiconductor regions as possible within the volume and metal layers on the surface. Consequently, the chip has to support the applied voltage both vertically and laterally. This major feature represents the main technological challenge for which new specific technological processes were developed and discussed in this paper. These new technology bricks involve, backside dielectrically filled deep trenches for lateral insulation and through metallic via for connecting top side electrodes with backside electrodes. These bricks

constitute a technological breakthrough as compared to the state of the art permitting innovative functionalization on SiC substrates that are widely used in numerous application sectors.

Concept of H-bridge power converter integration within multi-terminal chips - TCAD Sentaurus™ simulations

The proposed vertical multi-terminal architectures for H-bridge converter integration were designed so that each of the co-integrated switches supports at least 600V in the blocking state, both vertically and laterally at the upper-side of the SiC-chip, and to carry a nominal current of 10 A in on-state. The physical and geometrical parameters of the co-integrated VDMOS and JBS diode were imposed by the CNM laboratory (Centro Nacional de Microelectrónica from Barcelona, Spain) process flow [7,8].

Concept of three-terminal common-drain and common-source monolithic chips. The converter of Fig.1a can be realized by an appropriate packaging of two multi-terminal chips. Indeed, this can be achieved by using a first chip named a common-source three terminal chip that integrates two VDMOS structures as shown in Fig. 1b, whose 2D view is similar to that of the bidirectional Field Effect Transistor (BiDFET) realized in [9], and on a second chip named a common drain three terminal chip. Such a configuration leads to a generic H-bridge topology.

The device optimization consists thus in the minimization of the leakage current through the off-state section in vertical direction and in lateral direction. In the case of the common drain chip, a vertical trench is not mandatory between the two VDMOS sections. However, in the case of the common source chip, a vertical trench is mandatory to prevent any lateral current flow both in the N^- epi-layer and in the N^+ substrate between the drain1 and drain2 electrodes that are set at two different electrical potentials. Its realization requires the setup of a specific new technological brick to be integrated in a standard VDMOS process flow. The proposed new insulation technique combines a deep and high doped P^+-type implantation region in the top and a deep dielectrically filled etched trench from the back-side.

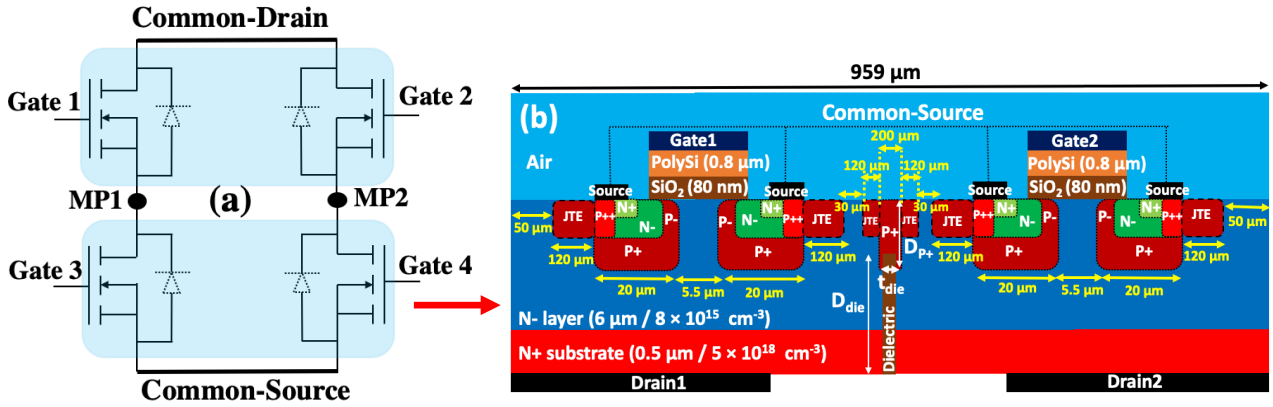

Fig. 1. a) Half-bridge simplified equivalent electrical circuit, using N-type SiC VDMOS devices, b) Cross-sectional principle of the Common-Source type structure (low-side row of the Half-bridge)

The operating modes, off-state, on-state and switching, were validated through 2D TCAD Sentaurus™ Mixed-Mode simulations [10]. The distribution of equipotential lines within the elementary chip (Fig. 2) shows a homogenous spreading in the structures, optimized in order to keep the electric field peaks lower than 2.1 MV/cm, under the critical electrical field in SiC. Geometrical parameters were determined for the optimized structure architectures.

These involve wafer thickness, junction termination extension (JTE) length, minimal lateral distances to support the high voltage between the different co-integrated vertical MOSFETs (Fig. 3). The minimum dielectric width "t_{die}" shown in Fig.1b must be greater than 20µm to ensure voltage blocking capability of 720V.

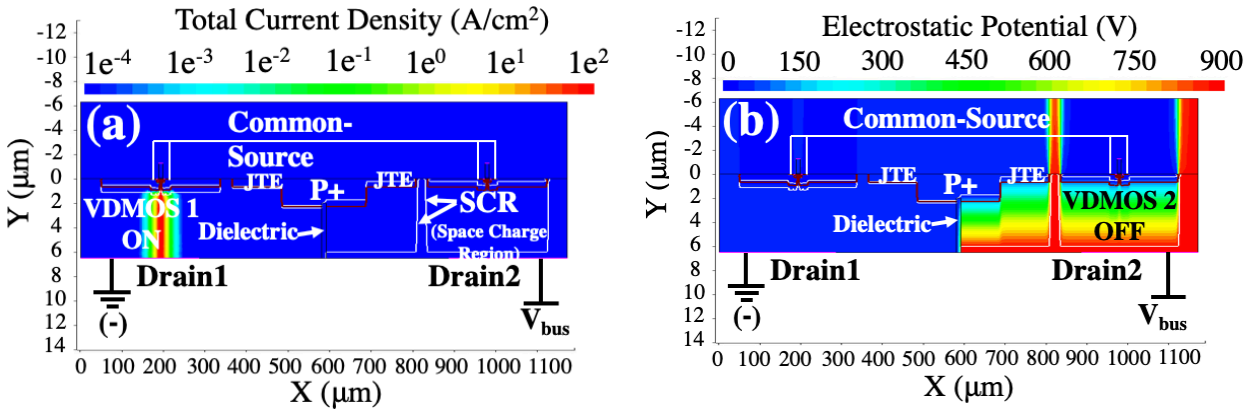

Fig. 2. a) Distribution of the total current density, b) Distribution of the equipotential lines in the common-source type three-terminal H-bridge SiC MOSFET power chip (X to Y ratio: 30 ,V_{bus} = 800V)

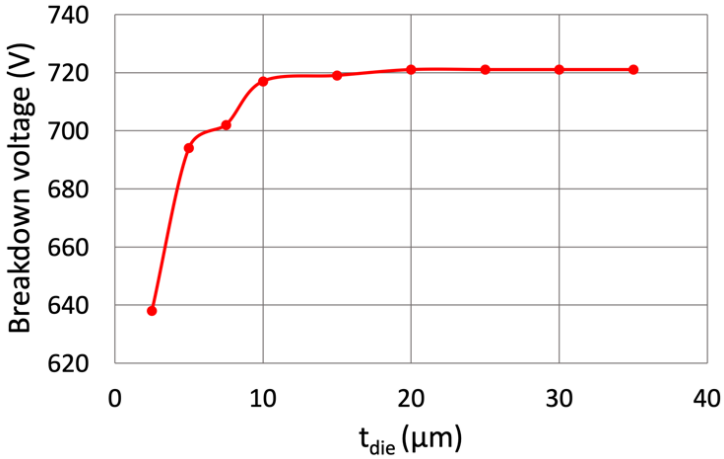

Fig. 3. Variation of the breakdown voltage of the common-drain H-bridge structure as a function of the dielectric thickness "t_{die}".

Concept of three-terminal monolithic switching cell. It aims at integrating a complete switching cell within a single multi-terminal chip. In this context, two versions of multi-terminal chips were designed: one chip that integrates the high-side JBS diode with the low-side VDMOS and the other chip integrates the low-side JBS diode with the high-side VDMOS as illustrated in Fig. 4.

Such configurations lead to a generic inverter phase-leg or a synchronous buck-boost chopper. The co-integrated VDMOS and JBS diode require insulation by a deep trench as described previously as well as the realization of the metallic via, through the epi-layer, that ensures original / novel electrical interconnection between the mid-point (MP) and the backside N^+ substrate. Such vias are realized by Nickel electroplating process. These specific technological bricks will be discussed in the next paper section.

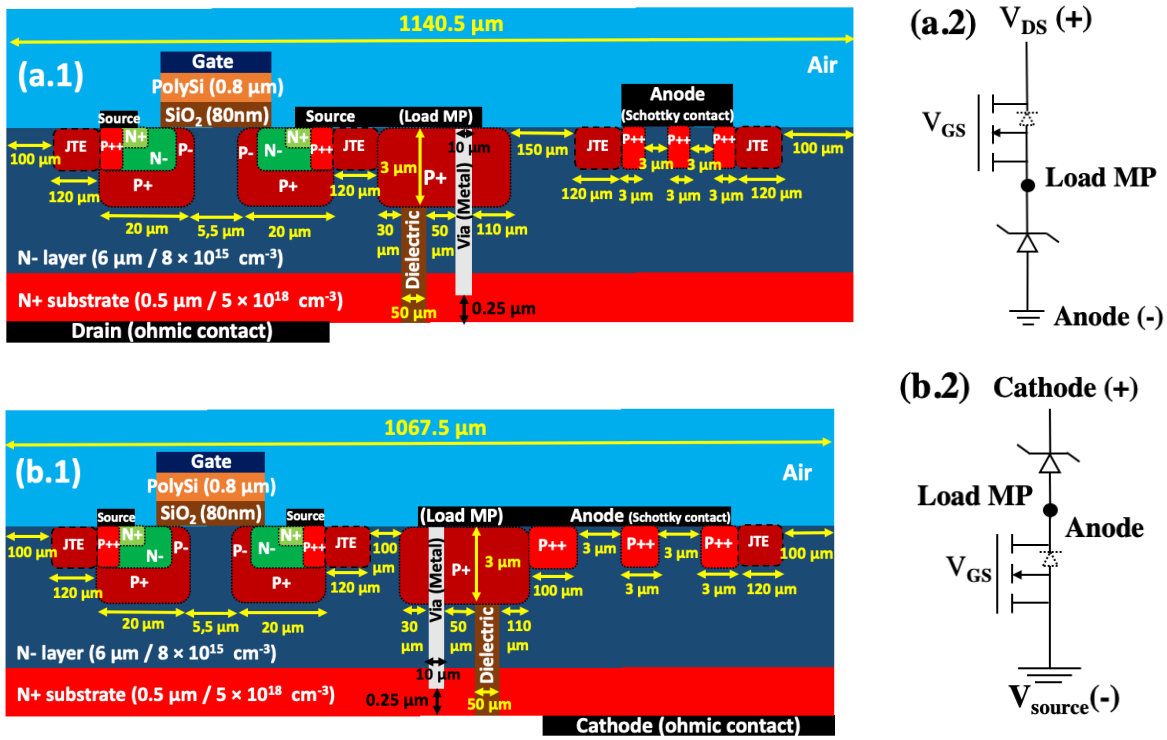

Fig. 4. a) SiC VDMOS-JBS Buck-type switching cell principle: (a.1) Cross sectional view of the proposed 3-terminal chip with the different technological and geometrical parameters, (a.2) Simplified equivalent electrical circuit. b) SiC VDMOS-JBS Boost-type switching cell principle: (b.1) Cross sectional view of the proposed elementary 3-terminal chip with the different technological and geometrical parameters, (b.2) Simplified equivalent electrical circuit.

In order to validate the operating modes in blocking state, Buck-type and boost-type switching cells were simulated in configurations in which a VDMOS in the off-state and the diode in the on-state (Fig. 5) or vice-versa.

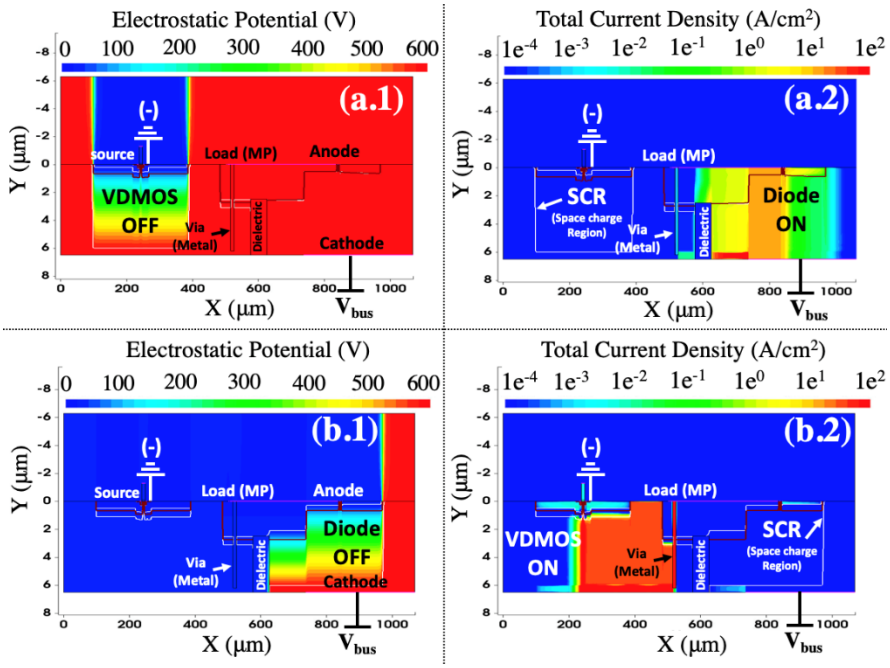

Fig. 5. Equipotential lines and current density distribution in the Boost-type switching cell. (V_{bus} = 600V)

Fig. 5 gives the corresponding distribution of equipotential lines and current density within the elementary boost-type chip. In the cases (a.1) and (a.2) one can notice that the JBS diode is in ON-state and the VDMOS is in off-state and supports the voltage of 600 V. On the other hand, if the VDMOS is ON and the diode is off (Fig.5.b), the JBS diode supports a voltage of 600 V (Fig.5.b) and the VDMOS carries a current density of 100 A/cm2 (Fig.5.b). In all cases the maximum electric field peak value inside the structures does not exceed 2.1 MV/cm which is lower than the critical electrical field in SiC (~2.5 MV/cm [11]).

Fig. 6 shows the VDMOS drain-source and gate-source voltage/current waveforms, together with JBS anode-cathode voltage/current waveforms within both Buck-type and boost-type switching cells. A voltage of 600 V is applied between the MOSFET drain and the JBS anode. A 10A load current is applied between the JBS anode and the midpoint (MP) which is connected to the metal via. An equivalent trapezoidal gate-source voltage was imposed from 0 to 15 V (Vgs > Vth) with a rise/fall time (T_{switch}) of 10µs. This time was used to ease the convergence of the simulations and to reduce the computation time. Indeed, this allowed to divide by almost four the simulation time as compared to the case of using rise/fall times of the order of ns. The observed voltage/current waveforms within the VDMOS/JBS-diode in the buck/boost switching cells confirm the correct operation of the monolithically integrated switching cells.

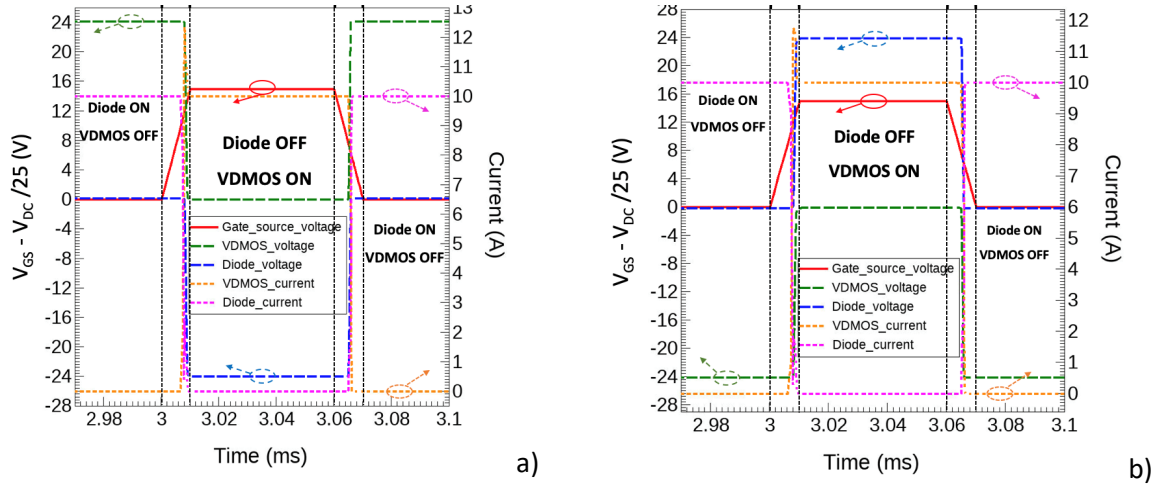

Fig.6. MOSFET-part and JBS-part switching waveforms of the proposed 3-pole Buck (a) and Boost-type (b) switching cell at V_{DC} = 600V, I_{LOAD} = 10A, V_{GSmax} = 15V, T_{CASE} = 300K.

Development of specific technological bricks

Deep trench insulation by fluorinated plasma and electrochemical etching. A first key technological step has been developed to insulate vertically the individual integrated transistors and diodes. Electrical insulation using a deep trench etched in the back-side and a p-type highly doped, deep well, created above this trench is introduced. P^+-type layers are created by aluminum ion implantation and high temperature activation annealing [12].

The trench in the back-side of SiC wafers is created by mask patterning, fluorinated plasma etching and electrochemical etching utilizing p-type created wells as stopping layers to selectively etch the N^+-substrate (Fig. 7)

Both dry plasma and wet electrochemical etching are needed to entirely etch the thick N^+ substrate. The fluorinated plasma (SF_6) is created in a MU400 Plassys Inductively Coupled Plasma/ Reactive Ion Etching reactor (ICP/RIE) and KOH wet solution is used during the electrochemical process. Set-up presentations and optimized parameters utilized are detailed in our previous published article [13].

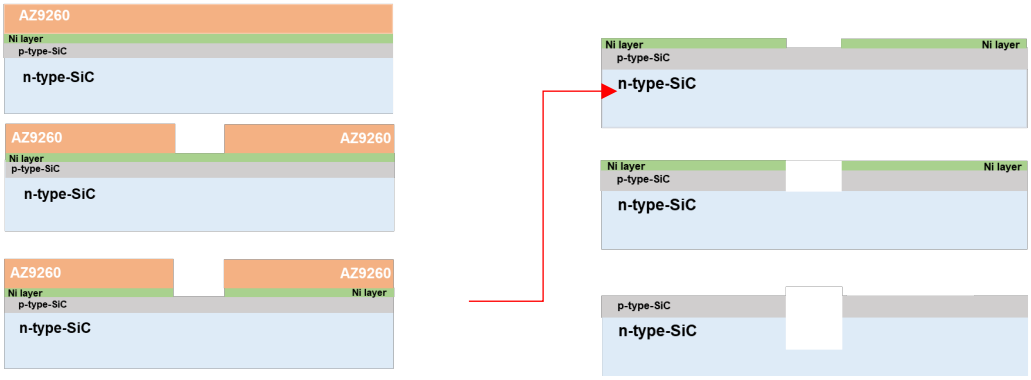

Fig. 7. Steps involved in patterning the n-type SiC substrate with p-type SiC utilized as masks during electrochemical etching.

Comparing the two dry and wet etching processing steps, higher rates are obtained by wet electrochemical process and the masks are inert during the entire process. Nevertheless, in this case etching direction is difficult to control and tilted trenches are obtained instead of the vertical ones we can obtain by ICP/RIE SF_6 plasma (Fig 8). By plasma, the etching rates are limited to 1µm/min and the Ni mask consumption requires the repetition of steps.

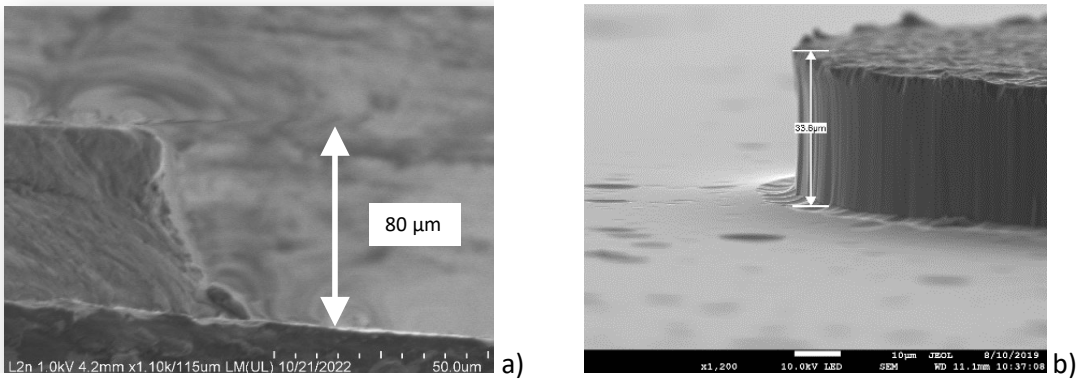

Fig. 8. Scanning electronic microscopy (SEM) images of tilted trenches etched by KOH electrochemical process (a) compared to vertical ICP/RIE fluorinated plasma etched ones (b).

Surface states are also very different, very smooth surfaces are obtained by ICP/RIE SF_6 plasma while by KOH electrochemical etching, rough surfaces are obtained (Fig 9) as the etching mechanism is based on the porosification of the SiC substrate [13].

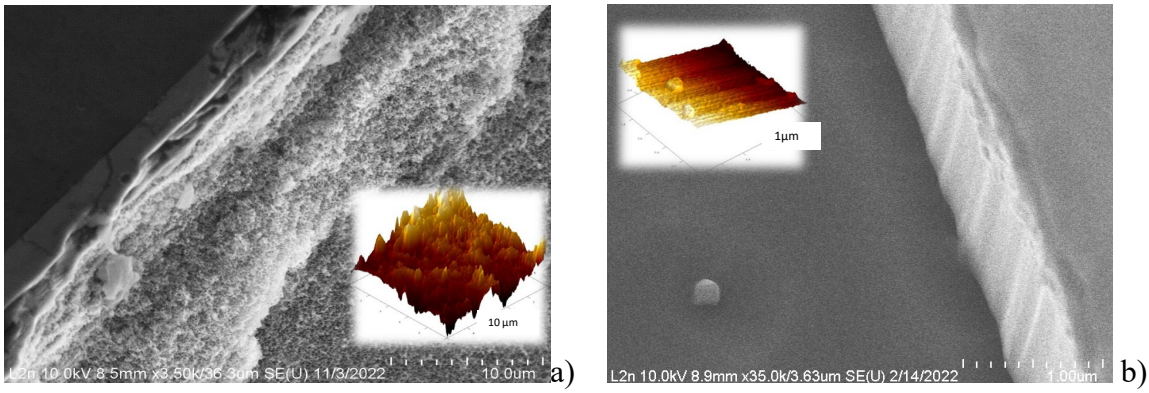

Fig. 9. SEM images of surface states, at the trench bottom and sidewalls after etching by KOH electrochemical process (a) compared to ICP/RIE fluorinated plasma one (b). The inserts are surfaces topographies obtained by AFM (atomic force microscopy).

A post-etching smoothing treatment could be helpful by high temperature annealing and/or oxidation, paying attention to their compatibility with the entire process of the proposed monolithic multi-terminal chips.

Integration of the top metal via contact. A second key technological step has been developed for the Buck and Boost structures. A via in trench is created in the front-side by fluorinated plasma etching, filled with Ni metal by electroplating to connect the VDMOS and the JBS from one side to the other of the SiC wafer (Fig. 4). Ni is preferred to Cu due to the MOSFET process compatibility. We focus on Ni also because Ni is currently used to take ohmic contacts on N^+ SiC substrates.

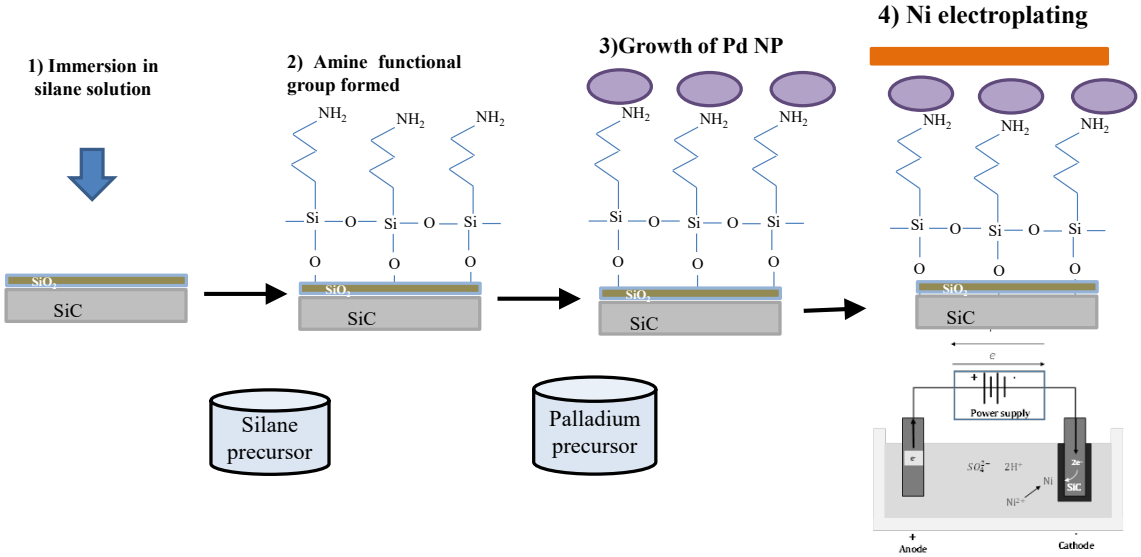

Fig. 10. Functionalization of SiC surface to stabilize the Ni electroplating process to fill the contact via.

High adhesive layer of electroplated Ni metal layer has been obtained by functionalizing the SiC surface. The process is detailed in Fig.10. This adhesive metal layer has been stabilized through growing palladium nanoparticles on the thin silicon oxide layer natively presented on the silicon carbide substrate. An intermediate step has been also inserted with 3-Aminopropyl triethoxysilane (APTES) and using hydroxyl group formed with O_2 plasma treatment [14]. A Ni thickness superior to the via depth (6µm) have been obtained (Fig 11)

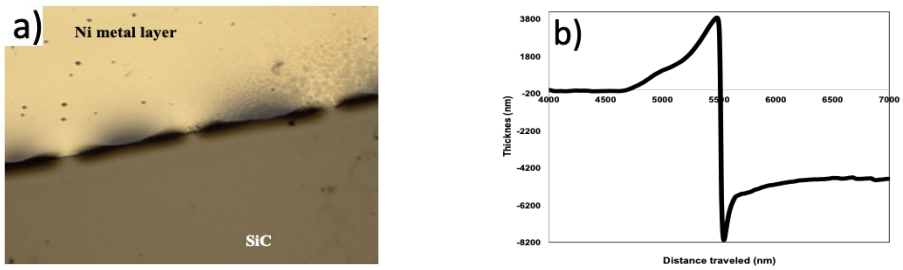

Fig. 11. Optical image of the Ni electroplated layer on the SiC (a) and α-step measurement of the Ni metal layer performed (b).

Conclusion

A new and original design perimeter for monolithic integration of H-bridge power converter on SiC substrate is explored. To that end, we have designed monolithic multi-terminal power chips integrating VDMOS devices as well as multi-terminal power chips integrating switching cells consisting of VDMOS and JBS diode. Using 2D Sentaurus^{TM} simulations, the operating modes of the 3-terminal Buck-type and Boost-type switching cells within one switching cycle were validated.

To fabricate these new monolithic integrated architectures, we developed two main technological bricks, for vertical insulation and for the integration of a top metal via, using Ni both as a mask for SiC etching and to fill the via up. Electrochemical etching in KOH is also necessary to increasing the etching rate for the thick N^+ substrate.

Currently, several runs are under fabrication to validate experimentally the concept

Acknowledgments

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References

[1] Z. J. Shen: *SiC Research Beyond Power MOSFET: What's Next?* IEEE Power Electronics Magazine Vol. 8, no. 2 (2021) p. 14.

[2] H. Yamaguchi et al., 3D-PEIM International Symposium Osaka, Japan, 2021, p. 1.

[3] S. Tanimoto and K. Matsui: *High Junction Temperature and Low Parasitic Inductance Power Module Technology for Compact Power Conversion Systems* IEEE Transactions on Electron Devices Vol. 62, no.2 (2015) p. 258

[4] M. Okamoto, A. Yao, H. Sato, S. Harada: *First Demonstration of a Monolithic SiC Power IC Integrating a Vertical MOSFET with a CMOS Gate Buffer* ISPSD International Symposium, Nagoya, Japan (2021) p. 71.

[5] A. El Khadiry, A. Bourennane, F. Richardeau: *Converter Integration in Si: Dual-Chip and Ultimate Monolithic Integrations* IEEE TED, Vol. 63, no. 5 (2016) p. 1977.

[6] A. Lale, A. Bourennane, F. Richardeau, N. Videau: *Three Multiterminal Silicon Power Chips for an Optimized Monolithic Integration of Switching Cells: Validation on an H-Bridge Inverter*," IEEE Trans Electron Devices, Vol. 66, no. 12 (2019) p. 5238.

[7] V. Soler, *Design and Process Development towards an Optimal 6.5 kV SiC Power MOSFET*, Phd Thesis, Universitat Politècnica De Catalunya Barcelonatech (2019).

[8] M. Cabello, V. Soler, G; Rius, Josep Montserrat, J. Rebollo, P. Godignon, *Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review*, Materials Science in Semiconductor Processing, Vol. 78 (2018) p. 22.

[9] K. Han et al. *Monolithic 4-Terminal 1.2 kV/20 A 4H-SiC Bi-Directional Field Effect Transistor (BiDFET) with Integrated JBS Diodes* 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria (2020) p. 242

[10] Sentaurus TCAD Simulation Tool by Synopsys Inc. Version U 2022.12-SP1.

[11] O Slobodyan, J. Flicker, J. Dickerson, et al. *Analysis of the dependence of critical electric field on semiconductor bandgap* Journal of Materials Research Vol. 37 (2022) p. 849

[12] M. Lazar, F. Laariedh, P. Cremillieu, D. Planson, J.-L. Leclercq: *The channeling effect of Al and N ion implantation in 4H–SiC during JFET integrated device processing* Nucl.Instrum.Method Phys.Res.B Vol. 365 (2015) p. 256.

[13] N. Beydoun, M. Lazar, X. Gassman: SiC Plasma and Electrochemical Etching for Integrated Technology Processes Rom. J. Inf. Sci. Technol. Vol. 26 (2) (2023) p. 238p.

[14] D.-G. Kurth and T. Bein: *Thin films of (3-Aminopropyl) Triethoxysilane on Aluminum Oxide and Gold substrates* Langmuir Vol. 11 (1995) p. 3061