

Comparing 4H-SiC NPN Buffer Layers by Epitaxial Growth and Implantation for Neural Interface Isolation

Scott Greenhorn^{1,2,3,a*}, Edwige Bano^{2,b}, Valérie Stambouli^{1,c},
Konstantinos Zekentes^{2,3,d}

¹Laboratoire des Matériaux et de la Génie Physique, Grenoble INP, France

²Institut de Microélectronique Electromagnétisme et Photonique et le Laboratoire d'Hyperfréquences et de Caractérisation, Grenoble INP, France

³Foundation for Research and Technology – Hellas, Greece

^ascott.greenhorn@grenoble-inp.fr, ^bedwige.bano@grenoble-inp.fr,

^cValerie.Stambouli-Sene@grenoble-inp.fr, ^dtrifili@physics.uoc.gr

Keywords: Isolation, P-N junction, neural interface

Abstract. 4H Silicon Carbide multichannel neural interface devices using NPN junctions for channel isolation were fabricated using four different doping structures. Two devices used thicker, lower-doped epitaxial layers, one used thin, highly-doped implanted layers implanted into a N epilayer, and one used thin-highly-doped implanted layers into an N substrate. The devices were characterized in terms of resistance, charge delivery, leakage current through the substrate, and crosstalk between channels. The thickest, lower-doped epitaxial layers performed best, resulting in great isolation and good performance. While the implanted layers showed high charge delivery, their resistance is reduced due to the thin layers and the isolation is particularly poor.

Introduction

As neural interface technologies develop and begin to show their clinical potential, there is a need for multichannel devices with higher channel density, biocompatibility, and longer working life compared to current devices [1]. Silicon carbide, due to its high chemical inertness, mechanical strength, and variety of electronic properties [2], allows the fabrication of thin, flexible, and robust neural interfaces [3-4]. Despite these material advantages, it is still necessary to ensure and further optimize the basic device functionality. In particular, the low voltages associated to electric potentials in the brain require devices that are highly sensitive to small currents, with high signal-to-noise ratio and low leakage. Of particular interest for scaling multichannel neural interface devices is leakage current between independent measurement channels or from external electronics into the device through substrate layers.

A common strategy for isolating SiC neural interfaces is to use NPN doped layers as a buffer, with back-to-back diode structures to prevent the flow of current [4-6]. These structures can allow low leakage current on standard wafer technology and with conventional processing techniques. This study seeks to characterize different 4H-SiC NPN buffer structures formed by epitaxial growth and by ion implantation in order to optimize the buffer structure for future devices. Three structures are tested in the current study: E1, an epitaxial structure with low doping and thick layers, E2, an epitaxial structure with higher P level doping but thinner layers, and I1, with a very thin, high-doped NPN structure implanted in a low-doped epitaxial layer (Table 1).

Table 1. Sample details for the epitaxial and implanted layers under study

Demo #	E1	E2	I1A350	I1A950	I2
Origin	NovaSiC	NovaSiC	ASCE NT	ASCENT	ASCENT
N++ layer (um)	2.5	0.59	0.35*	0.35*	0.27
N++ layer doping	1E19	1E19	1E21*	1E21*	1 ^E 21*
N layer (um)		0.54			
N layer doping		1.5E17			
P isolation layer (um)	10	2.2	0.7*	0.7*	0.35*
P layer doping	1E16	1E19	1E18*	1E18*	1 ^E 19*
N layer (um)			18	18	
N layer doping			1E15	1E15	
Mesa Depth (um)	5	4	3,0	3,0	3,0
Etched to	P epi	substrate	N epi	N epi	substrate
Post metal deposition RTA?	950°C 2 mins	950°C 2 mins	350°C 2 mins	950°C 2 mins	950°C 2 mins
Ni Metal Height** – before RTA (nm)	180	150	105	105	100
Metal Height** – After RTA (nm)	460	200	250	250	195

*denotes implanted layer, with target thickness and doping obtained from ion implantation simulations.

Experimental

The devices are fabricated by etching the conductive N channels from the top layer of the stack using reactive ion etching, removing the entire N and some of the P layers in the non-channel regions. Ni electrodes are then deposited on part of the top N layer by sputtering, leaving 5 μm between the edge of the structure and the metal pad. The samples are then annealed for 2 minutes using Rapid Thermal Annealing (RTA), at 950°C for the epitaxial samples and 950°C or 350°C for the implanted samples (I1A950 and I1A350, respectively).

Devices are first tested by measuring the resistance between the pad and the electrode to find the total resistance of the device.

Channel isolation is tested by measuring either the crosstalk between adjacent, unconnected channels (measured pad-to-pad) or the leakage current through the substrate (measured pad-to-substrate). All measurements are undertaken with a Keysight B1500a semiconductor analyzer, varying the applied voltage between two terminals while measuring the current. The crosstalk measurements are taken by measuring the I-V curve between the metal pads on two adjacent channels (Fig. 2, left). The substrate leakage measurements are taken by contacting one metal pad on the surface, and contacting the back face of the substrate using a copper-coated PCB chip with a gold thin film deposited on the surface (Fig. 2, right).

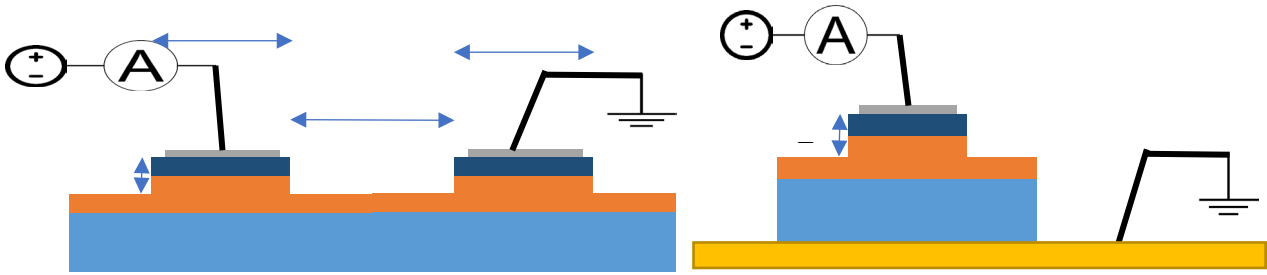


Fig. 2. Diagram of the measurement setups. Left: measuring the crosstalk between two contacts. Right: measuring the leakage through the substrate.

Results

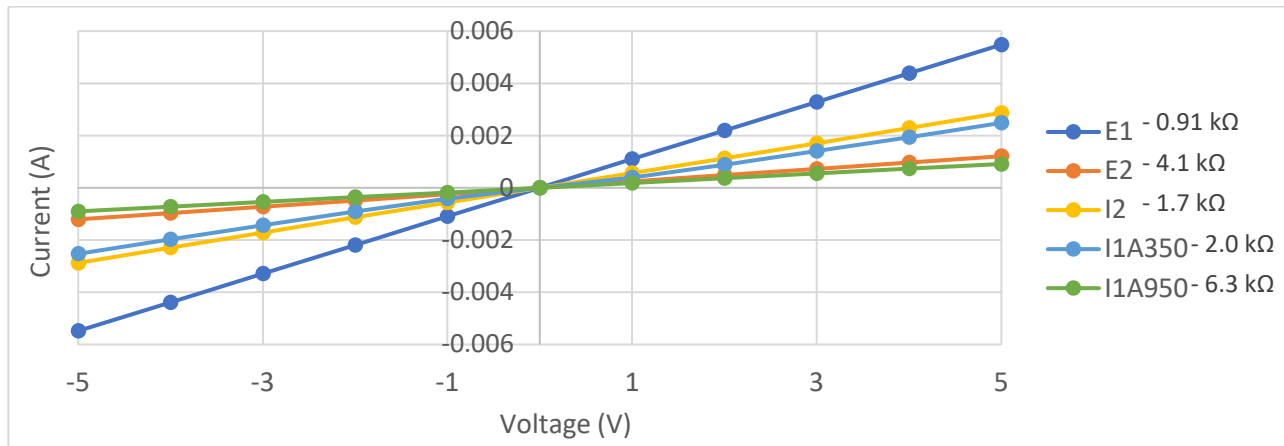


Fig. 3. I-V curves for pad to electrode resistance measurements. The resistance obtained for each device is shown on the right.

Measurements of the device resistance match well with expectations, where the thickness of the top N++ layer as well as the doping fully determine the resistance of the measurements. When the channel lengths are accounted for, the resistivity is highly uniform across all channels, implying a consistent fabrication process. For the case of E2, the results are consistent with the current passing entirely through the top, highly-doped N++ layer rather than the lower-doped N layer immediately below.

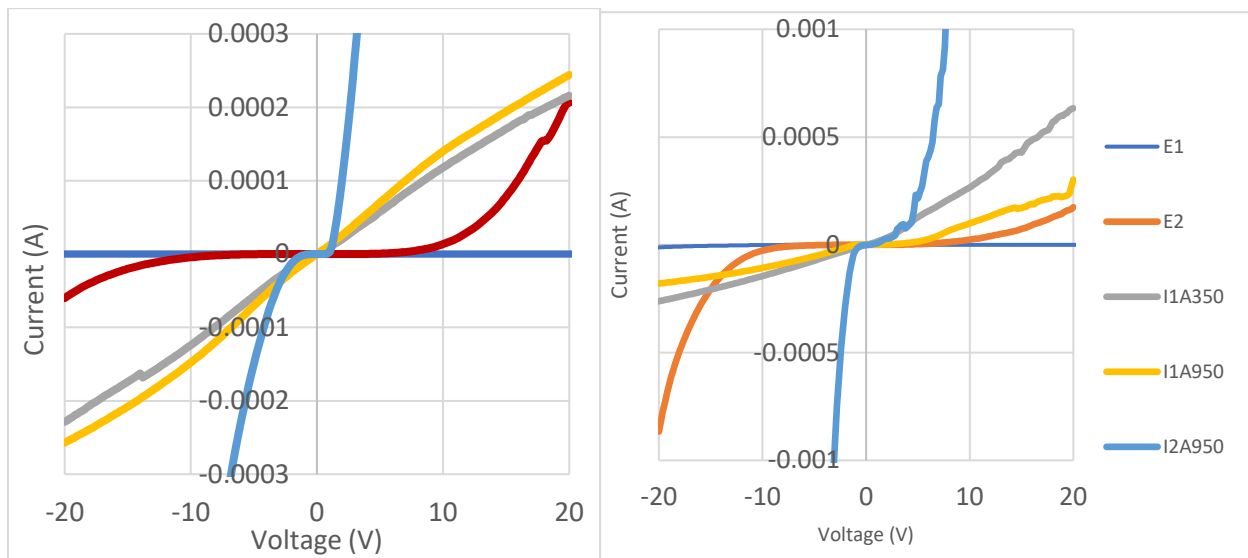


Fig. 4. I-V curves for (left) crosstalk measured between two pads on the N++ layer and (right) leakage through the substrate.

The results show that the thick, low-doped NPN samples E1 provides the best isolation, with no measureable crosstalk (current below 1.5 pA from -20 V to 20V) (Fig. 3) and leakage through the substrate below 15 μ A (Fig. 4). The thinner, higher-doped epitaxial layers show reasonable performance on the range of -5V to 5V, but have crosstalk on the order of 500 μ A and substrate leakage on the order of 1.5 mA for higher voltages.

The sample with ion implantation into the substrate showed minimal current blocking both through the substrate and for crosstalk, blocking current only in a small region between -1 V and 1 V. The sample with ion implantation into an epilayer, and the typical 950°C annealing, showed near-ohmic behavior for both crosstalk and substrate leakage. As the annealing was thought to have consumed a small thickness of the doped layers [7], an additional sample, this one annealed at only 350°C, was tested using the I1 structure. The crosstalk was slightly improved while the leakage through the substrate increased, in addition to a slight improvement in the channel resistance (Fig. 4).

Discussion

The best results overall are achieved using the low-doped epitaxial sample with the thickest layers, which achieves great isolation through the substrate and between channels as well as low channel resistance due to the thicker active layer. However, the charge delivery is poor compared to the implanted samples. In addition, the total thickness of 12.5 μ m for the epilayers limits the thickness (and therefore flexibility) of any future devices based on this technique.

In order to achieve optimal performance, the isolation between the channels must be improved. Due to the limitations of the samples available, tests with low-doped implanted samples or thinner epitaxial samples were not possible, which would provide additional information about the causes for the differences in performance. The isolation performance will depend not just on the thickness of the layers, the annealing, depletion widths, sharpness of the junction boundary, and the presence of defects, all of which are expected to vary significantly between the sample types.

Conclusion

The results of a comparative study of different NPN isolation layers are tested for the application of neural interfaces. Four samples, including two lower-doped epitaxial samples with thicker layers and two higher-doped implanted samples with thinner layers. The resistivity of each sample matches well with expectations considering the changes in thickness and doping. The implanted samples display higher charge delivery in cyclic voltammetry, although the origin of the change (whether due to morphological changes from implantation or higher doping) is not certain. However, the thin layers result in poor isolation, with high current leakage through the substrate and significant crosstalk between channels. More crosstalk is observed for higher annealing temperatures in the implanted samples.

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