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Modeling the Charging of Gate Oxide under High Electric Field

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Abstract. Accelerated aging in reliability testing of gate oxides often involves application of high electric fields well above use case conditions. For wide bandgap devices, for example silicon carbide metal-oxide field effect transistors (SiC-MOSFETs), the barrier between SiC and the gate oxide, typically silicon dioxide (SiO2), is rather small and will thus cause large Fowler-Nordheim (FN) currents and an increased charge trapping rate during reliability testing. Thus, to assess the reliability of SiC-MOSFETs, it might prove useful to better understand the high field charging behavior.

We fabricated planar and trench MOS-capacitors, using an oxide deposition process and post oxidation anneal that is known to be prone to anode hole injection. Voltage ramps were measured at different constant ramp speeds at 25 °C and at 175 °C. Additionally, we performed constant voltage stress measurements.

The measured voltage ramps were fitted with the FN-equation in the low-field range, where no significant charging is expected. Deviation from the fitted equation at high fields is believed to be due to charging of the oxide, which causes a non-homogenous electric field within the gate oxide. We adapt the rate equations from [1] to model and fit the measured IV-curves using an explicit forward approach.

Using the model, we can explain the hump in the current observed during constant voltage stress, corresponding to an average of electric field strength of 7.5 MV/cm, typical for time-dependent dielectric breakdown (TDDB) experiments. The model also shows the strong inhomogeneity of the electric field due to anode hole injection during the initial phase of TDDB, which might cause deviations when extrapolating accelerated aging tests to use conditions. We therefore recommend to slowly ramp up the voltage with a slope <100 mV/s before starting the constant voltage stress phase. This allows for the recombination of the trapped holes to catch up with the anode hole injection and keep steady state conditions. The slow slope also allows some electron trapping before the highest hole concentration is reached, to further reduce the electric field inhomogeneity.

Introduction

The charging of gate oxide in metal-oxide-semiconductor (MOS) devices under high electric field stress is typically observed during measurements to assess gate oxide reliability, using constant or ramped voltage or current stress, and described extensively in literature [1-3]. In a typical experiment the gate oxide charge is determined from a capacitance-voltage (CV)-curve before and after application of stress. Modeling the charging under constant current stress has been successfully done for silicon devices using rate equations for anode hole injection, trapped hole annihilation and electron trapping [1]. For wide bandgap devices, for example silicon carbide metal-oxide field effect transistors (SiC-MOSFETs), the barrier between SiC and the gate oxide, typically silicon dioxide (SiO2), is smaller and therefore the Fowler-Nordheim (FN) current larger at the same applied electric field. The larger current may cause an increased trapping rate, affecting reliability assessment. Thus, to assess the reliability of SiC-MOSFETs, it might prove useful to better understand the high field charging behavior.

The band offset between monocrystalline SiC and SiO_2 depends on the SiC crystal plane. For example, XPS-spectra of thermally grown SiO2 on Si-face show a ~0.3 eV higher barrier than SiO_2 grown on C-face [4]. To check if the charging behavior, apart from the different band-offset, depends on the crystal plane, we compare planar with trench devices.

Sample Fabrication

Planar and trenched capacitors were processed on 4H-SiC epitaxial wafers with a n-doping concentration suited for 1200V MOSFET devices. The oxide was deposited using dry oxidation and subsequently annealed in NO using a process that is known to be prone to anode hole injection. The top electrode on the oxide consists of n-doped poly-crystalline silicon and aluminum contact pads. The active area, defined as the area along the poly-Si/SiO_2-interface, of both planar and trench capacitors was 2.7 mm².

Measurements

We measured IV-curves on the capacitors using different constant ramp speeds ranging from 10 mV/s to 10 V/s. Measurements were performed at 25°C and at 175°C with positive voltage applied to the top electrode. The IV-curves were converted into current density versus applied electric field curves (JE-curves) using the oxide thickness derived from a capacitance measurement from a planar reference device. For each IV curve, we took fresh capacitors from the same wafer. Fig. 1 shows the calculated JE-curves measured with 10 V/s in the high field region, together with the FN-fits described in the next section.

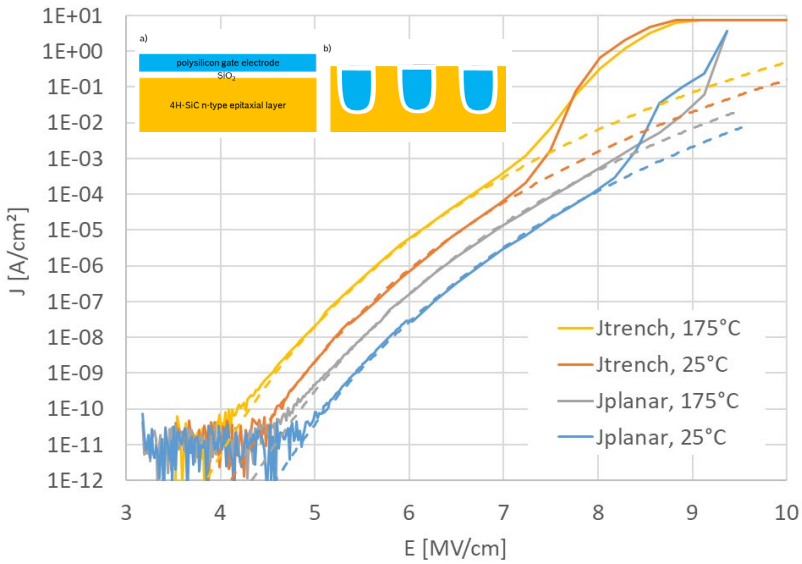

Fig. 1. Calculated gate JE curves (solid lines) from the experimental IV-curves and corresponding fits (dashed lines). Measurement speed was 10V/s in the high field region. Inset shows schematically the cross section of the a) planar and b) trenched capacitors.

We also measured a trench capacitor using constant voltage stress corresponding to an average electric field of 7.5 MV/cm across the dielectric.

Fit of the low-field region of the JE-curves

To allow a better fit of the JE-curves, we replaced the noisy part of the JE-curves measured with low resolution at 10 V/s, with a JE-curve measured with high resolution at 1 mV/s. The cross-over point was at 30 nA/cm². The calculated JE-curves shown in Fig. 1 were fitted in the current density range 100 pA/cm² and 10 µA/cm² using the standard Fowler Nordheim equation, assuming a relative effective electron mass of 0.43 [5]. The fit results are listed in Table 1.

Table 1. Fitted parameters from the FN-curves in Fig. 1. For definition of the parameters see [5].

Capacitor type	Temperature [°C]	A [A/MV²]	B [MV/cm]	m_e/m_o	Barrier height [eV]
planar	25	3×10^4	149	0.43	2.23
trench	25	3×10^4	188	0.43	2.60
planar	175	3×10^4	138	0.43	2.12
trench	175	3×10^4	177	0.43	2.50

Modeling charge trapping at high electric fields

To model charge trapping within the oxide volume we use a rate equation,

$$q\frac{dp}{dt} = \left[\sigma_p(N_p - p)\alpha(E_2) - \sigma_{ep}p\right]J_e(E_1)\,, \tag{1}$$

for anode hole trapping and recombination of trapped holes with conduction band electrons as proposed by DiMaria for silicon MOS-devices [3]. Here N_p is the concentration of hole traps, p is the concentration of free holes, q the elementary charge, σ_p the hole capture cross section, σ_{ep} the electron-hole recombination cross section, α the anode hole injection probability and J_e the electron current density. We calculate J_e using the FN-equation with the parameters from Table 1 and the electric field at the SiC/SiO_2-interface determined from the space charge distribution using the Poisson equation. Fig. 2. illustrates that depending on oxide charge state the electric field at the SiC/SiO_2-interface E_1 may be higher or lower than the electric field at the poly-Si/SiO_2-interface E_2.

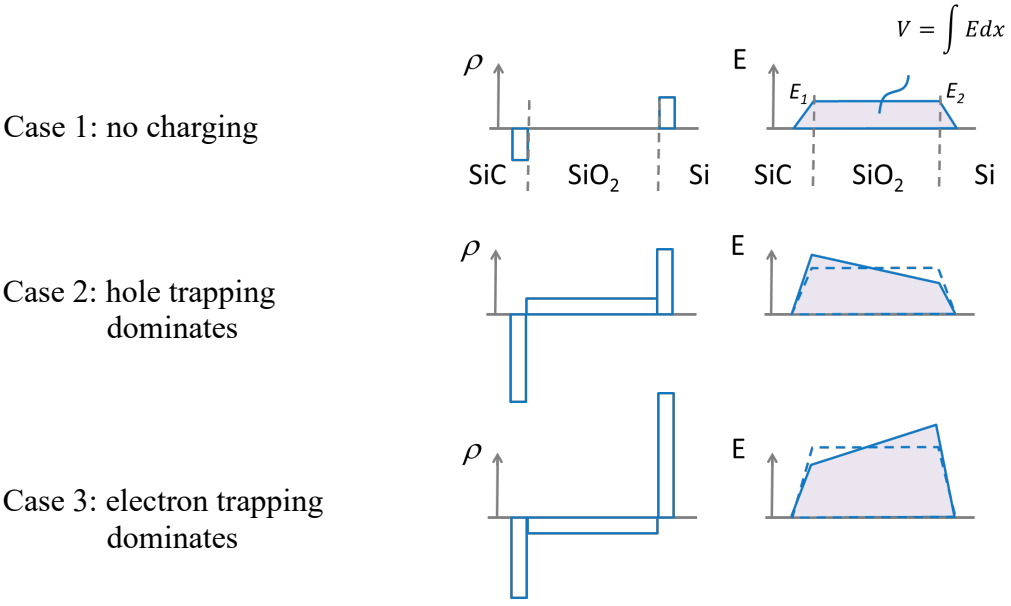

Fig. 2. Schematic drawing to explain the inhomogeneous electric field distribution due to charging of the oxide volume.

In steady state equilibrium between anode hole injection and electron-trapped hole recombination, dp/dt=0, equation (1) simplifies to

$$p_{ss} = \frac{1}{1+\frac{\sigma_{ep}}{\sigma_p\alpha(E_2)}}N_p\,, \tag{2}$$

where p_{ss} is the steady state hole concentration. We also include electron trapping in traps with insignificant recombination, as for example in shallow conduction band traps. Assuming the number of trap states is much larger than the number of trapped electrons we may write

$$q\frac{dn}{dt} = \sigma_e N_e J_e(E_1) \tag{3}$$

for the electron trapping rate. Here n is the number of free electrons, σ_e the electron capture cross section and N_e the number of electron traps. We will call the product $\sigma_e N_e$, the total electron capture cross section. We assume that the trapping cross sections are independent of applied field and that trapping occurs homogeneous across the oxide volume. Fig. 3 illustrates the different trapping mechanisms described by the above equations. We will fit the electric field dependence of the anode hole probability, using a simple expression with two positive parameters X and Y,

$$\alpha(E_2) = \frac{1}{1+e^{-X(E_2-Y)}}, \tag{4}$$

that exponentially approaches zero for low fields and approaches unity for high electric fields.

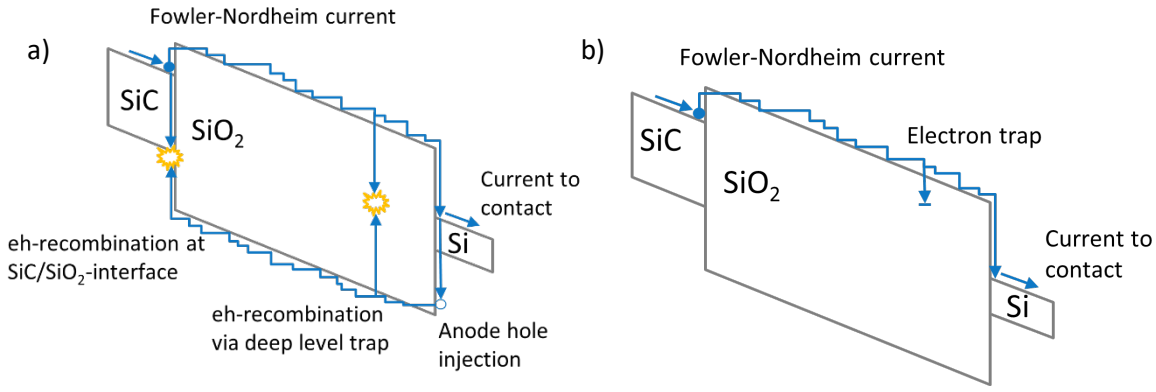

Fig. 3. Band diagram illustrating different charge trapping mechanisms used in modeling the JE-curves. a) dynamic equilibrium between anode hole generation and recombination with electrons in the conduction band. b) electron trapping in rather shallow traps with negligible cross section for eh- recombination.

We solve the rate equations numerically using the explicit forward approach. We start at zero voltage with no charge within the oxide volume and ramp up the voltage in discrete time steps. At each timestep we calculate the accumulated charge using the transient rate equations. However, when the transient solution approached the steady state solution, we encountered convergence problems. We solved this problem by switching to steady state when the hole concentration was within 1% of the steady state solution. Fig. 4 shows 4 sets of curves measured from planar and trench capacitors at 25 °C and 175 °C. To account for slight variation in oxide thickness between the capacitors used to compare the effects of different ramp speeds, we scaled the horizontal axis of JE-curves such that all curves, cross the JE-curve of the capacitor measured at 10 mV/s at 100 nA/cm². In each set of curves we used 4 different ramp speeds and each of the curves is also fitted using the rate equations. The fit results are listed in Table 2. Fitted IV-curves with parameters from Table 1 are also included as a reference case without oxide charging. The set of curves measured from trench capacitor at 25 °C show the largest deviation from the reference curve, indicating strong charging effects. In contrast to that, the planar capacitor at 175 °C shows least deviation from the reference curve.

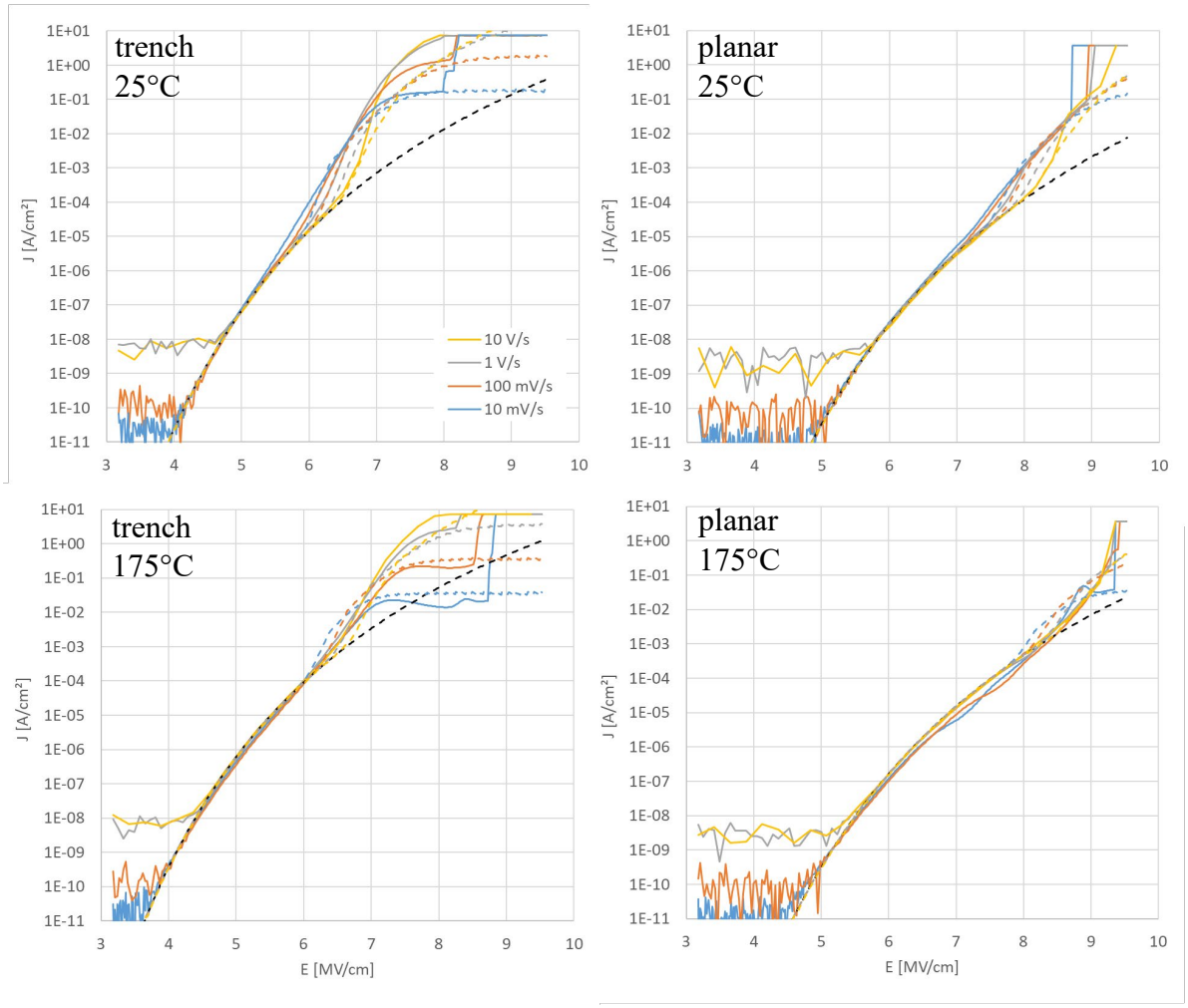

Fig. 4. Measured (solid lines) and fitted (dashed lines) IV curves obtained with different constant voltage ramp speeds. Fitted IV-curves from Fig. 1 (black dashed lines) are included as a reference for the case without oxide charge.

Fig. 5a shows the result from constant voltage stress measurement where the current density drops over several orders of magnitude. The little hump after 1 h could be fitted quite well using the values in Table 2. Fig. 5b shows that the slope of the electric field, extracted from the fitted numerical solution, switches sign during the constant voltage stress measurement.

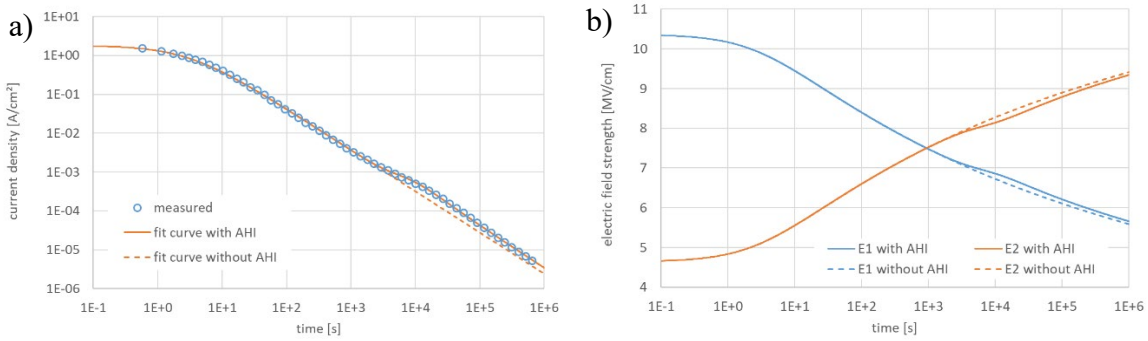

Fig. 5. Results from a constant voltage stress measurement on a trench capacitor with 7.5 MV/cm at 25 °C. Measured (open circles) current density and fitted curves assuming anode hole injection (solid lines) and assuming no anode hole injection (dashed lines). a) measured and fitted current density over time. b) fitted electric field strength at location E_1 and location E_2.

Table 2. Fit results for voltage-ramp and constant voltage stress measurements.

Parameter	V-ramp 25°C	V-ramp 175°C	CVS 25°C
hole capture cross section trench	4×10^{-11} cm²	1×10^{-12} cm²	7×10^{-20} cm²
hole capture cross section planar	2×10^{-13} cm²	5×10^{-16} cm²	
eh-recombination cross section	5×10^{-19} cm²	5×10^{-19} cm²	3.6×10^{-21} cm²
hole trap concentration	8×10^{18} cm^{-3}	8×10^{18} cm^{-3}	1.2×10^{18} cm^{-3}
Total electron capture cross section	2×10^{-3} cm^{-1}	1×10^{-2} cm^{-1}	7×10^{-3} cm^{-1}
AHI parameter *X*	8 cm/MV	8 cm/MV	8 cm/MV
AHI parameter *Y* trench	8 MV/cm	8 MV/cm	8 MV/cm
AHI parameter *Y* planar	9 MV/cm	9 MV/cm	

Discussion

The FN-current density of the trench capacitors observed in Fig. 1 is much higher than the FN-current density from the planar capacitors. As these devices were manufactured on the same wafer with the same oxide process, we believe that the oxide thickness is quite similar and maybe somewhat smaller oxide thickness for the trench devices because of lower gas concentrations within a trench. Scanning electron microscopy (SEM) did not show significant smaller thickness for trench devices that could explain the difference in current density. The curvature of the SiC/SiO_2 interface is not expected to give rise to an increased current for the trenched capacitors because the FN-interface is on the stretched outside border of the curved oxide layer corresponding to lower field line density and thus lower electric field strength. XPS-spectra of thermally grown SiO_2 on Si-face show a ~0.3 eV higher barrier than SiO_2 grown on C-face [4]. So, it is likely that the crystal plane of the trench could have a lower FN-barrier than the Si-side top surface. Also, roughness of the trench sidewall may contribute to the higher FN current density. We observed strong lateral micro-roughness when viewing the photolithographic trench mask after etching and this will be reproduced in the trench sidewall when trenching the SiC epitaxial layer. Thus, we assume that the combination of different crystal plane and higher roughness is responsible for the higher current density in trenched capacitors.

The measured current density for trench capacitors beyond 10 A/cm² at 25°C at 8 MV/cm could not be reproduced with the model. One possible explanation is that, at these high field strengths, we have avalanche current additional to the FN-current. Due to the strong inhomogeneity of the internal field strength, the probability for local avalanche might be strongly increased. Ignoring avalanche may also contribute between different fit results from constant voltage stress and voltage ramp. As the fit results match the measurement results only roughly qualitatively, we must be careful with interpreting the fit parameters. Obviously, the model needs to be improved. Apart from including avalanche, maybe the assumption of inhomogeneous charge distribution is too restrictive. The difference in the fit results between trench and planar capacitors is quite striking and unexpected, because apart from the interface, we expect the same oxide bulk parameters and the same poly-Si/SiO2 interface. We may only speculate about the cause. Micro-roughness of the trench interface could cause local enhancement of electric field and inhomogeneous charging along the trench sidewall. Annealing of the poly-Si may be different within trench and on the top side because of different layer thickness and different thermal contact to the substrate. In the model, we ignored both interface traps and near interface traps, assuming that they do not charge or discharge in strong accumulation beyond 5 MV/cm. Several publications suggest that NO-anneal causes hole traps within the oxide volume [6, 7]. Maybe the difference of the SiC/SiO_2 transition zone in planar and trench cause a difference in defect states that may affect charging of the oxide.

The model shows strong inhomogeneity of the electric field due to anode hole injection during the initial phase of the constant voltage stress measurement, with a voltage, corresponding to an average electric field strength of 7.5 MV/cm, typical for time-dependent dielectric breakdown (TDDB). The inhomogeneous electric field strength might cause deviations when extrapolating accelerated aging

tests to use conditions. To avoid excessive internal electric field strength during TDDB, we recommend to slowly ramp up the voltage with a slope <100 mV/s before starting the constant voltage stress. This allows for the recombination of the trapped holes to catch up with the anode hole injection and keep steady state conditions. The slow slope also allows some electron trapping before the highest hole concentration is reached to further reduce the electric field inhomogeneity.

After the initial phase of the constant voltage stress measurement, the current drops over several orders of magnitude. This current drop shows a distinct hump after 1 hour of stress and is explained by the model as an increase of anode hole injection due to electron trapping, causing an increase in electric field strength at the poly-Si/SiO_2 interface. This explanation may also apply to the little hump observed at 8 MV/cm in the voltage ramp with 10 mV/s of the trench capacitor at 175°C. The current at that point is much lower than the reference FN-curve without charging, indicating strong electron trapping and thus increasing probability for AHI.

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