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Temperature Dependence of 4H-SiC Gate Oxide Breakdown and *C-V* Properties from Room Temperature to 500 °C

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Abstract. Silicon carbide (SiC) is intrinsically more suitable for high temperature operation than silicon. However, for devices and circuits based on metal-oxide-semiconductor, high temperature behavior of gate oxides is still under investigation. This work aims to provide insights on how temperatures from room temperature up to 500 °C affect gate oxide properties of metal-oxide-semiconductor structures. Characterization is performed by current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements with different SiC and polysilicon gate electrode doping types. Increasing breakdown voltages were observed with higher temperatures for n-type SiC doping, while p-type ones break down at lower voltages. Polysilicon doping type only has minor impact on the breakdown voltage but influences the *I-V* behavior. High temperatures increase the probability of strong inversion being observable in *C-V* investigation. Regarding the *I-V* results, it can be stated that the 55 nm gate oxide used in the utilized HT CMOS technology has breakdown voltages above absolute values of around 55 V, independent of any doping types, and no significant current could be observed within the intended 20 V operation range of the technology.

Introduction

Wide-bandgap materials like silicon carbide (SiC) exceed bulk silicon's (Si) temperature operation limit of around 200 °C, making them in principle suitable for high temperature (HT) metal-oxide-semiconductor (MOS) field effect transistors (MOSFETs) and, thus, for high temperature complementary MOS (CMOS) circuits [1]. An example of an important material property for SiC HT operation is the lower thermal generation of electron-hole pairs compared to Si, which results in a significantly lower intrinsic carrier concentration [2, 3].

Gate oxide properties on 4H-SiC are well known from vertical power MOSFETs up to around 200 °C. Above that temperature, literature is scarce. Yu et al. made lifetime predictions for operation at 375 °C [4] and Le-Huu et al. extrapolated thermal gate oxide time to breakdown of over 16 years at 400 °C [5]. However, no direct HT breakdown investigations were presented. When utilizing HT CMOS technology, gate oxide could be a critical point for reliability, especially at higher temperatures. Thus, research on gate oxide properties at temperatures above 400 °C is needed.

Doped polysilicon is considered a promising material for the gate electrode due to the well-known properties of its interface towards the silicon dioxide (SiO_2) gate oxide [6]. It has been previously shown, that a p-doped polysilicon (pPolySi), in comparison to a n-doped polysilicon (nPolySi), will shift the threshold voltage of SiC MOSFETs to more symmetrical values even at temperatures of 500 °C [7]. Therefore, HT gate oxide investigations for both polysilicon types are of scientific interest.

This work aims to provide insights on how temperatures up to 500 °C affect gate oxide properties using current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements at 100 kHz on MOS capacitors (MOSCAPs). Additionally, the impact of the doping process and type of the polysilicon gate electrode on the gate oxide properties is investigated.

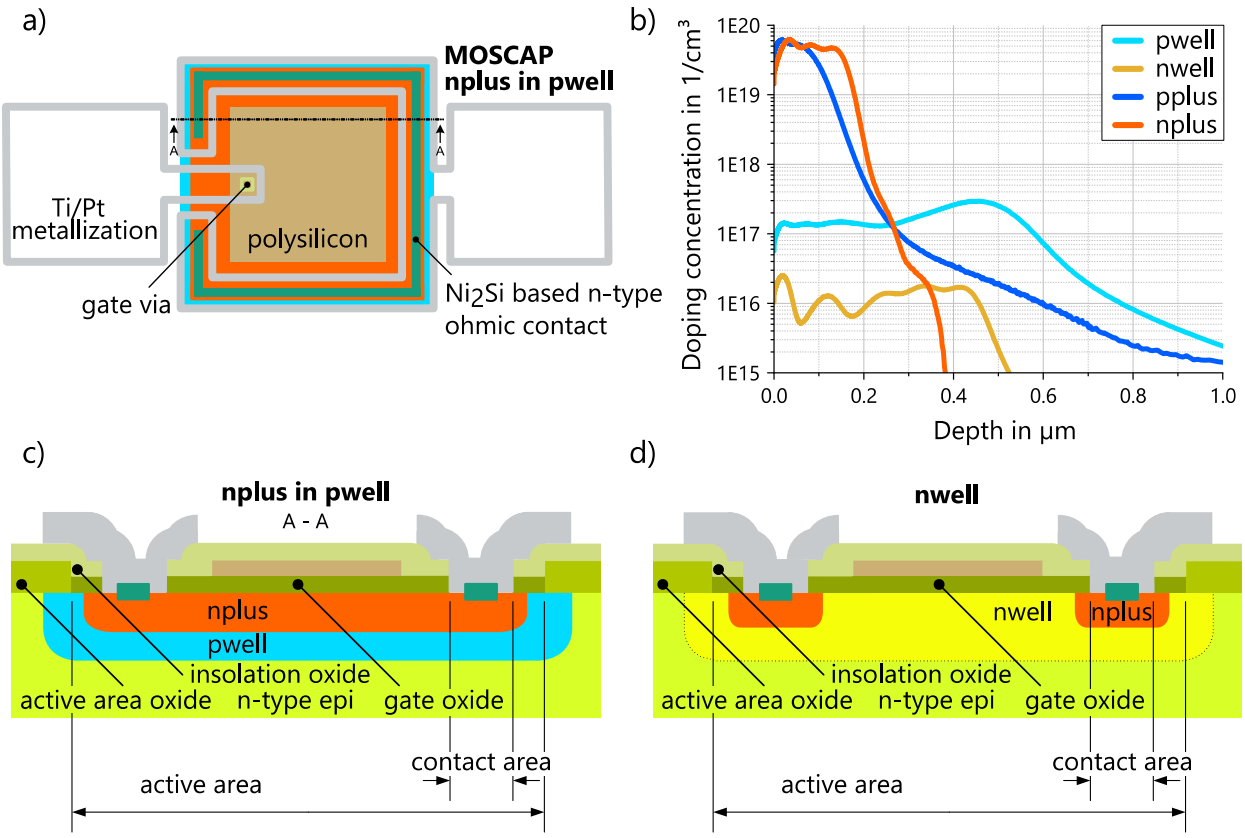

Fig. 1. a) Top view and c) cross view schematics of squared nplus in pwell MOSCAP. d) Cross view schematics of squared nwell MOSCAP. The counterparts with inverted doping types (pplus in nwell & pwell) have matching designs with Ti_3SiC_2 as p-type ohmic contact material. b) Implantation profiles used for the investigated MOSCAP structures with Al for p-type doping and N for n-type one. In a), metallization is depicted by only using borders to allow clear visibility of the layers below.

Sample Fabrication

Squared MOSCAPs, schematically displayed in Fig. 1, were fabricated using IISB's 4H-SiC 2 µm double-well HT CMOS technology, also accessible via EUROPRACTICE IC service [8], which can operate at 500 °C [7]. Utilized doping profiles, in the form of as implanted Monte Carlo simulated graphs using Synopsys Sentaurus Process, are also presented in Fig. 1 b).

A SiO_2 gate oxide with targeted thickness of 55 nm is thermally grown at 1300 °C and annealed in nitric oxide atmosphere at 1300 °C for 60 min to produce a high concentration of nitrogen at the SiC/SiO_2 interface, which is known to reduce interface state density [1].

Differently doped SiC, especially for the high concentration contact implantations nplus and pplus, has varying thermal oxidation rates, causing up to roughly 8 nm thicker oxides on nplus areas.

Polysilicon is used as a gate electrode and both nPolySi and pPolySi are compared on different wafers. Therefore, both in-situ nPolySi and undoped amorphous polysilicon were deposited. The latter was then implanted using Boron and annealed for 20 s at 1070 °C to create pPolySi. During the ohmic contact formation, a second HT step of 1050 °C for 5 min was applied. The fabrication details can also be found in our previous work [7], from which the optimized Boron implantation parameters for the pPolySi of $7.5 \cdot 10^{15}$ cm^{-2} at 50 keV were chosen.

A HT Ti/Pt metallization was utilized to enable operation at 500 °C, provided by a hot plate system during measurement. Electrical characterization was performed using a E4980A precision LCR meter from Agilent and a SCS-4200 from Keithley.

Results and Discussion

Breakdown *I-V* measurements from room temperature (RT) up to 500 °C were performed on five MOSCAP samples for each temperature for both SiC and both polysilicon doping types. Due to sample availability, destructive *I-V* measurements could not be performed on the same device design as *C-V*, which is depicted in Fig. 1 d). Hence, the design in Fig. 1 c) was selected.

Due to being limited to lateral technology and pseudo vertical devices, the MOSCAP geometry is not ideal, however, directly emulating transistor design for nwell and pwell design. This and the temperature dependence of the flat band voltage (V_{FB}) make exact breakdown field correlation not trivial. Thus, current is depicted against applied voltage rather than electric field in Fig. 2, which presents exemplary breakdown *I-V* measurement results at different temperatures from the investigated nPolySi and pPolySi MOSCAP samples.

The breakdown log(*I*)-*V* curves, describing the conduction through the oxide can be separated into different regions [9]. First, no relevant current, is flowing through the gate oxide.

Next, an exponential current increase occurs, visible as linear section due to the logarithmic y-axis. For the presented *I-V* characteristics, injecting extrinsic charge carriers from the SiC or polysilicon bands into the oxide bands is necessary for charge carrier transport to occur. For MOS structures, this usually happens mainly due to tunneling, with the exact mechanisms depending on several conditions such as electric field, oxide thickness and temperature [10].

For direct tunneling, the current flows through the entire oxide and, thus, is excluded for the investigated samples due to the oxide thickness of around 55 nm. The current must overcome only a small barrier instead of the full oxide for Fowler-Nordheim tunneling. Also, Poole-Frenkel emission can occur with current flowing due to random thermal fluctuation occasionally promoting electrons trapped in localized oxide states shortly into the oxide conduction band. Besides being affected by electric field, with larger electric fields reducing the required thermal energy, a rather significant temperature dependency is given[10].

Especially as measurements up to 500 °C are performed, Schottky or thermionic emission can give electrons enough energy to overcome the oxide potential barrier. It is expected to have a significant impact for higher temperatures, potentially replacing tunneling as a dominating mechanism.

Another possible effect influencing the *I-V* characteristics is impact ionization, which can also trigger the avalanche effect mentioned below. This effect is especially relevant for thicker oxides, statistically occurring after roughly 2 MV/cm for the utilized oxide thickness of about 55 nm [11].

From first preliminary estimations, linear regions in a $\ln(I/T^2)$ vs. $V^{0.5}$ Schottky emission plot, the $\ln(I/V)$ vs. $V^{0.5}$ Poole-Frenkel emission plot and a $\ln(I/V^2)$ vs. $1/V$ Fowler-Nordheim tunneling plot suggest all these mechanisms might exist in the samples. Dedicated calculation of each mechanism similar to Murakami et al. [12] in combination with the temperature dependence of multiple variables are required to fully understand the dominating effect and characterize the samples in more detail.

Finally, the section of the *I-V* curve displaying drastically increased current corresponds to oxide destruction by an avalanche multiplication effect, significantly damaging the insolating properties of the oxide. This is followed by another instant current increase of several orders of magnitude, which destroys the oxide permanently, causing polysilicon and SiC to be shorted by a hard oxide breakdown [9].

For all samples, within the normal operation range of our HT CMOS technology up to absolute values of 20 V, no significant current increase is observed, which also proves sufficient oxide quality even for high temperature application. This range is significantly extended for the pPolySi samples compared to the nPolySi ones.

In the second region, both polysilicon types exhibit similar exponential increase behavior for nplus in pwell samples. Temperature change affects the slope, causing a crossing of the *I-V* graphs at roughly 50 V. While the exact reason has yet to be identified, possible explanations could include a change of carrier transport mechanisms in the oxide or in SiC, defect states in the oxide or at the interface, or the non-ideal device geometry. Only for RT pPolySi, a pronounced steep current increase is visible there. It is possible, that either avalanche effects already start occurring, e.g., triggered by impact ionization, or a change in conduction mechanisms happens. For pplus in nwell, no distinct

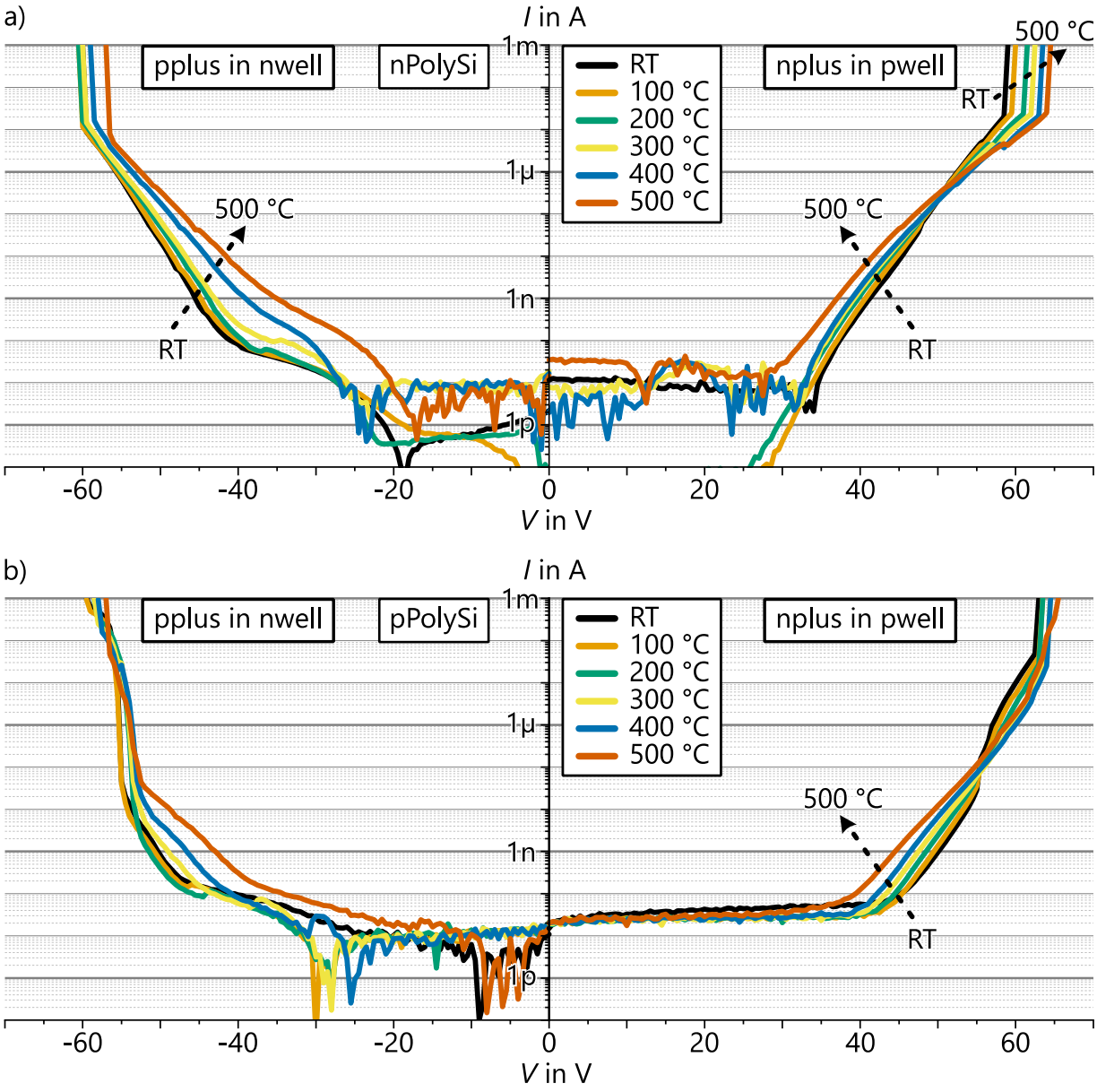

Fig. 2. Breakdown *I-V* measurement results from RT to 500 °C for pplus in nwell and nplus in pwell a) nPolySi and b) pPolySi MOSCAPs with an area of 100 x 100 µm^2.

crossing due to temperature change is visible. In contrast to nPolySi, the avalanche region for pPolySi samples starts at lower voltages. All displayed pplus in nwell samples show higher current values in the exponential increase region at higher temperature, which could be explained by more stress in the oxide induced by higher temperature, damaging the oxide by causing more defect states. This is also the case until the crossing point for the nplus in pwell devices. Above this point, the temperature effect is inverted.

Finally, all plotted curves except pplus in nwell pPolySi show clear breakdown behavior, destroying the oxide and entering measurement compliance. For these, either the breakdown process begins at considerably lower voltages, or a combination of overlapping effects occurs. Utilizing pPolySi compared to nPolySi, the *I-V* curves exhibit considerable differences, likely originating from different physical properties of the polysilicon doping, varying charge carrier transport mechanisms and defects possibly introduced due to the incomparable polysilicon fabrication process.

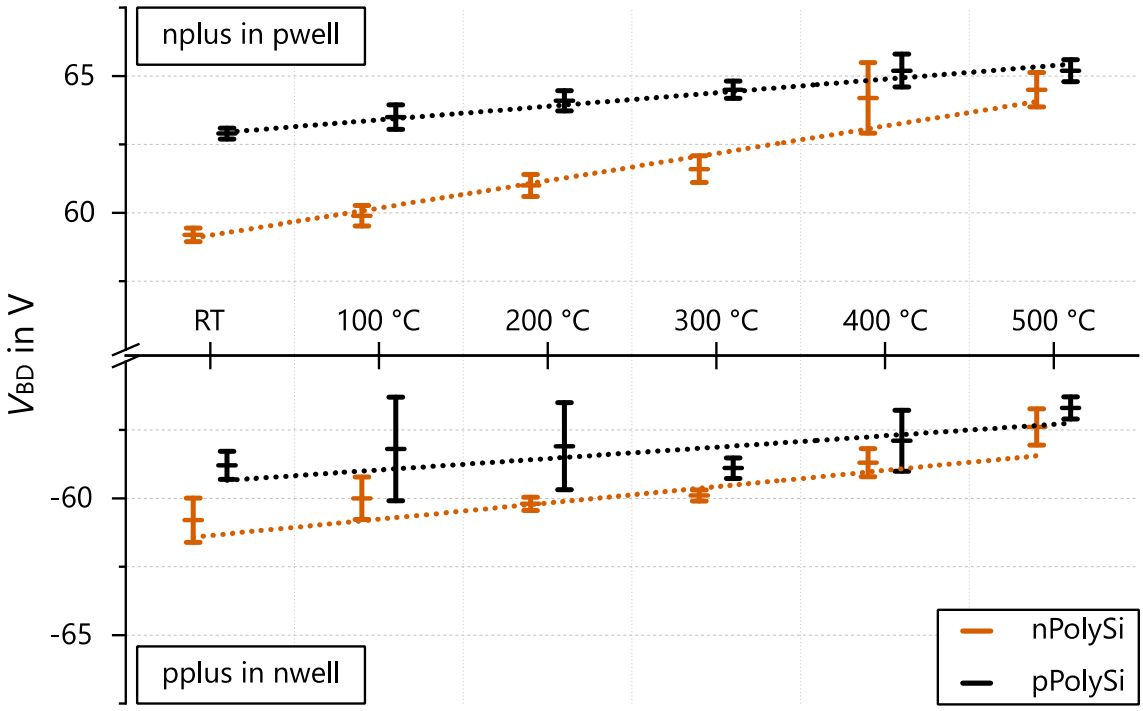

Fig. 3. Breakdown voltage of nplus in pwell and pplus in nwell MOSCAPs from RT to 500 °C for nPolySi and pPolySi. Each data point is averaged from five samples with error bars representing standard deviation. The x-offset between nPolySi and pPolySi data points for each measurement temperature is only for better visualization. The measurement temperature is identical. Dotted lines are a guide to the eye.

Fig. 3 presents the resulting breakdown voltage (V_{BD}) of nplus in pwell and pplus in nwell MOSCAPs with an area of 100 x 100 µm² from RT to 500 °C for nPolySi and pPolySi.

Considering an oxide thickness of 55 to 60 nm, evaluated RT breakdown field is around 10 MV/cm, which proves sufficient oxide quality. With rising temperatures from RT to 500 °C, findings show a V_{BD} increase for n-type nPolySi MOSCAPs, whereas p-type ones break down at lower V_{BD}. This temperature trend is unchanged by using pPolySi. However, V_{BD} values are further shifted to increased values for n-type devices and to lower absolute ones for p-type. For nplus in pwell, this shift is stronger at lower temperatures, whereas apparently far weaker dependence or even independence of temperature for pplus in nwell is visible.

Higher temperature lowering V_{BD} for pplus in nwell could be attributed to temperature induced stress, damaging the oxide. However, more detailed investigation is needed to explain why higher temperatures cause the nplus in pwell devices to break down at higher voltages.

C-V measurement results from RT up to 500 °C were performed on one exemplary MOSCAP sample for both SiC and both polysilicon doping types. Compared to the breakdown samples, the *C-V* ones have a lower SiC doping concentration due to having no contact implantation below the polysilicon. For all *C-V* investigations, the -20 V to 20 V (forward) measurement was performed first, being followed by the 20 V to -20 V (backward) one immediately afterwards.

From the *C-V* results depicted in Fig. 4, V_{FB} values were extracted using forward data for p-type and backward data for n-type doping. For nPolySi nwell, values between -2.0 V for RT and -1.7 V for 500 °C were evaluated. Due to values being nearly constant up to 300 °C with less than 0.1 V difference, it is assumed that there is no temperature dependence until 300 °C. It cannot be clearly stated if the difference of around 0.1 V between 300 °C and 400 °C and between 400 °C and 500 °C each is an indication of a temperature dependence. The evaluated effective series resistance varies from 900 Ω at RT to 1.9 kΩ at 500 °C, which is expected to not influence the presented *C-V* measurement results. V_{FB} evaluation was performed utilizing a fixed doping concentration of $2 \cdot 10^{16}$ cm^{-3}. All fixed concentrations were assumed from the doping profile simulation displayed in Fig. 1b).

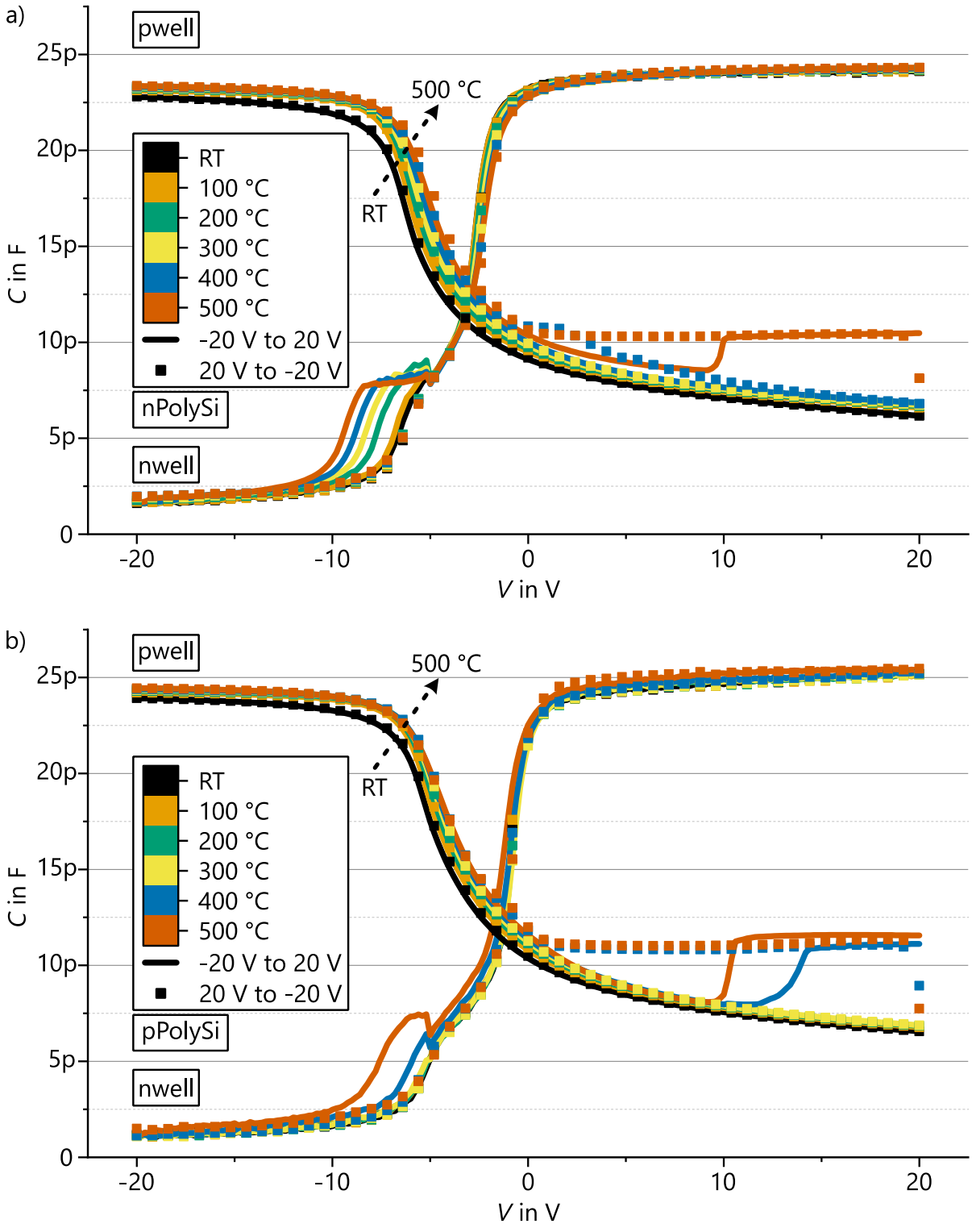

Fig. 4. *C-V* measurement results at 100 kHz from RT to 500 °C for nwell and pwell a) nPolySi and b) pPolySi MOSCAPs with an area of 200 x 200 µm². Measurements performed from -20 to 20 V (forward) are displayed as lines and 20 V to -20 V (backward) as squares. For better visibility, only every fourth square is depicted.

For nPolySi pwell, a significant V_{FB} change was noticed. Starting from -7.5 V at RT, a continuous increase to -6.0 V at 500 °C underlines an existing temperature dependence contrary to the nwell MOSCAPs. In addition, a decrease in series resistance from 9.6 kΩ at RT to 3.5 kΩ was evaluated. Interestingly, the series resistance seems to saturate, showing no major change above 300 °C. This could be attributed to the low ionization rate for Al until around 300 °C and is likely directly related

to the sheet resistance of the pwell and the contact resistance to the pplus implantation. This also makes the evaluation not trivial as the difference to the theoretically expected *C-V* graphs increases. The fixed doping concentration for evaluation was $6 \cdot 10^{16}$ cm^{-3}.

For pPolySi nwell, a shift of around -0.35 V was observed, going from -0.4 V at RT to -0.75 V at 500 °C, with no significant change until above 300 °C. Here, $1.7 \cdot 10^{16}$ cm^{-3} was used as fixed doping concentration value. Series resistance increases from 300 Ω at RT to 1.5 kΩ at 500 °C, comparable with the nPolySi equivalent. Finally, pPolySi pwell, evaluated at a fixed doping concentration of $7.5 \cdot 10^{16}$ cm^{-3}, shows V_{FB} results of -6.5 V at RT and -5.5 V at 500 °C. Series resistance is 8.3 kΩ at RT, decreasing to 2.8 kΩ at 500 °C with almost no change after 300 °C. All four evaluations give oxide thickness values between 54 nm and 59 nm, which is within expectation.

C-V measurement results of nwell nPolySi MOSCAPs follow expected *C-V* behavior for the forward measurement, starting in deep depletion before depletion and finally accumulation. However, the nPolySi sample exhibit a steep capacity increase between around -10 V and -5 V above 100 °C. This is attributed to the generation of inversion charges, reaching strong inversion conditions. As the probability of inversion charge generation increases with higher temperature, a shift towards more negative voltages can be seen. Thus, strong inversion appears for the 200 °C to 500 °C samples. The transition between strong inversion, when occurring, and depletion happens at nearly identical voltage values. This transition is also superimposed by the fact that the space charge region at very low voltages extends into the n-epi but is fully located in the nwell region from -6 V on, making evaluation complex. The backwards measurements do not show the temperature dependent strong inversion effect.

For nPolySi pwell MOSCAPs, forward *C-V* measurements start in accumulation and transition into depletion before entering deep depletion. Only for 500 °C, strong inversion condition can be observed from around 10 V towards higher voltages. Due to pwell having around one order of magnitude higher doping concentration than nwell, and Al doped regions featuring higher defect density compared to N doped ones, inversion requires more minority carriers to be generated, thus occurring at higher temperatures. The backwards measurements are identical up to 300 °C. For 500 °C, as we exit the forward measurement in strong inversion, the device maintains in this strong inversion state at the start of the backward measurement until the SiC surface is no longer in strong inversion conditions. The 400 °C backward measurement starts in deep depletion but exhibits the begin of inversion charge generation at around 10 V, deviating from the forward results. The measurement results show strong inversion at around 1 V before transitioning to depletion afterwards.

The pwell *C-V* curves appear to be slightly temperature dependent with higher capacities at higher temperature, especially for the lower temperature values. One possible reason could be incomplete ionization of the implanted and annealed Al doping, which causes higher series and contact resistance, which in turn might result in a decrease of the apparent oxide capacitance.

In comparison to nPolySi, pPolySi *C-V* results only have slight differences. The nwell MOSCAP shows inversion charge generation only from 400 °C onwards compared to 200 °C for nPolySi. However, this difference is expected to not origin from the different polysilicon doping but from the statistic nature of the thermal generation rate of electron hole pairs, which depends on e.g., temperature and defect concentration in SiC. Small differences can already be observed across the wafer due to varying defect distribution. With the polysilicon split being on different wafers, small deviations in measurement temperature, defect distribution and epitaxial layer concentration are given. Increasing the *C-V* measurement points to four times as much will expose the device longer to a voltage regime where band bending basically allows inversion charge generation. The start of the inversion charge generation can then already be observed at lower voltages (not shown here), which is attributed to a higher statistical chance due to elongated time for generation.

The pPolySi pwell MOSCAP has slightly higher capacity values for accumulation and strong inversion conditions compared to according nPolySi MOSCAPS, presumably due to the difference in doping concentration and oxide thickness. This is also the case for nwell accumulation capacities. Strong inversion condition, already visible at the end of the pPolySi pwell forward measurement results for 400 °C, is likely also due to statistics from defects, temperature, and charge carrier lifetime.

Summary

To recapitulate, the temperature dependence of gate oxide characteristics has been investigated up to 500 °C, featuring increasing V_{BD} for MOSCAPs of both 4H-SiC doping types. *C-V* measurement results indicate a temperature dependence of strong inversion condition, occurring at higher temperatures in a more distinct way.

Using pPolySi instead of nPolySi, V_{BD} at lower temperatures require higher voltage values but no major differences were observed at 500 °C. The *I-V* curves do exhibit considerable differences. Reasons could include different physical charge carrier transport mechanisms and defects possibly introduced during the pPolySi fabrication process. Furthermore, its impact on *C-V* results is limited, increasing the absolute accumulation capacity slightly and possibly affecting the inversion conditions minorly.

Bringing to attention, no significant current increase is observed for the *I-V* results of all samples within the intended operation range up to absolute values of 20 V, which also proves its sufficient quality even for high temperature application.

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