Solid State Phenomena
ISSN: 1662-9779, Vol. 358, pp 65-70
doi:10.4028/p-Hs3sD9

Submitted: 2023-07-16
Revised: 2024-04-08
Accepted: 2024-04-08
Online: 2024-08-21

A Voltage Adjustable Diode Integrated SiC Trench MOSFET with Barrier Control Gate

Songjun Li[1,a], Xiaochuan Deng[1,2,b*], Xu Li[1,2,c], Xuan Li[1,d] and Yi Wen[1,2,e]

[1]School of Electronic Science and Engineering, University of Electronic Science and Technology of China, China

[2]Institute of Electronic and Information Engineering of UESTC in Guangdong, China

[a]songjun.li@foxmail.com, [b*]xcdeng@uestc.edu.cn, [c]lixu0612@foxmail.com
[d]andrew_xuanli@foxmail.com [e]wenyi@uestc.edu.cn

Keywords: SiC MOSFET, voltage adjustable diode, bipolar degradation, third quadrant

Abstract. Bipolar degradation of the intrinsic bipolar body diode is one of the most important reliability problems associated with SiC MOSFET. In this paper, a voltage adjustable diode (VAD) integrated SiC trench MOSFET (VAD-TMOS) with barrier control gate (BCG) is proposed to overcome this issue. Compared to the intrinsic bipolar body diode of conventional SiC trench MOSFET (C-TMOS), VAD has 57% reduction of the on-state voltage drop. Furthermore, the reverse recovery charge (Q_{rr}) of VAD-TMOS is only 1.21 μC/cm^2, whereas the value of C-TMOS is 3.84 μC/cm^2. The miller charge (Q_{gd}) of VAD-TMOS is reduced by about 6 × in comparison with that of C-TMOS owing to the reduction of the overlap region of gate and drain terminal. The better third quadrant and fast switching capability make SiC VAD-TMOS a potential candidate as a next generation of power switch.

Introduction

Trench gate silicon carbide metal oxide semiconductor field effect transistor (SiC MOSFET) with low specific on resistance is widely used in the electric vehicle, photovoltaic inverter, uninterruptible power supply [1]. However, the electric field in the gate oxide of the SiC trench gate MOSFET is very high in the blocking state, which can cause long term reliability problems [2]. The P- shield region at the trench bottom is introduced to protect the gate oxide in SiC trench gate MOSFET [3].

The parasitic body diode in SiC MOSFET could be utilized as a freewheeling diode in power converter circuits [4]. However, the forward on-state voltage drop (Von) of the parasitic body diode is as high as 3 V. And even worse, the recombination energy produced by the bipolar conduction of the body diode could induce the expand of Shockley Stacking Fault (SSF), which not only significantly increase Von but also the reverse leakage current of SiC MOSFET [5].

In this paper, a voltage adjustable diode integrated SiC trench MOSFET (VAD-TMOS) with barrier control gate (BCG) is proposed to mitigate the bipolar degradation in the third quadrant of device operation and improve high frequency switching capability. An N-channel layer beneath the barrier control gate is utilized to form a lower electron barrier height between the N^+ source region under gate oxide and the N-drift region, which is controlled by the applied barrier control gate bias and provides a new route for electron transit when VAD-TMOS works in the third quadrant.

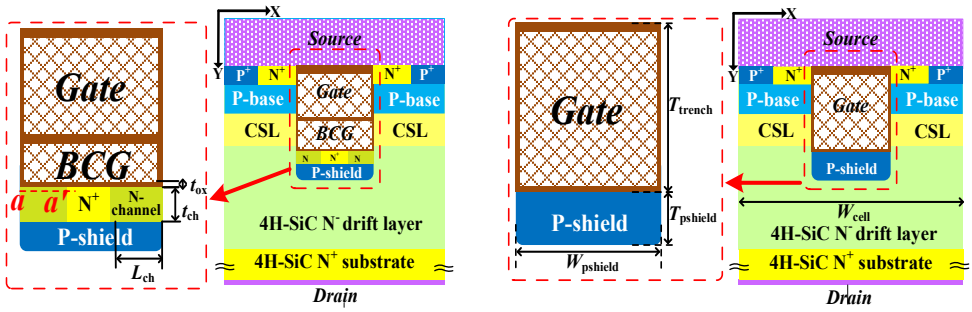
Device Structure and Mechanism

Fig. 1 illustrates the cross-section view of proposed VAD-TMOS and conventional SiC trench gate MOSFET with grounded P-shield (C-TMOS). Compared with C-TMOS, the main features of VAD-TMOS consist of an integrated voltage adjustable diode and a barrier control gate, which avoids the activation of parasitic body diode when VAD-TMOS works in the third quadrant. The basic parameters of VAD-TMOS and C-TMOS are kept same for a fair competition, as shown in Table I.

Table I. Device parameters for TCAD simulation

Parameters	VAD-TMOS	C-TMOS
T_{drift}/N_{drift}	11 μm/8×10^{15} cm^{-3}	11 μm/8×10^{15} cm^{-3}
N_{CSL}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
$T_{P\text{-}base}/N_{P\text{-}base}$	0.5 μm/2.8×10^{17} cm^{-3}	0.5 μm/2.8×10^{17} cm^{-3}
T_{trench}	1.3 μm	1.3 μm
$T_{p\text{-}shield}/N_{p\text{-}shield}$	0.5 μm/2×10^{18} cm^{-3}	0.5 μm/2×10^{18} cm^{-3}
$W_{p\text{-}shield}$	1.5 μm	1.5 μm
N_{ch}	2.5×10^{16} cm^{-3}	-
L_{ch}	0.50 μm	-
t_{ch}	0.20 μm	-
t_{ox}	40 nm	40 nm
W_{cell}	3.5 μm	3.5 μm

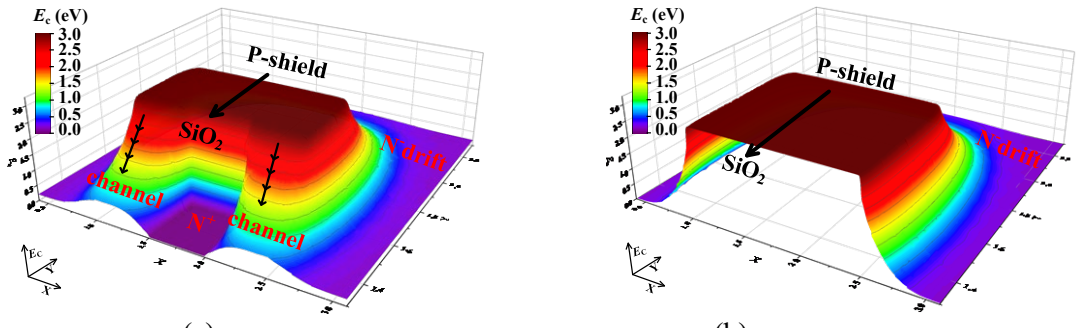
The polysilicon gate of VAD-TMOS is divided into two parts. The upper part is the gate electrode, and the lower part is the barrier control gate. The grounded P-shield at the trench bottom is used to protect the trench gate oxide from high electric field successfully in the blocking state and avoid charge storage effect during switching operation [6]. A current spreading layer (CSL) is also used to eliminate JFET pinch-off effect. In VAD-TMOS, an N type layer with doping concentration of 2.5×10^{16} cm^{-3} and thickness of 0.2 μm forms an accumulation channel between grounded N$^+$ source region and N-drift region. The doping concentration of accumulation channel is carefully designed, so it can be fully depleted by P-shield to ensure the blocking characteristics. The P-shield of both VAD-TMOS and C-TMOS and the N$^+$ Source under BCG electrode of VAD-TMOS is connected to the Source electrode.



(a) (b)

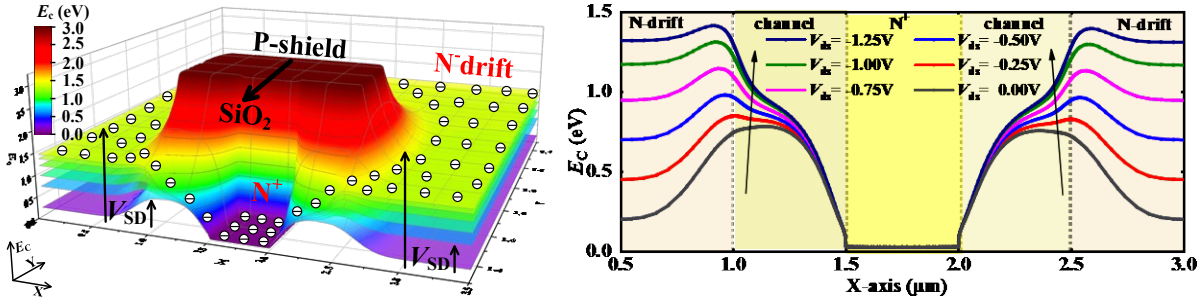
Fig. 1. Cross section views of (a) VAD-TMOS and (b) C-TMOS

Fig. 2 shows the 3D diagram of conduction band energy E_C for VAD-TMOS and C-TMOS at zero bias. It is clear the E_C of VAD-TMOS at SiC/SiO$_2$ interface (*a-a'* in Fig. 1 (a)) is significantly lower than that of C-TMOS. At the SiC/SiO$_2$ interface, the maximum value of E_C is the barrier height $q\Phi_{Bn}$ of electrons from drain to source terminal.



(a) (b)

Fig. 2. Three-dimensional *Ec* distribution of (a) integrated VAD and (b) parasitic body diode of C-TMOS at zero bias voltage.

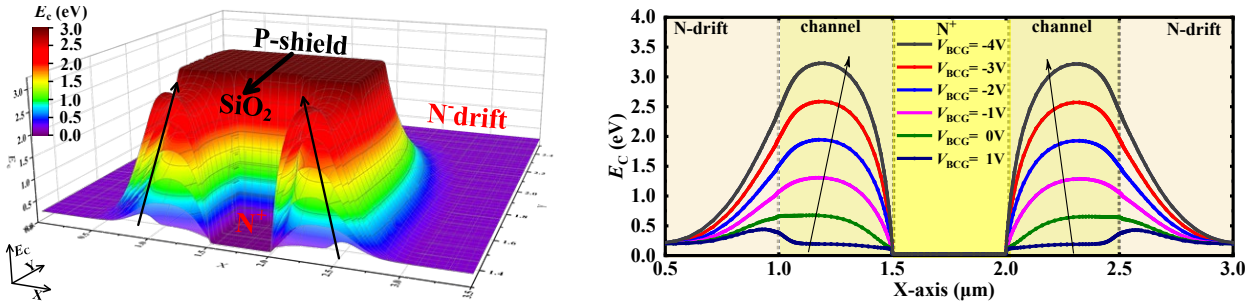


(a) (b)

Fig. 3. (a) Three-dimensional E_c distribution of VAD and (b) E_c distribution along SiO_2/SiC interface (*a*-*a*' in Fig. 1 (a)) with different V_{ds}

Fig. 3 illustrates the conduction band energy E_C distribution of VAD-TMOS at different drain to source voltage (V_{ds}). It is demonstrated that the electron energy associates with the decrease of V_{ds}. When electron energy is more than the potential barrier height of 0.7 eV at SiC/SiO_2, electrons could cross the barrier and flow directly into the N^+ source, instead of crossing the high barrier in the P-shield. This makes VAD-TMOS achieve much lower V_{on} than C-TMOS.

The BCG electrode is applied to adjust the barrier height $q\Phi_{Bn}$ of integrated VAD to minimize V_{on} for third quadrant operation. As shown in Fig. 4, when the bias voltage of BCG (V_{BCG}) increases from - 4 V to 1 V, the potential barrier height $q\Phi_{Bn}$ decreases from 3.3 eV to 0.2 eV.



(a) (b)

Fig. 4. (a) Three-dimensional *E*c distribution of VAD and (b) *E*c distribution along SiO_2/SiC interface (*a*-*a*' in Fig. 1 (a)) with different V_{BCG}

The relationship between $q\Phi_{Bn}$ and V_{BCG} can be described by the following equation.

$$q\Phi_{Bn} = -V_{BCG}\frac{q\varepsilon_{SiC}t_{ox}}{\varepsilon_{ox}t_{ch}+\varepsilon_{SiC}t_{ox}} + q\left(\chi_{Si\_SiC} + \frac{2\phi_{Si\_SiC}\varepsilon_{SiC}t_{ox} - N_{ch}t_{ox}t_{ch}^2}{2\varepsilon_{ox}t_{ch}+\varepsilon_{SiC}t_{ox}}\right) \quad (1)$$

Where $q\chi_{Si\_SiC}$ and $q\Phi_{Si\_SiC}$ are the difference of conduction band energy and work function between poly Si and SiC P-shield. ε_{SiC} and ε_{ox} are permittivity of SiC and SiO_2.

Results and Analysis

Fig. 5 (a) shows the influence V_{BCG} on the barrier height of VAD. It is found that $q\Phi_{Bn}$ is linearly decreases with the reduction of V_{BCG}. It should be noted that this model is in good agreement with the simulation results, except when V_{BCG} is greater than 1V. This is because we assume the accumulation channel was fully depleted in the model. But when V_{BCG} is greater than 1V, the channel is not fully depleted.

Fig. 5 (b) compares the performances of VAD-TMOS and C-TMOS in both the first and third quadrants. The $R_{on,sp}$ of VAD-TMOS and C-TMOS at V_{GS}=20 V and I_{DS}=100 A/cm^2 are almost the same, which are 1.89 mΩ·cm^2 and 1.84 mΩ·cm^2, respectively. However, the V_{on} of VAD-TMOS at I_{ds}=-100 A/cm^2 and V_{BCG}=0 V is only 1.48 V, whereas the C-TMOS is 3.52 V. Different from C-

TMOS, in VAD-TMOS, the current in the third quadrant does not flow from the P^+ Source electrode and P-shield Source electrode to the N-drift region and then into the Drain electrode, but flows from the N^+ region below the BCG electrode through the N-channel layer into the N-drift region and finally into the Drain electrode.

Fig. 5 (c) shows the electron current and hole current of VAD-TMOS in the third quadrant when V_{BCG}=0 V. Compared with electron current, the hole current of VAD-MOSFET is negligible. Fig 5 (d) illustrates the hole distribution of VAD-TMOS and C-TMOS at I_{ds}=-100 A/cm^2 and V_{BCG}=0 V. There is no hole injection in the drift region of VAD-MOSFET. The above analysis of VAD-TMOS and C-TMOS shows that there is no undesirable bipolar conduction in VAD-TMOS during the third quadrant operation. Therefore, the proposed VAD-TMOS successfully avoids bipolar degradation of the parasitic body diode.

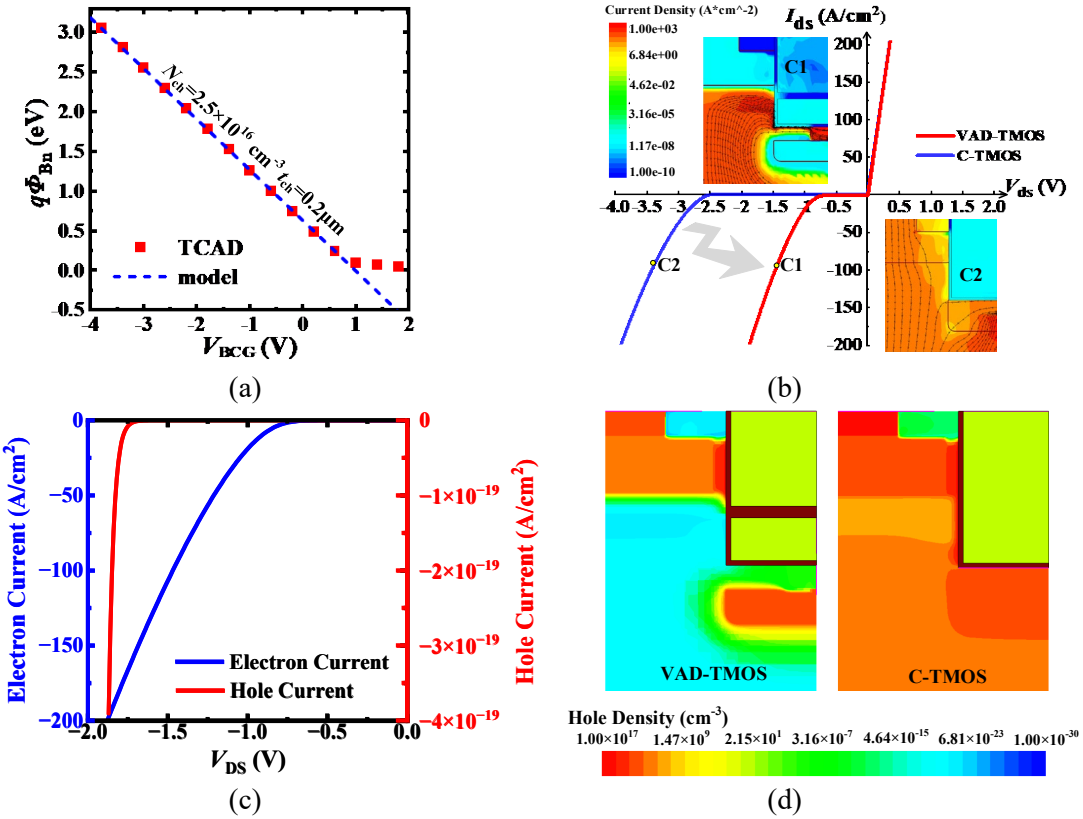
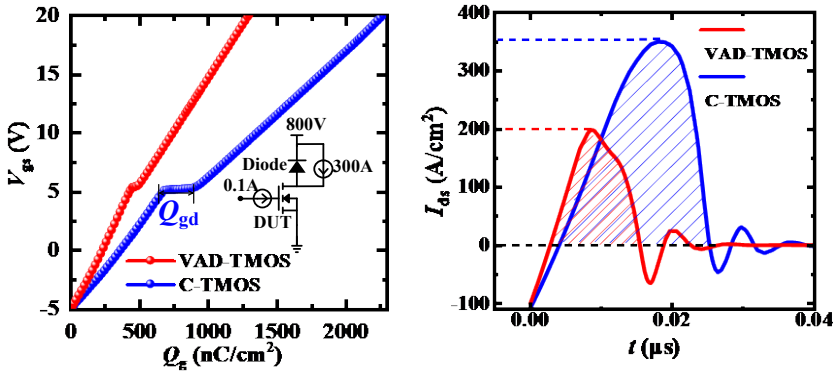


Fig. 5. (a) Comparison of $qΦ_{Bn}$ calculated from the model and extracted from the simulation at different V_{BCG} and (b) Performance Comparison in the first and third quadrant of operation for the optimum VAD-TMOS and C-TMOS. In the inset is shown the current distribution at C1 and C2 and (c) Electron current and hole current of VAD-TMOS in third quadrant and (d) hole distribution of VAD-TMOS and C-TMOS at I_{ds}=-100 A/cm^2 and V_{BCG}=0 V.

The gate charge Q_g of VAD-TMOS and C-TMOS are illustrated in Fig. 6 (a). The Q_g and Q_{gd} of VAD-TMOS is significantly reduced by 43% and 84% in comparison with C-TMOS. Because the barrier control gate reduces the overlap area of gate and drain terminal. These results clearly show VAD-TMOS could improve the high frequency performance. The small reverse recovery current significantly decreases the power loss in the diode, as shown in Fig. 6 (b). The reverse recovery charge (Q_{rr}) of VAD-TMOS is only 1.21 μC/cm^2, whereas charge is 3.84 μC/cm^2 for C-TMOS. This is because VAD is a unipolar diode and there is no recombination of electron and hole in the reverse recovery process.



(a) (b)

Fig. 6. Comparison of (a) Q_g and (b) Q_{rr} between VAD-TMOS and C-TMOS.

The simplified processes used for manufacturing VAD-TMOS devices are briefly described in Fig 7, which include CSL, P-base, P^+, N^+, P-shield and N-channel implantation, trench etch, isolated oxidation, gate oxidation, polysilicon gate deposition and etching, and metallization.

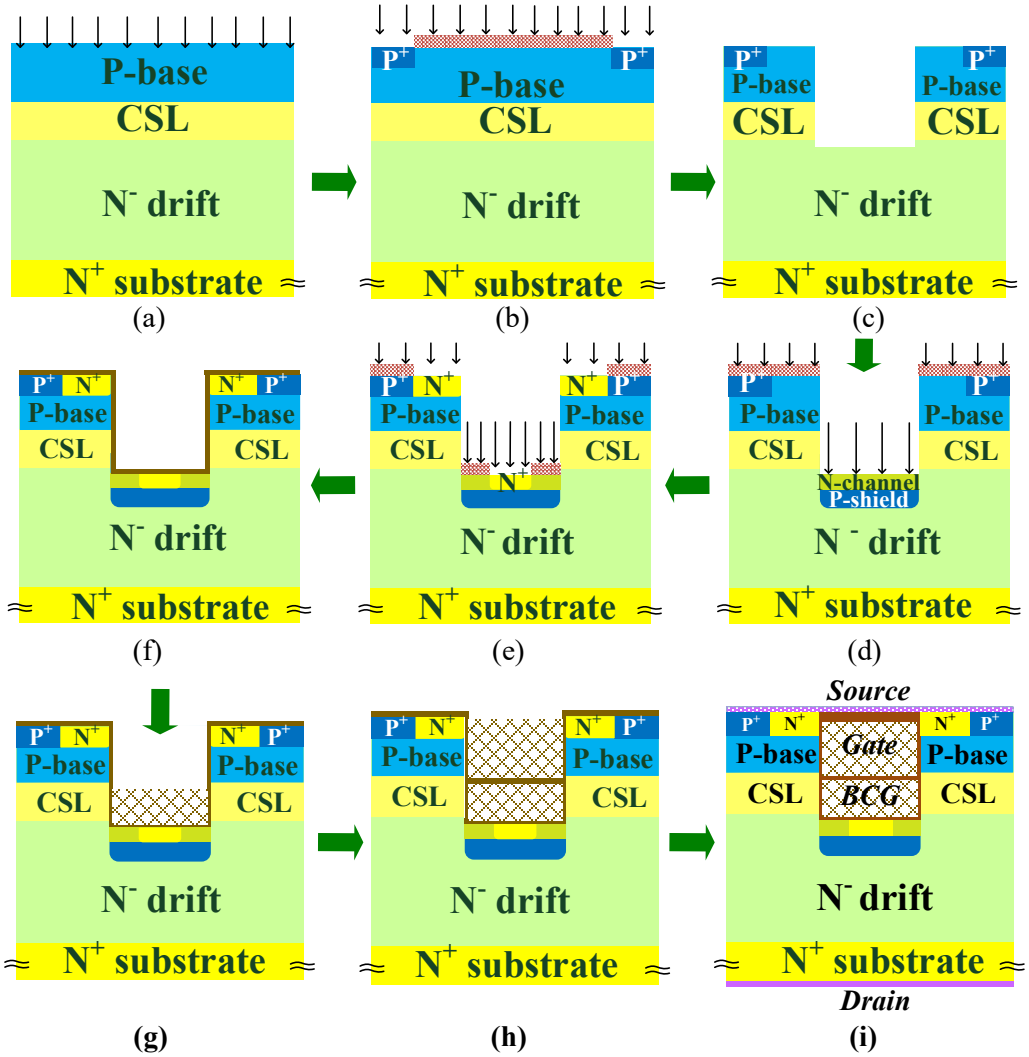


Fig. 7. Fabrication process for the proposed power VAD-MOSFET structure: (a) CSL and P-base implantation; (b) P^+ implantation; (c) trench etching; (d) P-shield and N-channel implantation; (e) N^+ implantation; (f) gate oxidation; (g) polysilicon deposition and etching; (h) isolated oxide and polysilicon deposition and etching; (i) metallization.

Summary

In this paper, a novel SiC trench gate MOSFET with an integrated voltage adjustable diode (VAD-TMOS) is proposed and investigated to improve third quadrant and high frequency performance by using TCAD simulation. A barrier control gate is utilized to control the forward voltage drop of the integrated VAD. Compared with C-TMOS, VAD shows 57% reduction of the V_{on} as well as the improvement in $R_{on,sp}\times Q_{gd}$ by a factor of 6. These results clearly indicate VAD-TMOS is an attractive power device for the next generation power application.

Acknowledgments

The work is partly supported by the Natural Science Foundation of Sichuan Province of China (Grant No. 2022NSFSC0526) and the National Natural Science Foundation of China (Grant No. 61974016) and Guangdong Basic and Applied Basic Research Foundation (Grant No. 2023A1515010538)

References

[1] F. Hoffmann, N. Kaminski and S. Schmitt, Proceedings of the 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Japan, 2021, pp. 175-178.

[2] T. Kimoto, J.A. Cooper, Fundamentals of Silicon Carbide Technology, John Wiley & Sons Singapore Pte. Ltd, Singapore, 2014.

[3] Y. Kitamura, H. Yano, N. Iwamuro, F. Kato, S. Tanaka, T. Tawara, S. Harada and H. Sato, Proceedings of the 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Canada, 2022

[4] Kadavelugu, U. Raheja, M. Mobarrez, E. Aeloiza and R. Rodrigues Proceedings of the IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WIPDA), USA, 2019.

[5] M. Skowronski and S. Ha J. Appl. Phys. 99, 011101 (2006).

[6] J. Wei, M. Zhang, H. Jiang, H. Wang and K.J. Chen, Proceedings of the 29th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Japan, 2017, pp. 287-190.