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Venus Surface Environmental Chamber Test of SiC JFET-R Multi-Chip Circuit Board

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Abstract. This paper describes a first attempt to build and operate a multi-chip prototype lander control and sensor signal digitization electronics circuit board comprised of ten NASA Glenn IC Generation 11 SiC JFET-R IC chips in 460 °C, 9.4 MPa harsh Venus surface conditions. The lander circuit ceased electrical operation prematurely at 107 °C as the Venus chamber heated up. Microscopic post-test inspections indicate that only one of the ten SiC chips on the board failed. Most of circuit-damaging cracks observed on the failed chip corresponded to micron-scale irregularly-shaped dielectric film hillock defects. The study of these defects suggests minor processing changes to eliminate this suspected root failure cause.

Introduction

The demonstrated ability of NASA Glenn SiC junction field effect transistor-resistor (JFET-R) integrated circuit (IC) chips to function for at least 60 days immersed in chamber-simulated Venus surface environment without sheltering [1] offers sea-change improvements to Venus surface missions and scientific exploration [2]. Along with continued upscaling of individual IC functionality, environmental chamber demonstration of multi-chip circuit boards (subsystems) is a logical next step in technology development and maturation compared to single-chip testing of simpler (< 200 transistors/chip) individual NASA Glenn Generation 10 ICs accomplished previously [1]. This paper describes a first attempt to build and operate a prototype circuit board comprised of ten Generation 11 SiC JFET-R IC chips in 460 °C, 9.4 MPa harsh Venus surface conditions.

Experimental

Consistent with initial long-duration Venus lander mission concepts [2], a prototype electronics subsystem circuit board was designed to autonomously analog-to-digital convert (ADC) twelve separate sensor voltage input signals into a repeated sequence of serial digital data using minimal power consumption. The functional block diagram of the circuit, as realized within the confines of IC Gen. 11 chip complexity (~ 1000 transistors/chip [3]), is illustrated in Fig. 1. Application-specific ICs (ASICs) custom-designed into the IC Gen. 11 mask set for realizing the prototype circuit include a 12-bit shift register, 8- and 10-bit counters, 8-bit digital to analog converter (DAC), op-amp based voltage comparator, and simple control logic gates. When externally supplied electrical power and clock signals are applied, the circuit automatically alternates between a collect data mode, which digitizes and stores each voltage value into a corresponding shift register, and a transmit (XMIT) data mode which repeatedly pings out a serial bitstream of stored shift register values. The value of the 10-bit counter, via jumper-adjustable logic gates, dictates the active circuit mode. In collect data

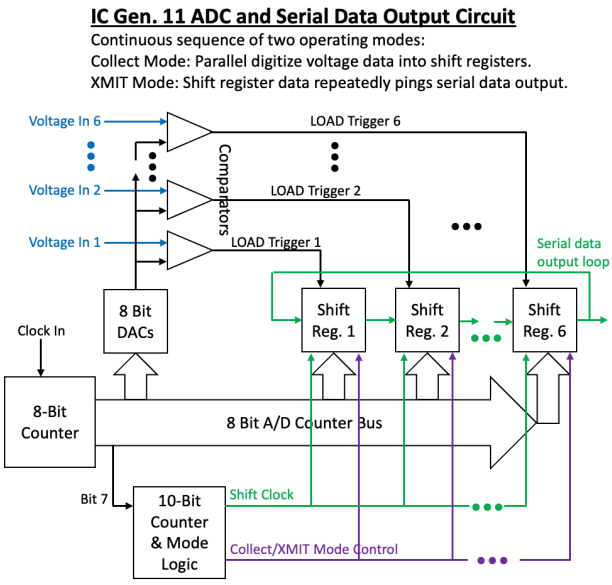

Fig. 1. Functional block diagram of the prototype IC Gen. 11 multi-chip circuit board tested. As part of a Venus lander mission this board would 8-bit digitize six analog sensor signals and ping the corresponding digital bitstream to a transmitter.

mode, the 8-bit counter drives multiple DACs (most channels shared a DAC) that ramp up voltage supplied to one side of sensor channel comparator. When a respective comparator first senses DAC voltage has exceeded the sensor input voltage, the 8-bit counter value is stored at the comparator output transition into the shift register along with 4 additional channel identification bits unique to each channel set by circuit board wiring. In transmit mode the stored shift register values are continuously pinged through a digital data loop that in a full system would feed an RF data transmitter.

The poor fabrication yield of IC Gen. 11.1 resulted in a very small inventory of probe-test functional shift register chips [4]. This in turn drove a strategic decision to jumper-reconfigure the already-fabricated circuit board into a 6-channel board needing correspondingly fewer shift register chips.

The SiC JFET-R IC fabrication process flow as well as key differences between IC Gen. 11 vs. IC Gen. 10 are described elsewhere [4-6]. The interconnect stack includes four layers of 1 µm thick SiO_2 and a thin 65 nm Si_3N_4 layer all grown by low pressure chemical vapor deposition at 720 °C. It is important to note that interconnect and bond pad metal layers are blanket deposited via ultrahigh vacuum sputtering and then dry-etched into desired pattern using photoresist etch masks.

ICs were electrically (25 °C on-wafer probe test) and microscopically (optical microscope for defects) screened and diced in preparation for placement onto the multi-chip circuit board. In contrast to conventional packaging flow, NASA-designed and commercially fabricated high temperature co-fired ceramic (HTCC) custom chip packages were then fastened onto a NASA-designed commercially fabricated two-sided multi-chip ceramic circuit board. Screened SiC chips were then attached into each package using gold-based paste annealed 2-3 hours at 600 °C [7]. Gold wire ball bonds were then made to electrically connect chips to respective ceramic packages.

The NASA Glenn Extreme Environments Rig (GEER) test chamber provided high-fidelity reproduction of the Venus surface conditions including 460 °C temperature, 9.4 MPa pressure, and the top ten chemical constituents measured at the Venus surface by short-duration Venera landers over two decades ago [8]. Custom-constructed electrical feedthroughs enabled electrical connection of the circuit board inside the Venus chamber to computer-controlled electrical measurement instruments residing outside the chamber.

In additional to optical microscopy, field emission-scanning electron microscopy (FE-SEM) imaging and focused ion beam (FIB) cross sections combined with energy-dispersive X-ray spectroscopy (EDS) maps were used to inspect critical SiC chip areas following the test. Thin layers of platinum were deposited to protect the surface on areas of interest where focused ion beam cross sections were taken.

Results

Largely due to interconnect processing difficulties reported in [4], none of the counter IC designs probe-tested as completely functional across the four IC Gen. 11 wafers fabricated. Nevertheless, two 8-bit counter ICs probe-tested sufficiently functional (in that the 6 most-significant bits operated) to support 6-bit analog-to-digital conversion (ADC) of input voltage signals. Circuit board functionality inside the Venus environmental chamber was verified before and after loading of Venus atmospheric

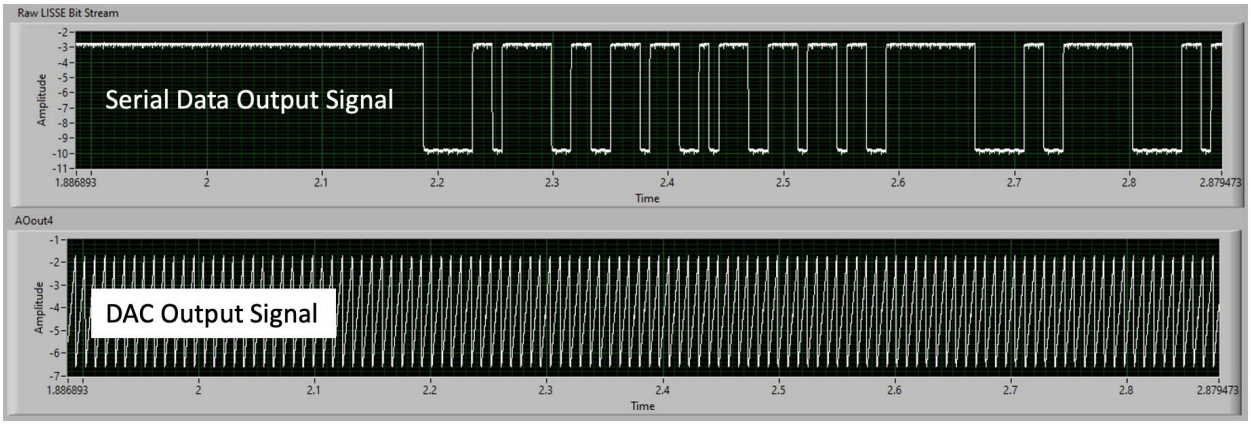

Fig. 2. Circuit output signals measured with board inside the Venus chamber at 107 °C just prior to failure. The measured diagnostic signal of the bottom trace is a repeating ramp staircase generated by counter IC driving a diagnostic output DAC. The top trace shows the start of serial data output as the operating mode transitioned from collect data mode to transmit data mode.

gas constituents near 25 °C. Fig. 2 shows functional waveforms measured (serial data output signal as well as counter-driven DAC signal ramp waves) at 107 °C during chamber heat-up. As the temperature was increased beyond 107 °C the circuit board stopped functioning. Power supply bias adjustments conducted at stabilized 460 °C Venus conditions temporarily restored a few bits of DAC diagnostic output signal but the serial data output was flatlined. By the end of the 11-day test however, the DAC and serial outputs were both flatlined and no useful serial data output was produced in 460 °C Venus surface conditions. Meanwhile, it is worth mentioning that a 16-bit IC Gen. 10 RAM IC [6] tested separately by itself successfully functioned throughout the entire 11-day test.

Fig. 3 shows the topside of the constructed 4-layer ceramic circuit board with 7 of the 10 packaged SiC chips following 11 days of exposure (without lids as pictured) to Venusian surface environmental conditions. Initial post-test optical inspections of the board revealed no physical evidence of packaging or wire bond failure. Post-test optical microscopy revealed the formation of observable dielectric layer cracks and associated/underlying $TaSi_2$ metal discoloration/oxidation on 2 of the 10 SiC chips. Fig. 4 shows a circuit-critical region, including the denoted diagnostic DAC IC, of the SiC chip highlighted in Fig. 3. A dielectric crack network and associated underlying metal oxidation/discoloration is clearly visible post-test (right image & denoted by arrows) that was not observed prior to packaging (left image). The crack network optical appearance is similar to cracking/discoloration observed in prior-studies of dielectric crack-related SiC JFET-IC failures during T ≥ 500 °C air-ambient testing [3-6, 9]. The multi-crack network extends from the very top edge of the die border to beyond the photograph bottom boundary damaging a major power bus as well as the diagnostic output DAC IC (shown) and 8-bit counter IC (not shown). While dielectric cracks were detected in additional circuit-

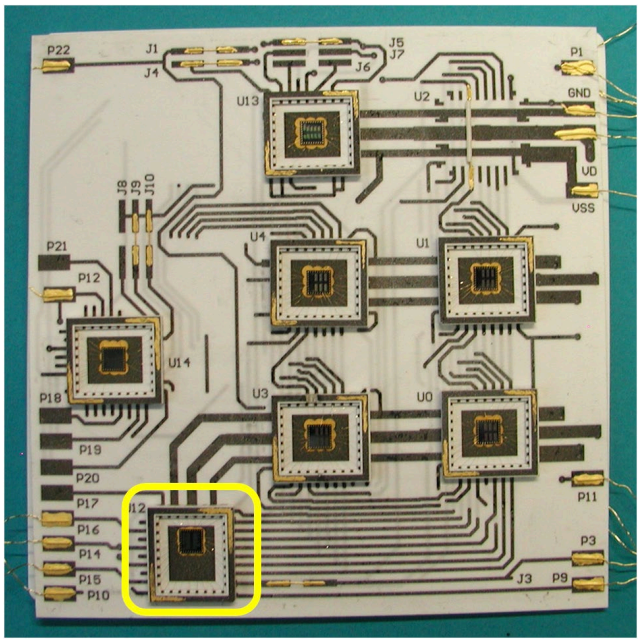

Fig. 3. 11.5 cm x 11.5 cm circuit board topside following 11 days exposure to Venusian surface conditions. The yellow box denotes the sole chip that exhibited dielectric cracking failure within active IC area.

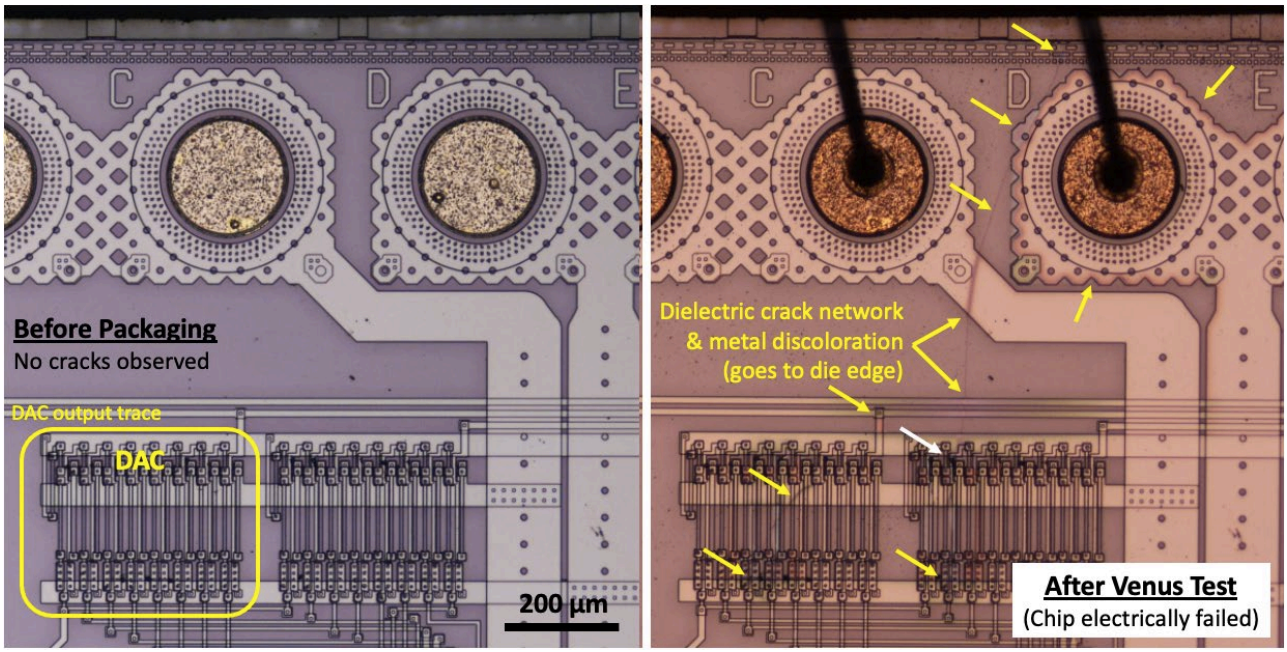

Fig. 4. Optical microscope photos of the same circuit-critical chip region before packaging (left) and after packaged Venus chamber testing (right). A laterally expansive crack network passes through electrically critical circuit regions including a major power supply bus and DAC subcircuit that electrically failed. The white arrow indicates where the Fig. 5a FE-SEM was recorded.

critical regions of the Fig. 4 chip, no cracks/discoloration over circuit-critical areas were found on any of the remaining circuit-board chips.

FE-SEM inspection of the failed chip revealed the presence of irregularly-shaped dielectric-film hillock-type defects with correspondence to the laterally expansive dielectric crack networks. Fig. 5 illustrates planar and FIB cross-sectional FE-SEM with results typical of multiple dielectric hillocks studied. The cross-sections in particular indicate tall hillock topography is present in the third oxide (i.e., SiO_2 3) layer, whereas underlying (prior-deposited) layers of oxide SiO_2 1 and SiO_2 2, as well as overlying Si_3N_4, and SiO_2 4 layers all exhibit desired uniform thickness. The EDS oxygen elemental map of the FIB cross-section of Fig. 5c particularly reveals the thin Si_3N_4 layer separating SiO_2 3 and SiO_2 4 layers enabling clear differentiation (not seen in Fig. 5b image) of the defect structure with respect to these top two oxide layers. Residual "IrIS" bond pad metal [10] was also prevalent around the bases of the micron-scale height hillocks, but is also evident to lesser degree around a few other areas of patterned oxide topography. Where dielectric cracks enabled atmospheric oxygen to reach $TaSi_2$, other FIB cross-sections revealed ~ 0.2 µm thick oxide layers formed along the buried $TaSi_2$ periphery, sometimes completely surrounding the entire periphery of a $TaSi_2$ trace cross-section.

Discussion

The optical and FIB FE-SEM post-test inspections indicate that only one chip failed on the circuit board. The crack/discoloration locations observed on this failed chip are consistent with electrical degradation and loss of DAC and counting functions. The dielectric crack failure symptoms are also similar to SiC JFET-R IC crack-related failures reported for Earth-air oven testing [3-6,9]. The hypothesized Earth-air failure sequence starts with initiation of a small crack somewhere on the chip, either due to a wafer fabrication/deposition defect or damage induced during wafer dicing or chip handling packaging.

For the chip that failed during this Venus-chamber test, most of dielectric cracks were correlated with dielectric film hillock defects that FE- SEM inspection (including Fig. 5) clearly revealed. Each hillock studied by FIB cross-sectional FE-SEM showed hillocks initiated at the bottom/start of the

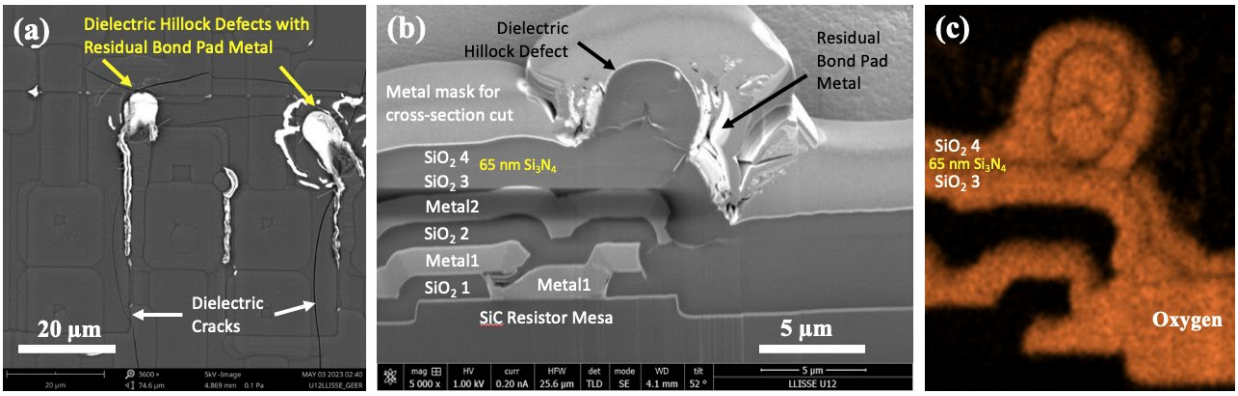

Fig. 5. FE-SEM images of dielectric hillock defects that corresponded to most of the dielectric cracks found on the failed chip. (a) Top view under imaging conditions highlighting residual metal leftover from the bond pad etch. (b) FIB cross-sectional image of hillock defect structure and prevalence of residual surrounding bond pad metal. (c) EDS oxygen elemental map of part (b) defect resolving top two oxide layers suggesting defect originated near start of SiO_2 3 layer deposition.

third SiO_2 layer that is deposited after completion of second interconnect metal patterning etch and prior to thin Si_3N_4 layer deposition. It is therefore suspected that residual photoresist (perhaps hardened during reactive ion etching) leftover after stripping the Metal 2 dry-etch mask nucleated localized dielectric hillock formation during subsequent deposition of the overlying SiO_2 3 layer. The undesired/uncontrolled topographic defect then propagates into subsequent Si_3N_4 and SiO_2 4 layers. This in turn results in adversely tall top surface topology that impedes complete removal of blanket-deposited IrIS metal during the final bond pad patterning etch. We surmise that the irregular shape and larger coefficient of thermal expansion (CTE) mismatch arising from the hillock-surrounding residual IrIS metal plays a significant role in crack initiation. Crack expansion is then driven by a hypothesized combination of CTE-mismatch induced stress and underlying $TaSi_2$ film oxidation and swelling [9]. However, application of this failure mode to the Venus chamber test is not straightforward given that (1) failure occurred so early (only 107 °C) into the Venus chamber heat-up, and (2) $TaSi_2$ did not oxidize during prior Venus-chamber testing [11]. It is therefore surmised that the majority of dielectric cracking and expansion occurred during the 600 °C die-attach anneal. Regrettably, microscopic inspection of chip surfaces following packaging prior to Venus-chamber insertion was not conducted.

Further work beyond the scope of this initial report is necessary to definitively substantiate chip failure details. Nevertheless, the preliminary findings of this report have already warranted revisions to the planned IC Gen. 12 interconnect fabrication process flow that go beyond the processing changes previously described in [12,13]. First, more-aggressive photoresist removal and wafer cleaning will be implemented following metal patterning etches to ensure that all residual photoresist is removed towards suppressing dielectric hillock defect formation. Second, a larger degree of over-etch will be applied during the final metal bond pad patterning etch towards removing more (nominally all) residual metal surrounding dielectric surface topography. More pre-step practice processing using representatively prepared dummy wafers as well as more comprehensive post-step microscopic inspections are also planned.

Conclusion

The first attempt at demonstrating a complex multi-chip lander-control circuit board in Venus surface environmental conditions using NASA Glenn IC Gen. 11.1 SiC JFET-R ICs ended prematurely in failure. Post-test studies detailed above indicate that only one of the ten chips on the board failed, due to non-ideal IC Gen. 11 interconnect processing. Remediation planned for IC Gen. 12 will hopefully enable future long-duration demonstrations of multi-chip circuits in Venus surface environmental conditions.

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