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Effects of High Gate Voltage Stress on Threshold Voltage Stability in Planar and Trench SiC Power MOSFETs

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Abstract. Gate oxide reliability is a challenge in SiC MOSFETs particularly due to the presence of high electric field in the dielectric during device operation and blocking, and SiC/SiO_2 interfaces suffer from a high density of traps and defects that can cause charge trapping and threshold voltage shift. Highly accelerated gate bias testing can be used for testing gate field effects on device reliability/stability, but care must be taken that the high acceleration biases do not invoke failure mechanisms that fall outside of normal device operation conditions. In this work, we attempt to address that aspect of high voltage gate tests in terms of threshold voltage instability and perform a comparative analysis between commercially available planar and trench SiC MOSFETs.

Introduction

There is significant interest in high-voltage Silicon Carbide (SiC) power devices due to their ability to block higher voltage with lower conduction and switching losses compared to their silicon counterparts [1]. Thanks to their wider bandgap leading to higher critical electric field, SiC devices can achieve higher breakdown voltage with much thinner drift regions relative to Si devices. Consequently, on-resistance can be significantly lower in SiC devices resulting in substantially lower power losses. However, in devices with lower voltage ratings, channel resistance is the main contributing factor towards overall on-resistance. Channel resistance is affected by the low mobility of electrons under inversion due to trapping and scattering at the SiC/SiO_2 interface. Even though significant progress has been made over the last decade to passivate interface defects e.g. with NO annealing, there still exists a high density of traps and defects that can cause charge trapping and threshold voltage shift [2-4]. Moreover, SiC MOSFETs experience high electric field in the dielectric during device operation and blocking; thus, making a reliable gate oxide particularly challenging. Highly accelerated gate bias testing can be used, but careful consideration is required to choose the right bias condition so that failure mechanisms that fall outside of normal device operation conditions do not emerge [5-9]; such as current accelerated process as schematically shown in Fig. 1. In this work, a comparative analysis between commercially available planar and trench SiC MOSFETs is performed to investigate the effect of high gate voltage stress particularly on threshold voltage stability.

Effect of High Gate Stress on V_T

Fig. 2 depicts the diagram of a gate bias and threshold voltage (V_T) measurement scheme that is performed at room temperature. A 6 s stress is applied at the gate starting with the rated gate

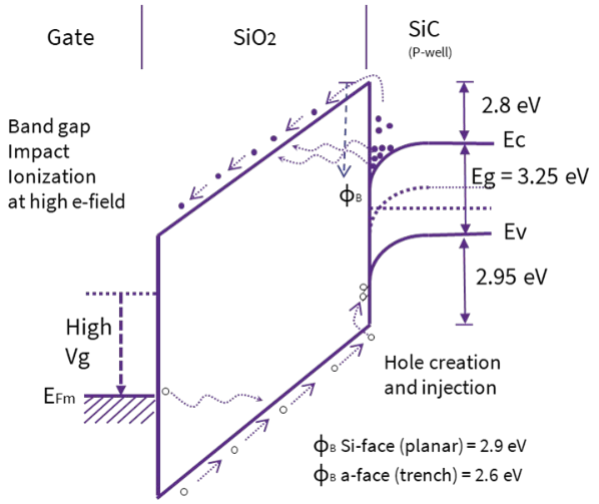

Fig. 1. At high electric field, hot electrons tunneled through oxide barrier with high energy tails exceeding 9eV may cause bandgap impact ionization near anode interface. This effect can be higher in trench devices due to lower Φ_B.

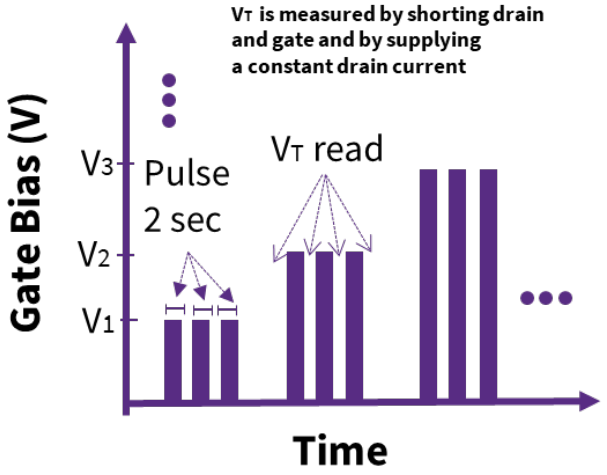

Fig. 2. Gate stresses (V_{GS}) are applied for a duration of 6 s with threshold readouts performed before the gate pulses, and at 2 s intervals. V_{GS} is then stepped to a higher value and the process is repeated.

bias (V_{GS}), while V_T is measured at time t = 0, 2, 4, and 6 s by shorting drain and gate together and by supplying a constant drain current of 1uA. This process is repeated by gradually incrementing gate bias to higher values of V_{GS}. Fig. 3 and 4 show the results of these tests for commercial 1200V planar and trench SiC MOSFETs, respectively where V_T values are plotted with respect to gate bias voltages. There exist four V_T measurements for each stress time ST = 0, 2, 4 and 6 s (from lighter circles to darker circles) at each gate bias where ST = 0 s indicates V_T measurement before any stress pulse is applied. After the application of the first pulse (ST = 2 s) at V_{GS} = 15V, the threshold voltage increases due to PBTI effects. Additional gate stress pulses (ST = 4 and 6 s) at 15V barely increase V_T further as indicated by the overlapping circles in figures 3 and 4. Gate stress is then increased from the rated value of 15V to 38V with a step of 5V (for lower stress region) and 2V (for higher stress region). V_T starts to increase gradually due to PBTI effects at lower stress, but after a critical value of V_{GS}, the threshold voltage starts to decrease. V_T increment is found to be higher in trench devices than in planar devices and the critical value happens to be 30V for planar device and 32V for trench device respectively. It should be noted that from our analysis of the products tested, the trench MOSFET has a thicker gate oxide, which would affect the onset of this V_T decrease behavior (oxide electric field should be more important than gate potential). At the higher voltage region above this critical value, consecutive pulses of higher V_{GS} continue to decrease threshold even lower. At the significantly high gate stress (V_{GS} = 38V), threshold decreases to zero in both planar and trench devices. The measurement approach used here for V_T evaluation does not allow $V_T < 0$V to be measured; however, from I_D-V_G sweeps the V_T is seen to fall well below 0V as the V_{GS} pulse height is increased.

While the increase in threshold voltage happens due to PBTI effect below the critical voltage or electric field, the physics of threshold degradation above critical value is still under debate. There exist several theories that attempt to explain gate oxide breakdown under high field in Si/SiO_2 and one such theory can be adopted to explain threshold instability in SiC/SiO_2 as well. The decrease in threshold voltage at high field can be attributed to bandgap impact ionization occurring near the SiO_2/gate interface. At high electric field (>9MV/cm) when a significant portion of electrons that

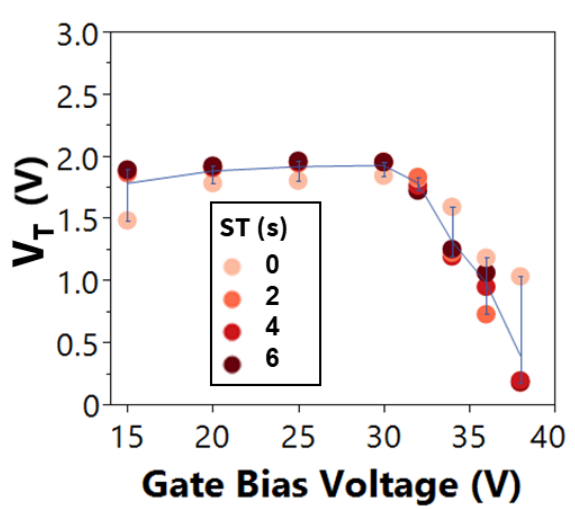

Fig. 3. (Planar) Variation of threshold voltages (V_T) with respect to the gate bias pulses. V_T is measured at t = 0, 2, 4 and 6 s for each gate bias condition. [ST = Stress Time]

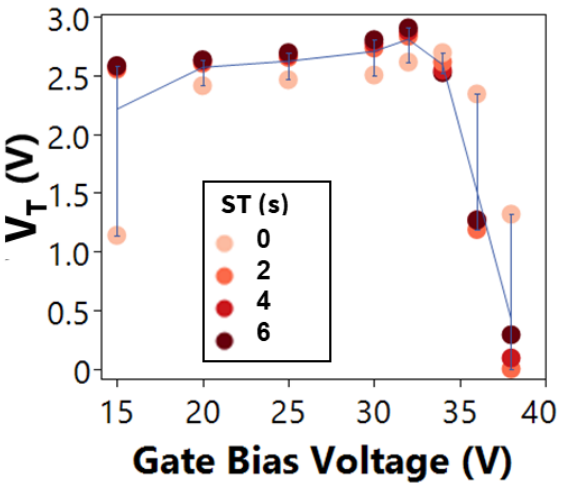

Fig. 4. (Trench) Variation of threshold voltages (V_T) with respect to the gate bias pulses of 6 s for a trench MOSFET. V_T is measured at t = 0, 2, 4 and 6 s for each gate bias condition. [ST = Stress Time]

tunnel through the dielectric via Fowler-Nordheim (FN) mechanism gain high kinetic energy (exceeding 9eV) from the electric field while traversing through the thick oxide and create electron-hole pairs due to impact ionization near the SiO_2/Gate interface [10-14]. Hot holes travel back through the oxide towards SiO_2/SiC interface and may get trapped during the process either in the oxide or deep energy interface states resulting in fixed oxide charges (see Fig. 1). In another scenario, when electron's energy does not exceed 9eV but high enough that upon reaching the anode, hole is generated from impact ionization at the anode. These holes tunnel into the oxide and eventually trap somewhere in the oxide while traversing towards SiO_2/SiC interface. Regardless of the underlining mechanism of hole generation, holes fill in the existing traps in the oxide and the net result is a buildup of positive charge that acts like fixed charge. There can be some hole annihilation due to electron trapping, but accumulation of holes outnumbers electron trapping, resulting in a decrease in threshold voltage. In addition, hole trapping in near-interface states near the valence band may be occurring simultaneously.

Gate Bias Hysteresis of Drain Leakage

In the previous section, V_T is measured by gradually increasing gate bias and it is observed that the threshold voltage degrades significantly under high bias above a critical value. In this section, we attempt to estimate the level of degradation by measuring a low gate bias hysteresis of drain leakage. Figures 5 and 6 show drain current hysteresis for pre- and post-stress (stress applied in Fig. 2) while sweeping V_{GS} from +5V to -5V (down arrow) and vice versa (up arrow) with a step of 0.1V. Drain voltage, V_{DS} is kept at a low value of 0.1V. Both planar and trench devices show negative shifts in their V_T indicating the presence of fixed oxide charges. While the planar device shows less hysteresis overall, a larger hysteresis is observed post-stress compared to pre-stress; whereas the trench device has a larger hysteresis, but it narrows post-stress. For example, in case of the planar device, $\triangle V_T$ (difference between down sweep and up sweep) at 1 nA drain current is increased from 0.5V to 1.0V (Fig. 5) where as $\triangle V_T$ is decreased in trench device from 2.65V to 1.9V (Fig. 6). However, the trench device hysteresis is larger than that of the planar device for both cases. It is believed that some existing hole traps get filled in the trench device during stress, resulting in a decreased post-stress hysteresis and decreased $\triangle V_T$.

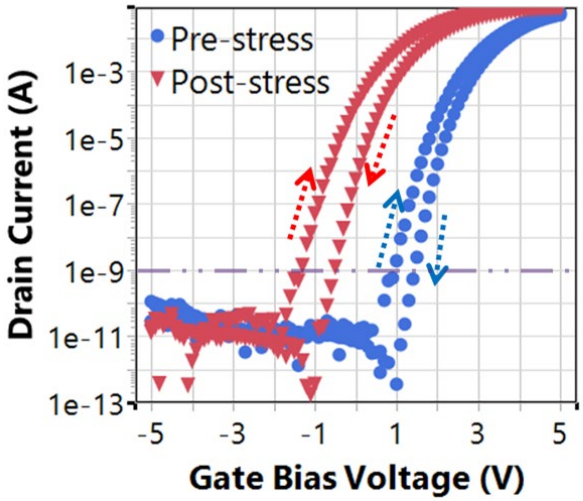

Fig. 5. Gate bias hysteresis of drain leakage for pre- and post- high voltage gate bias in a planar MOSFET structure.

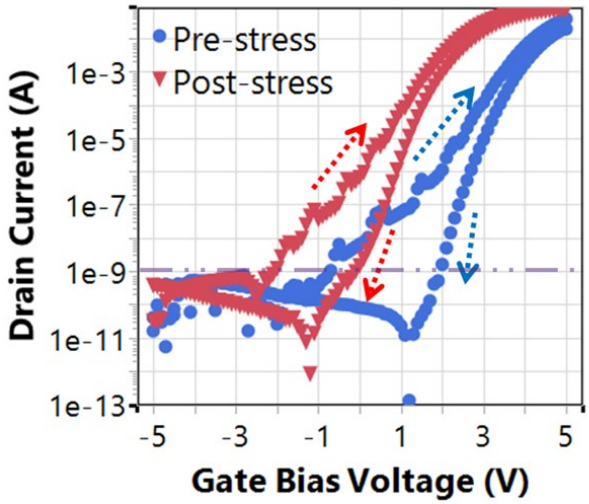

Fig. 6. Gate bias hysteresis of drain leakage for pre- and post-high voltage gate bias in a trench MOSFET structure

Quasi-static C-V measurement

Figures 7 and 8 show quasi-static C-V characteristics for planar and trench devices pre- and post- V_{GS} stress cycle. Gate bias voltage V_{GS} has been swept from +6V (strong inversion) to -10V (accumulation) while capacitance values have been measured between gate and source-drain grounded together. At strong inversion with the channel fully turned on, quasi-static capacitance values are measured as 5.6 nF and 9 nF for planar and trench devices respectively and these values can be considered as gate oxide capacitance assuming there are no oxide charges. Lower capacitance values in the planar device compared to the trench can be attributed mostly to the estimated gate oxide thickness/active area difference. Figures 7a and 8a clearly show a net shift in C-V curves indicating the creation of fixed charges. The shifts in voltage have been calculated as 2.2V and 1.9V in planar and trench devices respectively by overlapping the C-V curves for pre- and post-stress conditions (see figures 7b and 8b). If we consider that there is negligible effect from interface states, one can approximate the additional fixed charge ΔQ_f from the shift in C-V curve by using eq. 1 and 2 [15]

$$\Delta Q_f = Q_{f2} - Q_{f1} = \Delta V_{FB} C_{ox} \quad (1)$$

$$\Delta N_f = \Delta V_{FB} C_{ox}/Aq, \quad (2)$$

where Q_{f1} and Q_{f2} are fixed charges for pre- and post-stress conditions, V_{FB1} and V_{FB2} are pre- and post-flat-band voltages, C_{ox} is the oxide capacitance, A is area and q is electron charge. If we approximate ΔV_{FB} as the net shift in C-V curve, additional fixed charge developed in planar and trench devices can be calculated using eq. 2. Thus, the additional fixed charge due to gate stress are found to be $\Delta N_{f(P)} = 7.7 \times 10^{11}$cm^{-2} in planar device and $\Delta N_{f(T)} = 5.3 \times 10^{11}$cm^{-2} in trench device. Note that these values are obtained with area and t_{ox} approximated. Similar values of added charges indicate similar mechanisms are prevalent in both planar and trench devices. In addition to fixed charges, other trap related effects are also occurring in the trench device (Fig. 8b.), as indicated by the change in shape of the C-V characteristics in the depletion portion of the curve. This change in shape infer some sort of degradation in the oxide for the trench device due to the high gate voltage stress. However, further investigation is required to understand these effects that is outside the scope of this comparative study.

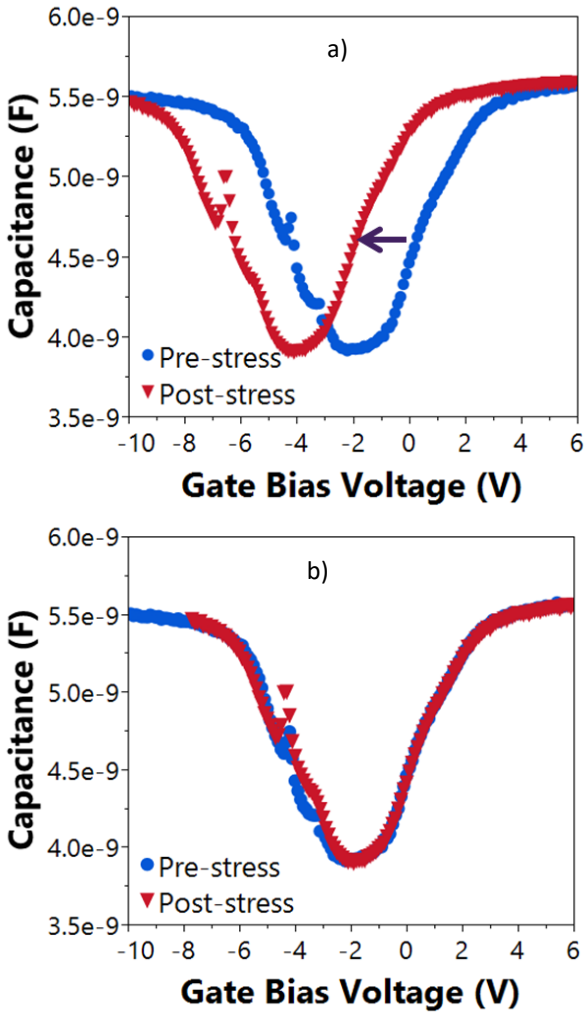

Fig. 7. a) C-V (quasi-static) measurement of a planar MOSFET for pre- and post- high voltage gate bias. b) C-V (quasi-static) after shifting the post-stress curve horizontally to the right by 2.2V.

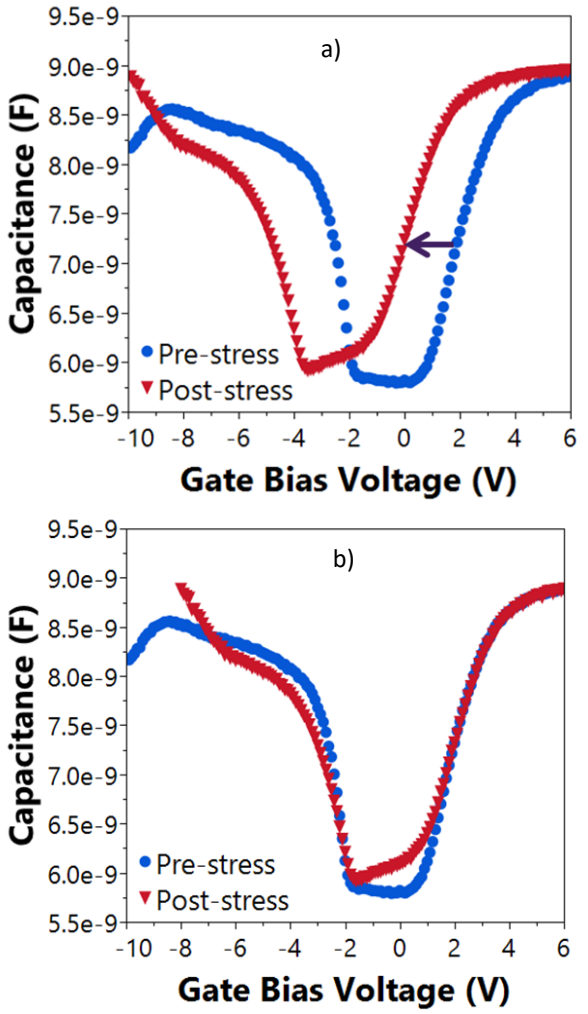

Fig. 8. a) C-V (quasi-static) measurement of a trench MOSFET for pre- and post- high voltage gate bias. b) C-V (quasi-static) after shifting the post-stress curve horizontally to the right by 1.9V [Other trap related effects into play].

Effect of Stress Duration and Multiple Stress Cycle

Figures 9 and 10 show the variation in V_T during multiple stress cycles ranging from 0V to 40V (planar) and 42V (trench). Every point in a particular stress cycle (SC) curve is the result of V_T measurement with a duration of 20 us after a single gate stress of 10 ms is applied. During the first stress cycle as indicated by TD = 0 in figures 9 and 10, similar PBTI related effects are observed as before and V_T trends towards higher values below the critical voltage. Albeit the gate stress pulse width is reduced from 6 s to 10 ms, V_T degrades in similar fashion above the critical voltage of the gate stress as observed in figures 3 and 4. However, critical voltage exhibits a higher value (36V for both planar and trench) as compared to a lower value (30V for planar and 32V for trench) for a 6 s stress pulse. This indicates that the degradation mechanism may also be influenced by the accumulation of total fixed charge along with the high electric field. After the first stress cycle, devices are immediately put under another SC (time delay, TD of 1-2 s) which shows some recovery in V_T after high voltage stress (first point in the SC curve at TD = 1-2 s) but

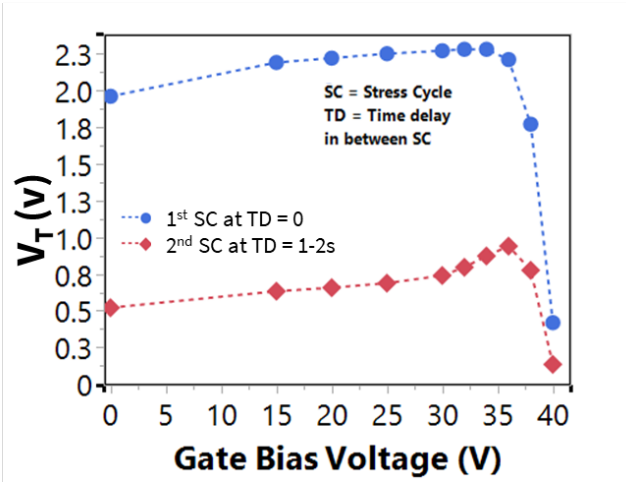

Fig. 9. (Planar) Gate bias is applied at each voltage for 10 ms and a subsequent read out of V_T is performed for 20 us in a stress cycle (SC) ranging from 0V to 40V. SC is repeated at time delay (TD)< 2s. Both SC curves follow similar pattern pointing to a single critical value at which V_T starts to decline.

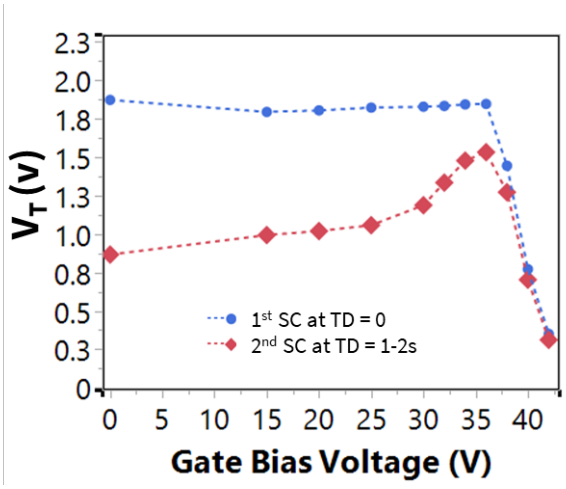

Fig. 10. (Trench) Gate bias is applied at each voltage for 10 ms and a subsequent read-out V_T is performed for 20 us in a stress cycle (SC) ranging from 0V to 42V. SC is repeated at time delay (TD)< 2s. Both SC curves follow similar pattern pointing to a single critical value at which V_T starts to decline.

follow similar trend of the first SC. In consecutive stress cycles both planar and trench devices start to show decline in V_T at the same voltage showing no shift in critical electric field even after several stress cycles.

Conclusion

To investigate the high voltage gate stress aspect of SiC MOSFETs, we study threshold voltage (V_T) instability since the latter has been a major concern in SiC power devices. Our study shows a significant degradation in V_T under high electric field due to the creation of fixed charge at the SiO_2/SiC interface in both planar and trench MOSFETs. Drain current hysteresis and quasi-static C-V have been used to approximately estimate fixed charges from the shift in hysteresis and C-V in pre- and post- stress measurements. We then modulate pulse duration and observe that threshold degradation may have dependency on total fixed charge accumulated in addition to the high electric field that initiates the creation of holes at the first place. In conclusion, we present the effect of high gate voltage stress on threshold voltage stability and suggest that gate bias stresses that cause excessive V_T shift should be avoided for highly accelerated gate stress tests.

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