Solid State Phenomena
ISSN: 1662-9779, Vol. 358, pp 79-87
doi:10.4028/p-9MknRR

Submitted: 2023-08-02
Revised: 2024-04-12
Accepted: 2024-04-15
Online: 2024-08-21

Design of $Al_2O_3/LaAlO_3/SiO_2$ Gate Stack on Various Channel Planes for High-Performance 4H-SiC Trench Power MOSFETs

Linhua Huang[1,a*], Yong Liu[1,b], Xin Peng[1,c], Takashi Tsuji[2,d], Yuichi Onozawa[2,e], Naoto Fujishima[2,f], and Johnny Kin On Sin[1,g]

[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong, China

[2]Fuji Electric Co., Ltd, 4-18-1 Tsukama, Matsumoto, Nagano 390-0821, Japan

[a]lhunagat@connect.ust.hk, [b]yliueg@connect.ust.hk, [c]xpengaj@connect.ust.hk, [d]tsuji-takashi@fujielectric.com, [e]onozawa-yuichi@fujielectric.com, [f]fujishima-naoto@fujielectric.com, [g]eesin@ust.hk

Keywords: SiC trench gate power MOSFETs, high-k gate stack, interface state density, channel planes, channel mobility limiting mechanisms.

Abstract. An $Al_2O_3/LaAlO_3/SiO_2$ gate stack is designed and implemented on various trench-gate channel planes for high-performance trench power MOSFETs. The designed high-k gate stack achieves a significant enhancement in the gate blocking capability (~1.73X) and maintains a low interface state density (D_{it}), in comparison to the SiO_2 gate. Moreover, owing to the implementation of the high-k gate stack, the high-k trench gate MOSFETs conduct a drain current of approximately 1.3 times larger than that of the SiO_2 trench gate MOSFETs on all 24 channel planes at the same overdrive voltage (V_{gs}-V_{th}) of 10 V. An analysis of the mobility limiting mechanisms on different channel planes reveals that the highest channel mobility on the $(11\bar{2}0)$ channel plane is primarily due to its largest Coulomb scattering mobility and surface roughness scattering mobility.

Introduction

The worldwide call for carbon neutrality has spurred a surge growth in demand for high-performance power semiconductor devices. Notably, SiC power MOSFETs have gained significant interest due to their impressive inherent material properties, including wide energy bandgap, high critical electric field, and large thermal conductivity. Despite their advantages, one vital problem preventing SiC power MOSFETs from achieving their theoretical expectations is the large channel resistance caused by the low channel mobility. One approach to lower the channel resistance is through the implementation of a trench-gate channel. However, the gate oxide at the trench bottom would experience a high electric field during reverse blocking, which causes a serious reliability concern. Fortunately, this issue can be overcome by the utilization of high-k gate dielectric [1]. High-k gate dielectric not only mitigates the electric field in the gate dielectric but also further reduces the channel resistance. A desirable high-k gate dielectric should not only have a high dielectric constant but also possess wide conduction and valence band offsets, as well as good thermal stability. However, the wide energy bandgap and high dielectric constant of a high-k material cannot be obtained simultaneously [2]. Therefore, a thin layer of SiO_2, typically several nanometers thick, is usually formed before the high-k dielectric deposition to improve the suppression of gate leakage current. Al-based high-k dielectric is a possible candidate because of its high thermal stability and wide energy band gap [1]. Al_2O_3 has been intensively investigated due to its relatively high energy band offsets and high crystallization temperature; however, it has only a moderate dielectric constant [3]. La_2O_3 is known to be superior in terms of both the thermal dynamic stability and dielectric constant, but its valence band offset is not sufficiently high (0.9 eV) [4]. Intermixing of Al_2O_3 with La_2O_3 to form $LaAlO_3$ enhances the dielectric constant of Al_2O_3, which also maintains a relatively wide band gap and good thermal stability [4].

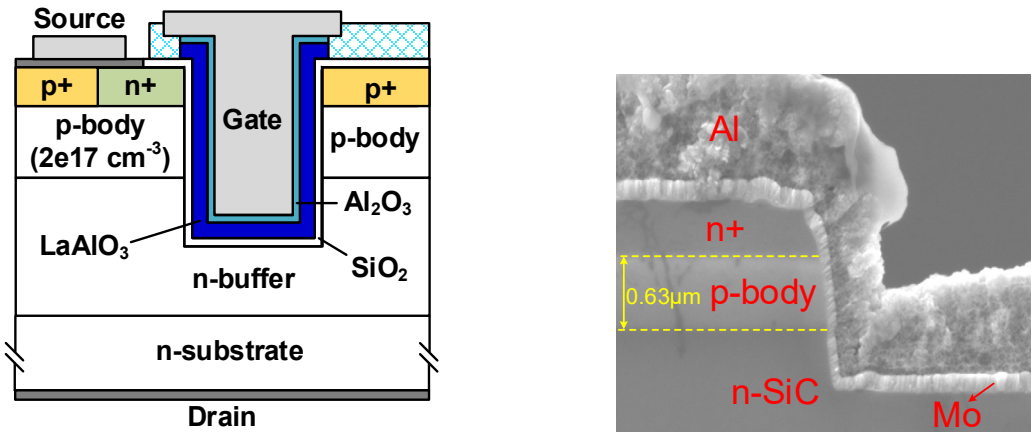
Based on above facts, an $Al_2O_3/LaAlO_3/SiO_2$ gate stack on planar SiC MOSFETs has been demonstrated to achieve a 40% reduction in channel resistance, negligible transfer hysteresis, better

threshold voltage stability, and longer short-circuit withstand time, compared to the conventional SiO_2 gate devices [5, 6]. In this paper, design of $Al_2O_3/LaAlO_3/SiO_2$ gate stack on various channel planes for high-performance 4H-SiC trench power MOSFETs will be investigated to further explore the benefits of the high-k gate stack.

Experimental Details

To design the $Al_2O_3/LaAlO_3/SiO_2$ gate stack for trench gates, two sets of MOS capacitors were fabricated on 4° off-axis n-type 4H-SiC (0001) Si-face wafers. The wafers had a 10-µm-thick epitaxial layer with a doping concentration of 1×10^{16} cm^{-3}. The wafers were diced into small samples and then cleaned by standard organic, Piranha, RCA cleaning and sacrificial oxidation process (1150°C dry oxidation and HF dip). The first set of four MOS capacitors had a single layer of SiO_2 and received different nitridation treatments. A 16-nm-thick SiO_2 layer was deposited and annealed at 1250°C in either 10% NO or 10% N_2O ambient. The annealing durations are 30 mins, 70 mins, and 100 mins. The second set of three MOS capacitors had the same nitridation treatment but different gate dielectrics: namely SiO_2, $LaAlO_3/SiO_2$, and $Al_2O_3/LaAlO_3/SiO_2$ MOS capacitors. The SiO_2 MOS capacitor is a control sample, which is the sample built above with the NO annealing for 70 mins. The $LaAlO_3/SiO_2$ MOS capacitor has a $LaAlO_3$ layer (40 nm) deposited by atomic layer deposition on the 70-min NO-annealed SiO_2 surface. The $Al_2O_3/LaAlO_3/SiO_2$ MOS capacitor was fabricated with an additional step of O_2 annealing and a subsequent deposition of an Al_2O_3 cover layer (10 nm) on top, in contrast to the $LaAlO_3/SiO_2$ MOS capacitor.

Alongside the fabrication of the MOS capacitors described above, SiC trench gate MOSFETs were also fabricated on 4° off-axis Si-face 4H-SiC wafers with an n-buffer layer and a p-type epilayer. The doping concentration and thickness of the n-buffer layer are 5×10^{18} cm^{-3} and 1.5 µm, respectively. The doping concentration and thickness of the p-type epilayer are 2×10^{17} cm^{-3} and 1 µm, respectively. Figures 1 (a) and (b) illustrate the structural diagram of the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET and SEM image of the trench gate, respectively. After n+ and p+ regions were implanted and activated, the wafers were etched to form gate trenches, followed by sacrificial oxide growth and removal to reduce the lattice damages caused during the trench etching. Subsequently, the gate stack and ohmic contact were formed using the contact-first process, which was previously developed for fabricating $Al_2O_3/LaAlO_3/SiO_2$ gate lateral MOSFETs [6]. It is worth noting that the ohmic contact is formed prior to the high-k gate stack formation. Particularly, the process utilized for forming the high-k gate stack of the trench gate MOSFETs is the same as the process used for building the $Al_2O_3/LaAlO_3/SiO_2$ MOS capacitor described above. SiO_2 trench gate MOSFETs were also



(a) (b)

Fig. 1. (a) Structural diagram of $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET and (b) SEM image of the trench gate.

fabricated as the control device, which had a capacitance equivalent thickness (CET) of 43 nm and received the same nitridation treatment as the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFETs. The electrical properties of the MOSFETs were measured with Agilent 4156C precision semiconductor parameter analyzer. Effective electric field in the gate dielectric ($E_{eff,ox}$) is calculated by (V_g-V_{fb})/CET, where V_{fb} is the flat band voltage. The gate voltage sweep rate in this study is 1 V/s. The channel length and width are 0.63 μm and 100 μm, respectively.

Results and Discussion

Design of $Al_2O_3/LaAlO_3/SiO_2$ gate stack. The first set of the four MOS capacitors described above was used to optimize the deposited-SiO_2/SiC interface. Figure 2 shows the interface state density (D_{it}) for the deposited-SiO_2/SiC interfaces. The MOS capacitor annealed in 10% NO for 70 mins shows the lowest D_{it} and longer duration has no further improvement on D_{it}. It is because that the 100-min 10% NO annealing provides excess nitrogen atoms diffused into the bulk SiO_2 layer near the interface, which degrades the interface quality [7]. Besides, the N_2O annealing has an inferior passivation effect to that of the NO annealing under the same conditions on the deposited-SiO_2/SiC interface. The cause for the inferior passivation effect is that the N_2O annealing grows additional SiO_2 [8]. The additional SiO_2 growth at the interface generates carbon-related defects, compromising the passivation effect of the N_2O annealing.

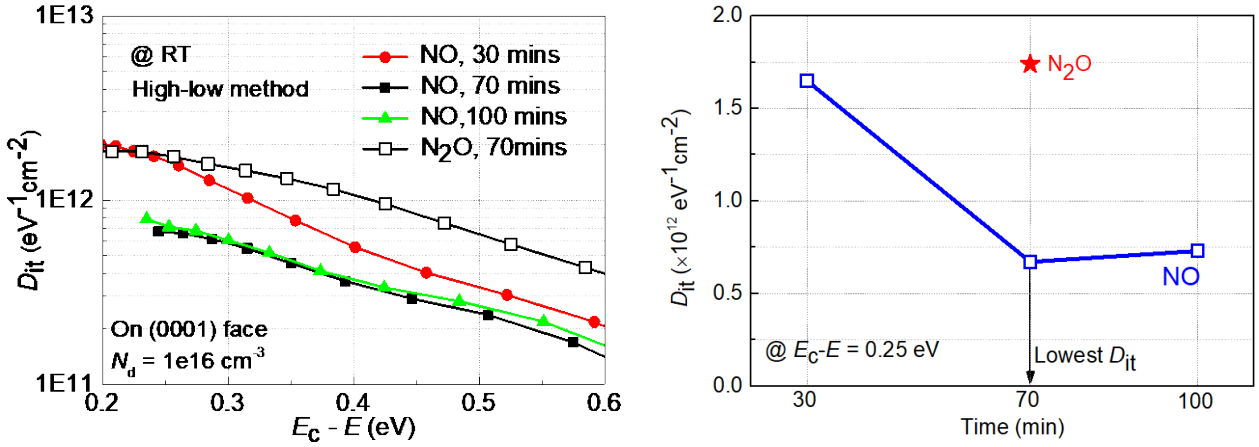


Fig. 2. (a) Energy distribution of D_{it} and (b) annealing duration vs D_{it}, at energy location of 0.25 eV below the conduction band edge for the four SiO_2 MOS capacitors.

The second set of the three MOS capacitors described above was used to investigate the impact of the O_2 annealing on the deposited-SiO_2/SiC interface. The O_2 annealing was employed to improve the high-k dielectric quality [5, 6]. Figure 3 (a) shows the *C-V* curves for the three MOS capacitors. The extracted dielectric constants from the *C-V* curves are 3.5, 8.2, and 21 for the SiO_2, Al_2O_3, and $LaAlO_3$, respectively. Figure 3 (b) shows a significant enhancement in the gate blocking capability (~1.73X) achieved by employing the $Al_2O_3/LaAlO_3/SiO_2$ gate stack. Figure 3 (c) shows a slightly increase in D_{it} for the $Al_2O_3/LaAlO_3/SiO_2$ MOS capacitor, which is possibly due to the additional O_2 annealing. Additional interface states would be generated during the O_2 annealing. This developed $Al_2O_3/LaAlO_3/SiO_2$ gate stack was then implemented in various trench gate MOSFETs with different channel planes.

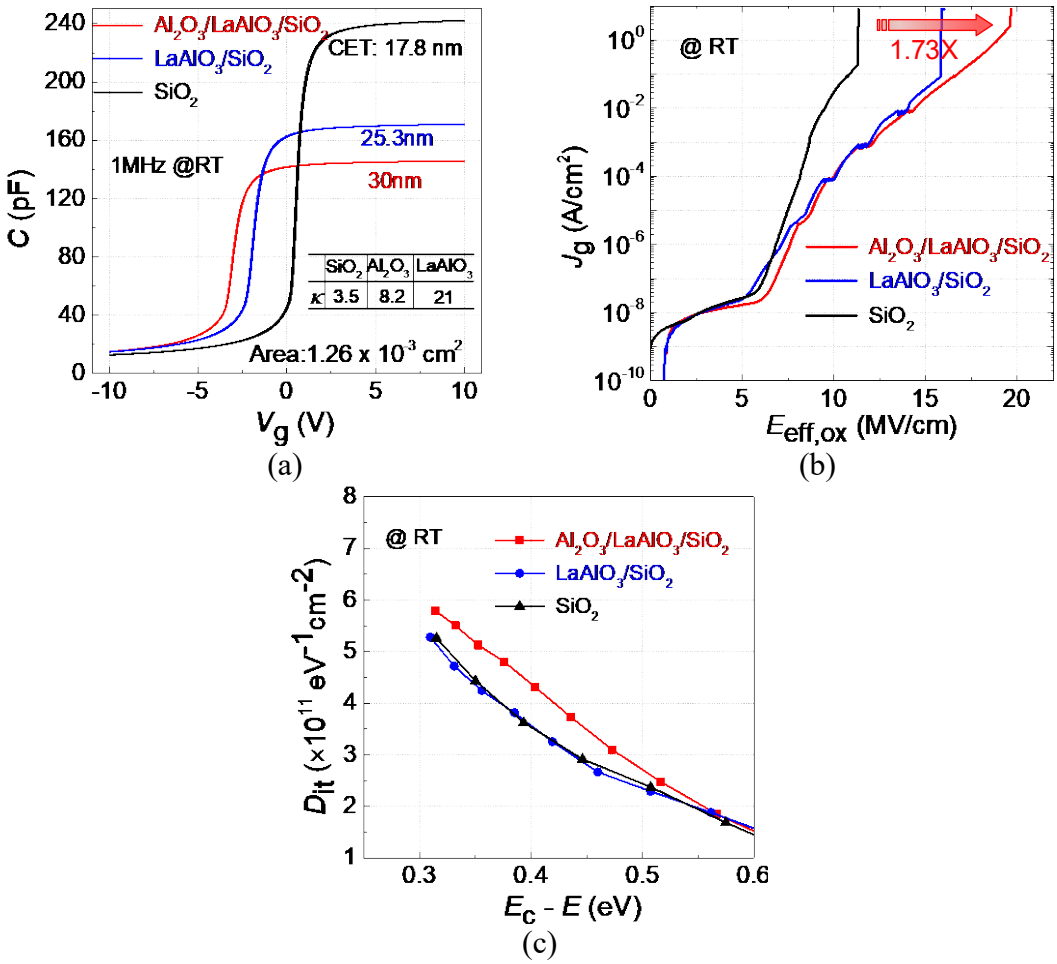


Fig. 3. (a) Bidirectional *C-V* curves measured at 1 MHz, (b) gate leakage current density (J_g) plotted against $E_{eff,ox}$, and (c) D_{it} distribution at room temperature for the three MOS capacitors.

Electrical characteristics of the high-k trench gate MOSFETs. To investigate the electrical characteristics of various channel planes, the trench-gate channel planes were formed on 24 crystal orientations with each rotation being 15° apart, as shown in Fig. 4. Each trench gate MOSFET uses a single channel plane to investigate each crystal face individually.

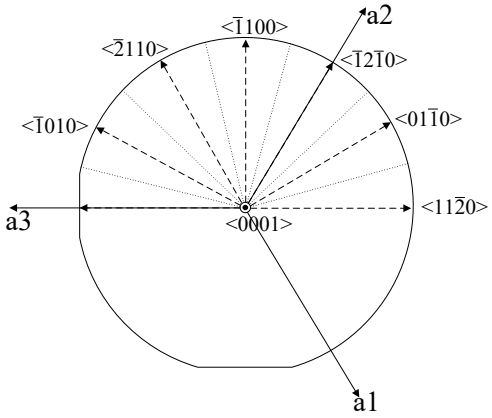


Fig. 4. Investigated crystal orientations with each rotation being 15° apart.

Figure 5 shows the transfer curves of the $Al_2O_3/LaAlO_3/SiO_2$ and SiO_2 trench gate MOSFETs on the four channel planes: $(11\bar{2}0)$, $(\bar{1}\bar{1}20)$, $(1\bar{1}00)$, and $(\bar{1}100)$. Under the same overdrive voltage (V_{gs}-V_{th}) of 10 V, the drain current of the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET is approximately 1.3 times higher than that of the SiO_2 device on the four channel planes. Among the four channel planes in either the $Al_2O_3/LaAlO_3/SiO_2$ or SiO_2 trench gate MOSFET, the largest drain current conducts on

the $(11\bar{2}0)$ channel plane, and the $(1\bar{1}00)$ and $(\bar{1}100)$ channel planes conduct almost the same drain current at the same overdrive voltage. Figure 6 (a) shows that the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET has enhanced drain current (~1.3X) on all 24 channel planes at the same overdrive voltage of 10 V. The channel planes near the $(11\bar{2}0)$ channel plane deliver a larger drain current compared to those near the $(\bar{1}\bar{1}20)$ channel plane. Figure 6 (b) shows the change in V_{thmax}/V_{th}, where V_{thmax} is the largest value of V_{th} among the 24 channel planes. The change in I_d (Fig. 6 (a)) is consistent with the change in V_{thmax}/V_{th} (Fig. 6 (b)). It is because that the larger interface state density on a channel plane would trap more electrons. The larger number of trapped electrons would cause a higher V_{th}, leading to a smaller V_{thmax}/V_{th}.

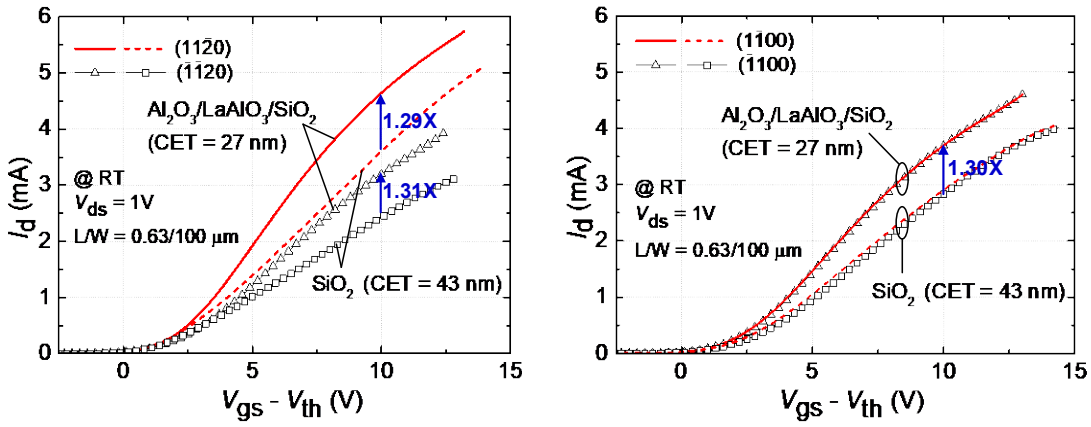


Fig. 5. Transfer characteristic I_d vs V_{gs}-V_{th} at room temperature for four channel planes: (a) $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$, and (b) $(1\bar{1}00)$ and $(\bar{1}100)$.

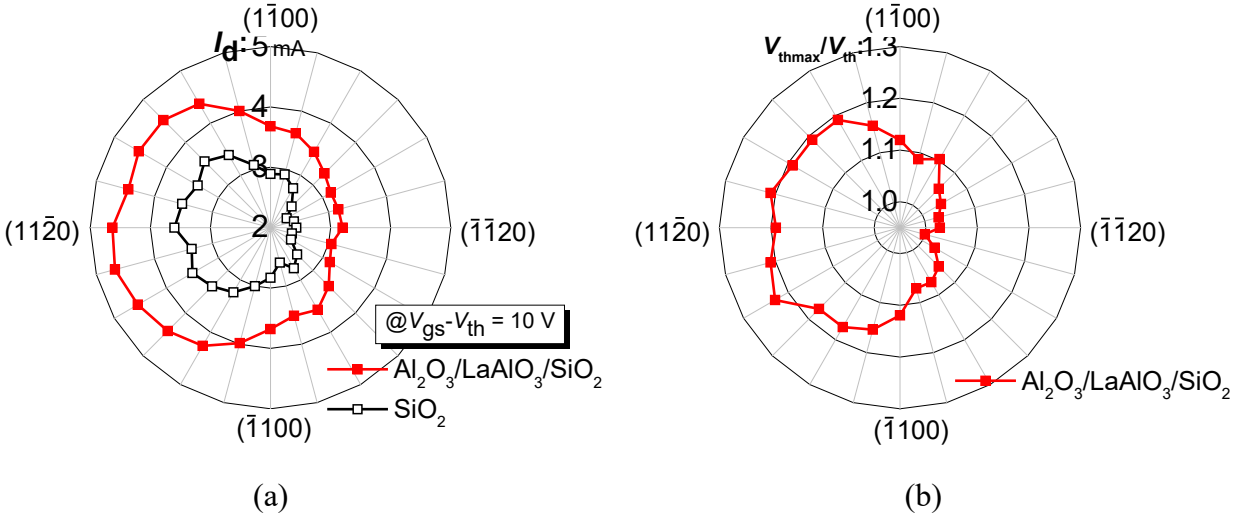


Fig. 6. (a) I_d on various channel planes at V_{gs}-V_{th} = 10V and room temperature for SiO_2 and $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFETs, and (b) V_{thmax}/V_{th} on various channel planes at room temperature for $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFETs.

The drain current is related to both the gate capacitance and the channel mobility. To distinguish which one contributes to the higher drain current, the channel mobility of the trench gate MOSFETs is investigated. Figure 7 shows the field-effect (FE) channel mobility of the $Al_2O_3/LaAlO_3/SiO_2$ and SiO_2 trench gate MOSFETs on the four channel planes: $(11\bar{2}0)$, $(\bar{1}\bar{1}20)$, $(1\bar{1}00)$, and $(\bar{1}100)$. On the same channel plane, the $Al_2O_3/LaAlO_3/SiO_2$ device shows a slightly smaller peak channel mobility than that of the SiO_2 device. This is consistent with the D_{it} values for the two kinds of gates, as shown in Fig. 3 (c). The cause is most likely related to the O_2 annealing for the $Al_2O_3/LaAlO_3/SiO_2$ device, which can deteriorate the passivated deposited-SiO_2/SiC interface and lead to a reduction in the channel mobility. Therefore, the higher drain current of the $Al_2O_3/LaAlO_3/SiO_2$ device is mainly

contributed by the higher gate capacitance. Nevertheless, the $(1\bar{1}00)$ channel plane of the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET delivers an enhanced peak channel mobility (~1.25X) than the reported value (~20 cm^2/Vs) [9] on the same channel plane, possibly due to the delicate NO annealing which helps the interface passivation. Furthermore, when comparing the channel mobility among the four channel planes in either $Al_2O_3/LaAlO_3/SiO_2$ or SiO_2 trench gate MOSFET, the largest channel mobility exhibits on the $(11\bar{2}0)$ channel plane, and the $(1\bar{1}00)$ and $(\bar{1}100)$ channel planes show almost the same channel mobility at the same overdrive voltage.

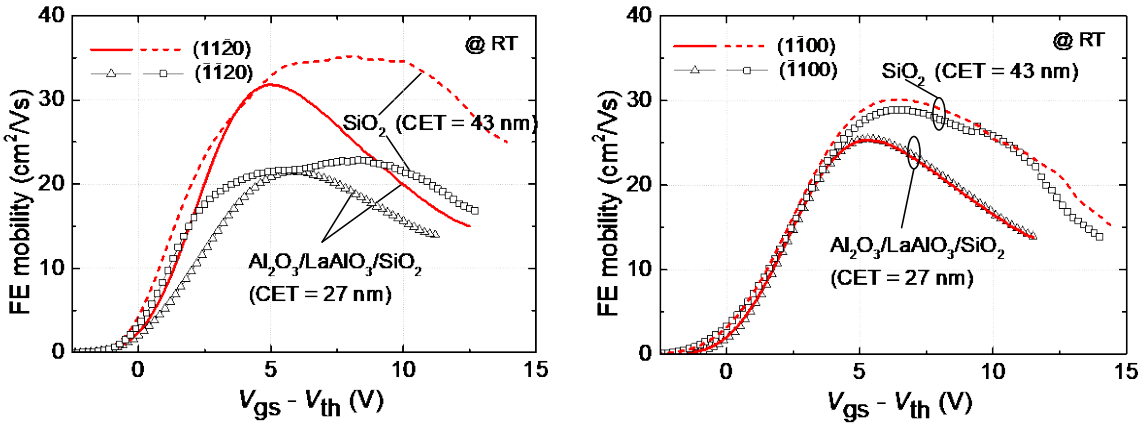


Fig. 7. FE mobility vs V_{gs}-V_{th} at room temperature for four channel planes: (a) $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$, and (b) $(1\bar{1}00)$ and $(\bar{1}100)$.

Channel mobility limiting mechanisms. To understand the channel mobility limiting mechanisms, modeling of these mechanisms is carried out. According to the reported results, the channel mobility is limited by Coulomb scattering, optical phonon scattering, and surface roughness scattering [9]. Therefore, Coulomb scattering mobility (μ_c), optical phonon scattering mobility (μ_{op}), and surface roughness scattering mobility (μ_{sr}), are taken into account to calculate the total mobility (μ_{total}) as shown below [9]:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_c} + \frac{1}{\mu_{op}} + \frac{1}{\mu_{sr}} \tag{1}$$

$$\mu_c = \frac{\Gamma_C T}{N_T}\left(1+\frac{N_S}{N_{scr}}\right)^{\zeta_C} \tag{2}$$

$$\mu_{sr} = \frac{\delta}{E_{eff,SiC}^2} \tag{3}$$

$$\mu_{op} = C_{op}\cdot E_{eff,SiC}^{n}\cdot\left[\exp\left(\frac{\hbar\omega_{op}}{kT}\right) - 1\right] \tag{4}$$

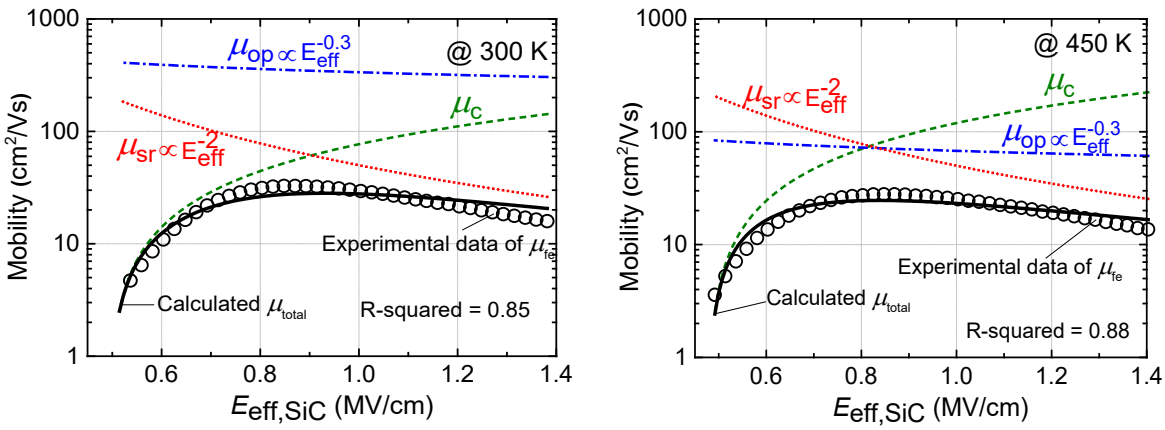
$$E_{eff,SiC} = \frac{q}{\varepsilon_{SiC}}\cdot\left(N_{dpl} + \eta N_S\right) \tag{5}$$

where N_T is the total number of trapped charges, including fixed and interface trapped charges, N_S is the surface carrier concentration, $E_{eff,SiC}$ is the effective field in the SiC, T is the absolute temperature, $\hbar\omega_{op}$ is the optical phonon energy, k is the Boltzmann constant, ε_{SiC} is the permittivity of SiC, N_{dpl} is the surface concentration of the depletion charges, η is taken to be 1/2 for electron mobility based on the Si mobility model, and Γ_C, N_{scr}, ζ_C, δ, n, and C_{OP} are the empirical parameters [9]. The parameters used in fitting the mobilities for the four channel planes at temperatures ranging from 300K to 450K are listed in Table 1. On the $(11\bar{2}0)$ channel plane, μ_c is proportional to $N_S^{1.1}$. However, on the other

three channel planes, μ_c is proportional to $N_S^{1.0}$. It means that fewer inversion carriers on the $(11\bar{2}0)$ channel plane would be affected by the Coulomb scattering. On the four channel planes, μ_{op} is proportional to $E_{eff,SiC}^{-0.3}$, which is consistent with the reported result [9]. Moreover, the value of δ of the $(11\bar{2}0)$ channel plane is larger than that of the other three channel planes, indicating that μ_{sr} is larger on the $(11\bar{2}0)$ channel plane.

Table 1. Parameters used in fitting the mobilities for four different channel planes at temperatures ranging from 300K to 450K

Parameters	Units	Channel planes		
		$(11\bar{2}0)$	$(\bar{1}\bar{1}20)$	$(1\bar{1}00)$ & $(\bar{1}100)$
Γ_C	$[K^{-1}V^{-1}s^{-1}]$	1e10	5e10	2e10
N_T	$[cm^{-2}]$	3.4e13	4.8e13	4e13
N_{SCR}	$[cm^{-2}]$	1e10	5e10	1.5e10
ξ_C		1.1	1.0	1.0
δ	$[Vs^{-1}]$	5e13	3.8e13	4.3e13
$\hbar\omega_{OP}$	[eV]	0.12	0.12	0.12
n		-0.3	-0.3	-0.3
C_{OP}	$[cm^{(n+2)}V^{-(n+1)}s^{-1}]$	2e2	2e2	2e2



(a) (b)

Fig. 8. FE mobility vs V_{gs}-V_{th} at room temperature for four channel planes: (a) $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$, and (b) $(1\bar{1}00)$ and $(\bar{1}100)$.

Figures 8 (a) and (b) show experimental data of the mobility on $(11\bar{2}0)$ channel plane for the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET at 300K and 450K, respectively. Calculated total mobility takes into account the contributions from Coulomb scattering mobility, optical phonon scattering mobility, and surface roughness scattering mobility. For all channel planes, the calculated total mobility is well agreed with the experimental data of the mobility. The values of the coefficient of determination (R-squared) for the mobility fittings are above 85% at various temperatures. The total mobility at each temperature is divided into the three components based on Equation (1), as shown in Fig. 8. At low $E_{eff,SiC}$, the Coulomb scattering is dominated; however, the surface roughness scattering is the limiting factor when $E_{eff,SiC}$ is high. When the measured temperature is increased, the optical phonon scattering becomes severe.

Figure 9 shows the three mobilities (μ_{op}, μ_c, and μ_{sr}) against temperatures at $E_{eff,SiC}$ = 0.8 MV/cm for the $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET. μ_{op} is the same for the four channel planes, which is independent of channel faces. Among the four channel planes, the $(11\bar{2}0)$ channel plane has the largest μ_c and μ_{sr}. It is because that this channel plane achieves the least deviation from the

crystallographically accurate crystal plane [10], as shown in Fig. 10. The accurate crystal plane reduces surface roughness and dangling bonds [11]. Therefore, the taper angle of the trench sidewall can be tuned to achieve a precise $(11\bar{2}0)$ channel plane to realize a higher channel mobility [12].

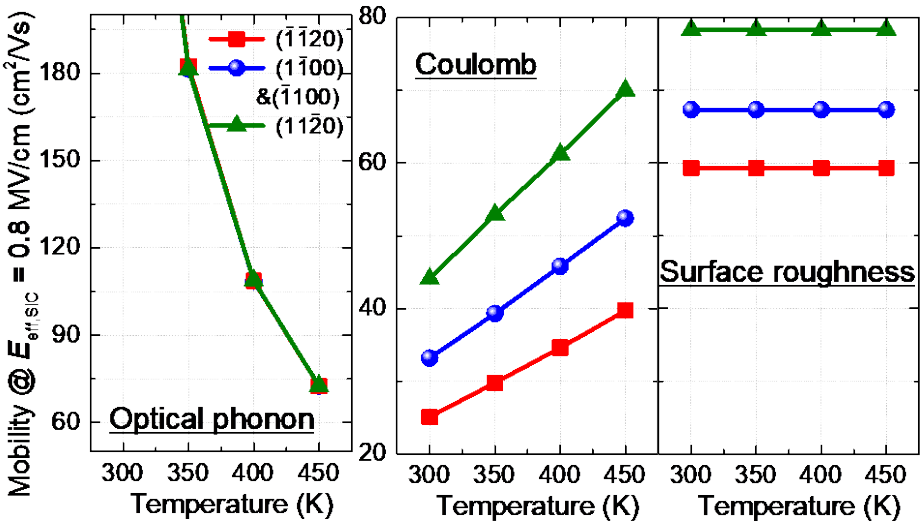


Fig. 9. Plots of the different mobilities against temperatures at $E_{eff,SiC}$ = 0.8 MV/cm for $Al_2O_3/LaAlO_3/SiO_2$ trench gate MOSFET: (a) optical phonon scattering mobility, (b) Coulomb scattering mobility, and (c) surface roughness scattering mobility.

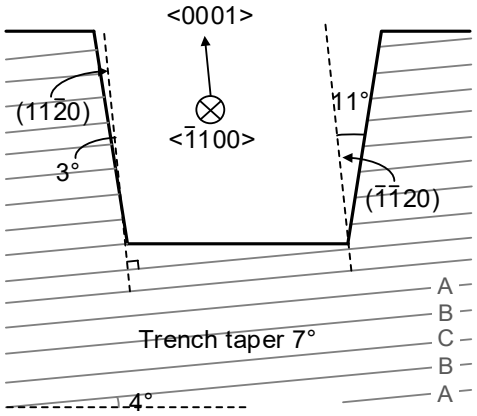


Fig. 10. Cross-sectional schematic of trench shape seen from <1̄100> crystal direction.

Summary

In this paper, the $Al_2O_3/LaAlO_3/SiO_2$ gate stack was designed and implemented on various channel planes for using in trench gate MOSFETs. The passivation of the deposited-SiO_2/SiC interface was first optimized, and it demonstrated that the NO annealing for 70 mins shows the lowest D_{it} and longer duration has no further improvement on D_{it}. Subsequently, the high-k gate stack on MOS capacitor was designed, which exhibits a considerable improvement in the gate blocking capability (~1.73X) and a slightly increased D_{it}, in comparison to the SiO_2 MOS capacitor. Finally, the high-k gate stack was implemented on various trench-gate channel planes. The high-k trench gate MOSFETs conduct a drain current ~1.3 times higher than that of the SiO_2 trench gate MOSFETs on all 24 channel planes at the same overdrive voltage of 10 V. Moreover, the mobility limiting mechanisms on various channel planes were discussed and analyzed. It turns out that the $(11\bar{2}0)$ channel plane has the largest Coulomb scattering mobility and surface roughness scattering mobility.

Acknowledgement

The authors would like to thank the staff of Fuji Electric Company, Ltd., the staff of the Nanosystem Fabrication Facility (NFF) of HKUST, and the staff of the Materials Characterization and Preparation Facility (MCPF) of HKUST, for their technical advice and help in device fabrication and characterization. The authors appreciate the supports by Fuji Electric Company, Ltd., under Grant RDC 2021158-0, and the Research Grants Council of Hong Kong, under Research Impact Fund R6008-18.

References

[1] T. Hosoi, S. Azumo, Y. Kashiwagi, S. Hosaka, R. Nakamura, S. Mitani, Y. Nakano, H. Asahara, T. Nakamura, T. Kimoto, T. Shimura, and H. Watanabe, in International Electron Devices Meeting (2012), pp. 10-13.

[2] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo, and P. Godignon, Materials Science in Semiconductor Processing, 78 (2017).

[3] R. Suri, C.J. Kirkpatrick, D.J. Lichtenwalner, and V. Misra, Appl. Phys. Lett., 96, 042903 (2010).

[4] M. Suzuki, T. Yamaguchi, N. Fukushima, and M. Koyama, J. Appl. Phys., 103, 034118 (2008).

[5] L. Huang, Y. Liu, X. Peng, Y. Onozawa, T. Tsuji, N. Fujishima, and J.K.O. Sin, IEEE Trans. Electron Devices, 69, 2 (2022).

[6] L. Huang, Y. Liu, X. Peng, T. Tsuji, Y. Onozawa, N. Fujishima, and J.K.O. Sin, IEEE Trans. Electron Devices, 70, 2 (2023).

[7] T. Kimoto and H. Watanabe, Appl. Phys. Exp., 13, 120101 (2020).

[8] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology (Wiley, Singapore, 2014).

[9] K. Kutsuki, Y. Watanabe, Y. Yamashita, N. Soejima, K. Kataoka, T. Onishi, K. Yamamoto, and H. Fujiwara, Solid-State Electronics, 157 (2019).

[10] H. Yano, H. Nakao, H. Mikami, T. Hatayama, Y. Uraoka, and T. Fuyuki, Appl. Phys. Lett., 90, 042102 (2007).

[11] K. Kutsuki, E. Kagoshima, T. Onishi, J. Saito, N. Soejima, and Y. Watanabe, in International Electron Devices Meeting (2019), pp. 20.3.1-20.3.4.

[12] H. Yano, H. Nakao, T. Hatayama, Y. Uraoka and T. Fuyuki, Mater. Sci. Forum, 556-557 (2007).