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Channel Density Design Guidelines for the Transient Characteristics of SiC Trench Gate MOSFETs

Shinichi Kimoto[1,a*], Ryosuke Iijima[2,b], and Shinsuke Harada[1,c]

[1]National Institute of Advanced Industrial Science and Technology, 16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan

[2]Toshiba Corporation, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Kanagawa 212-8582, Japan

[a]shinichi1.kimoto@toshiba.co.jp, [b]ryosuke.iijima@toshiba.co.jp, [c]s-harada@aist.go.jp

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Abstract. Channel density design guidelines for SiC trench-gate MOSFETs with low switching loss, and high short-circuit and avalanche capabilities were proposed. The cell and grounding region pitches were used as parameters to control the channel density to investigate the parameter dependence of each transient property. The results suggest a clear difference in the dependence of switching loss reduction and short-circuit/avalanche capability increase on these parameters; however, the extents of dependence of specific on-resistance on the controlling parameters were comparable. The reduction in the grounding region pitch contributed to faster charging of the parasitic drain-source capacitance, which was effective in improving transient characteristics, such as *dV/dt* at turn-off, and saturation current at short-circuit. Furthermore, a reduction in this distance increased the area-flowing avalanche current and hence, an increase in the avalanche energy. The influence of the two design parameters in effectively improving the trade-off between each transient characteristic and the specific on-resistance was summarized.

Introduction

SiC trench-gate MOSFETs have a significant effect in increasing their channel density. In particular, deep-channel MOSFETs (DC-MOSFETs) featuring a deep n^+ source region and buried interlayer dielectric in the trench achieved a reduction in specific on-resistance ($R_{on}A$) with a cell pitch (W_{cell}) of 2.0 μm or less [1]. DC-MOSFETs have a p^+ shielding region under the trench-gate through a self-aligned process, causing them to suppress the electric field when a drain-source voltage (V_{DS}) is applied. Formation of the grounding region is required to connect the p^+ shielding region to the source potential. A periodic grounding along the striped trench-gate has been proposed as an effective grounding method for narrow W_{cell} trench-gate MOSFETs [2, 3]. The grounding density should be lowered in terms of $R_{on}A$ because a higher grounding density implies reduced channel density. However, the channel density should be designed comprehensively, considering the transient performance. It has been reported that increasing the grounding density improves the short-circuit capability [3, 4]. In this study, we investigated the dynamic characteristics and withstand capabilities of SiC trench-gate MOSFETs when $R_{on}A$ was varied using two parameters, W_{cell} and grounding region pitch (D_G), which can structurally control the channel density. We proposed guidelines for how W_{cell} and D_G should be designed to improve the trade-offs with $R_{on}A$.

Structural Design and Conditions for Comparison

Channel Density Design. Fig. 1 (a) shows the perspective structure of a DC-MOSFET, with the p^+ shielding and grounding regions partially extracted. This DC-MOSFET had a drift layer of 4.7 μm for 650 V-class and a substrate of 333 μm. The design parametric values investigated in this study were 1.6, 1.8, and 2.0 μm for W_{cell}, and 10, 30, and 90 μm for D_G. First, W_{cell} was fixed at 1.8 μm, while D_G was varied; similarly, D_G was fixed at 30 μm, while W_{cell} was varied. The length of the grounding region (L_G) was set to 2.8 μm, which was a fixed value independent of D_G. Fig. 1 (b) shows

the channel density ratio versus R_{onA} (the median value of approximately 30 devices) based on designs with either W_{cell} (= 1.8 μm) or D_G (= 30 μm) being fixed, while the other was varied. When W_{cell} was narrowed, the channel density increased and R_{onA} decreased. Although the narrowing of W_{cell} indicates a reduction in the JFET width (W_{JFET}), R_{onA} decreased because the increase in the JFET resistance (R_{JFET}) would be smaller than the increase in the channel density. On the other hand, when D_G was shortened, the channel density decreased and R_{onA} increased. Within the range of W_{cell} and D_G investigated, the trend of R_{onA} with the channel density ratio was consistent. This suggests that a targeted R_{onA} can be approached by controlling either D_G or W_{cell}.

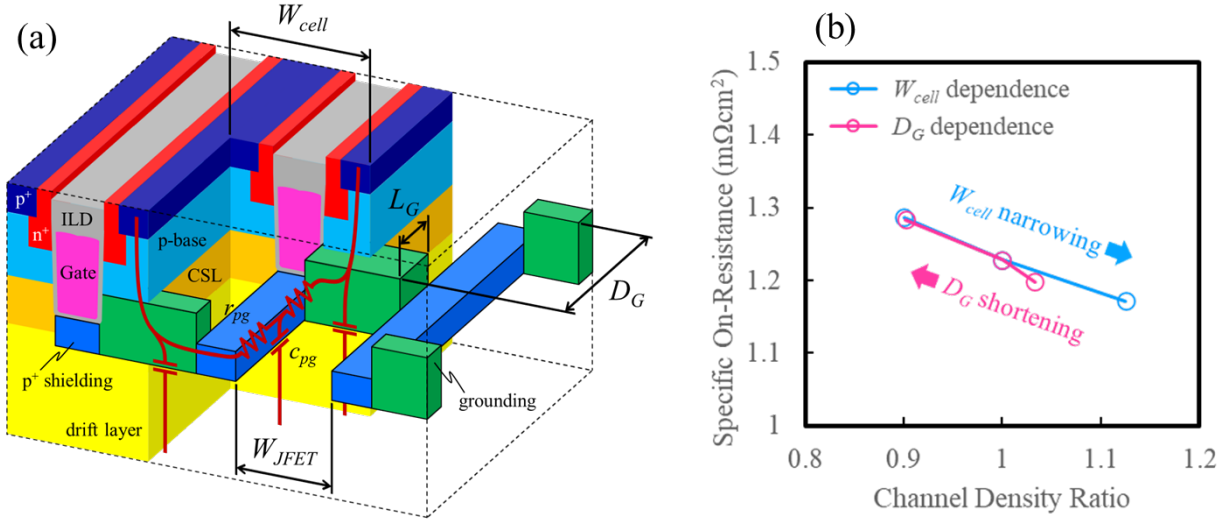

Fig. 1. (a) Perspective structure of the DC-MOSFET with partially extracted p^+ shielding and grounding regions. (b) Channel density ratio versus R_{onA}, with D_G varying (while W_{cell} was fixed at 1.8 μm), and W_{cell} varying (while D_G was fixed at 30 μm).

Effects of Grounding Region Pitch (D_G). Fig. 2 (a) shows cross-sectional schematics of the local resistance and capacitance parasitic to p^+ shielding and grounding regions. The parasitic resistance and capacitance in the half of D_G (5 μm) are defined as r_{pg} and c_{pg}, respectively. Thus, the parasitic resistance and capacitance for D_G = 10, 30, and 90 μm would be r_{pg}, $3r_{pg}$, and $9r_{pg}$, and c_{pg}, $3c_{pg}$, and $9c_{pg}$, respectively, considering the distance contributed by one grounding point. Fig. 2 (b) shows the simplified equivalent circuits corresponding to Fig. 2 (a), representing different numbers of drain-source RC circuit stages for each condition. The RC time constant in this local RC circuit is expressed by

$$\tau_{pg} = r_{pg} c_{pg} \left(\frac{D_G}{10} \right)^2 . \quad (1)$$

Fig. 2 (c) shows the RC time constants (the subscript represents the value of D_G) for each D_G. Eq. 1 shows that τ_{pg} is proportional to D_G squared, and the relationship of $\tau_{pg90} = 9\tau_{pg30} = 81\tau_{pg10}$ is expressed. Thus, a longer D_G implies that the charging and discharging of the drain-source capacitance (C_{DS}) takes a long time and degrades the transient response [5].

Fig. 3 (a) shows the top view of the main diffusion area in the active region. The yellow box indicated by D_G and $2W_{cell}$ is the unit area considering the grounding region, and the total area of the p^+ shielding and grounding regions in this active area (A_{PG}) is given by

$$A_{PG} = \frac{W_t}{W_{cell}} A + \frac{L_G (W_{cell} - W_t)}{2 D_G W_{cell}} A, \quad (2)$$

where W_t is the trench width and A is the active area. Fig. 3 (b) shows the D_G dependence of A_{PG} for W_{cell} = 1.8 μm, W_t = 0.7 μm, L_G = 2.8 μm, and A = 0.053 cm^2. The A_{PG} values for D_G = 10, 30, and 90 μm are indicated by red circles, and the values of the ratio of the occupancy to the active area A_{PG}/A were 47.4%, 41.7%, and 39.8%, respectively. Thus, A_{PG}/A approaches 38.9%, as D_G increased because the second term in Eq. 2 approaches zero. Because A_{PG} is the area where the drain cut-off current (I_{DSS}) or avalanche current (I_{AV}) flows when V_{DS} is applied, an extension of D_G implies an increase in current density through A_{PG}.

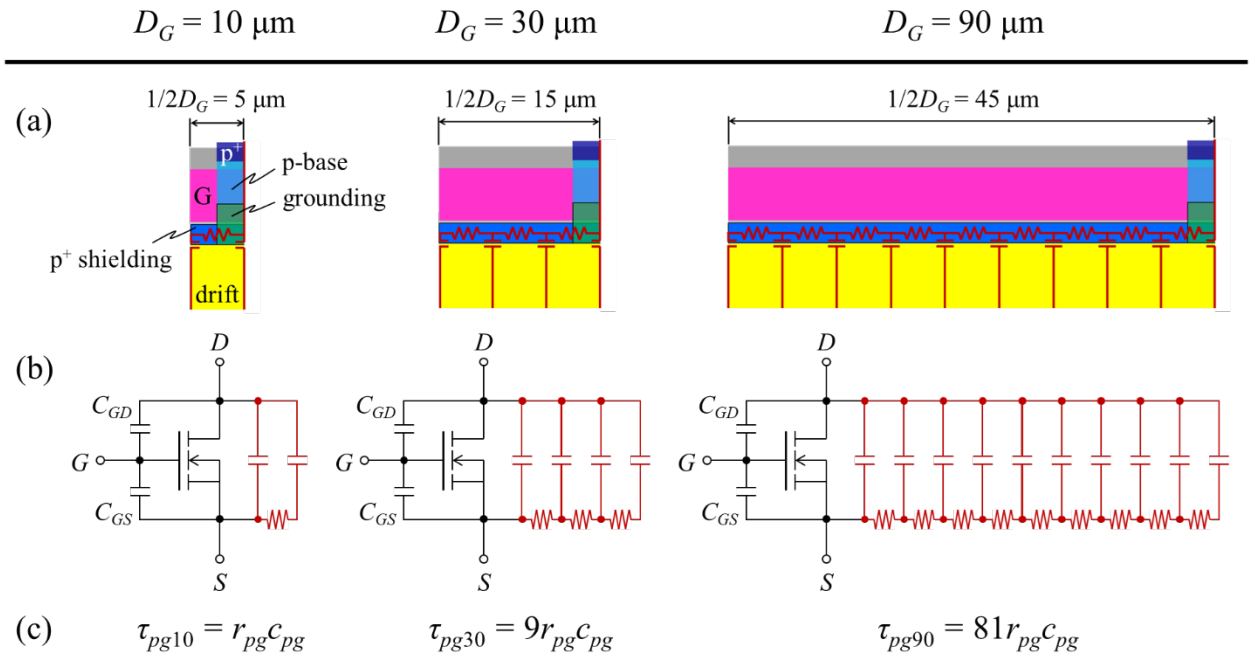

Fig. 2. (a) Cross-sectional schematic of the local parasitic resistance and parasitic capacitance in the p$^+$ shielding and grounding regions. (b) Simplified equivalent circuits for schematics shown in (a). (c) RC time constants for each D_G shown in (a).

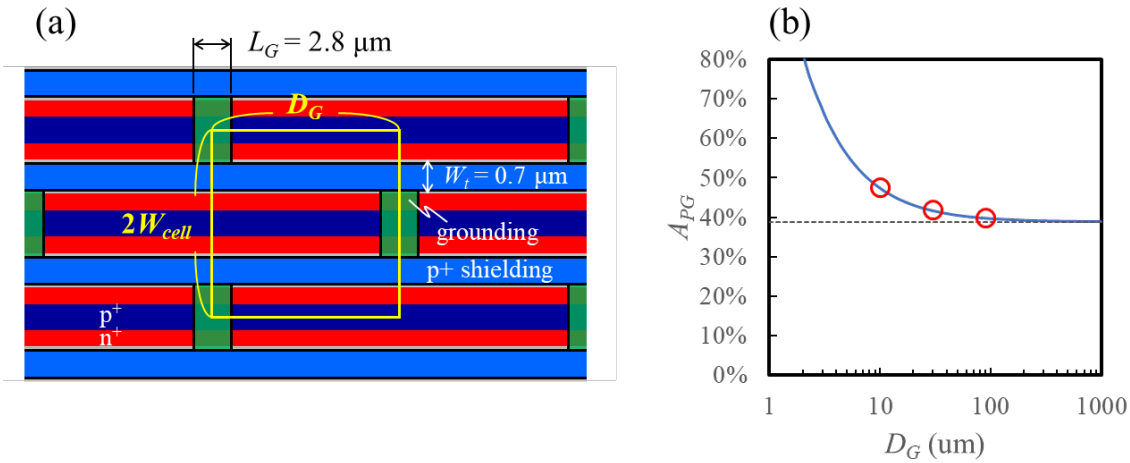

Fig. 3. (a) Top view of the main diffusion area in active region. (b) D_G dependence of A_{PG} for W_{cell} = 1.8 μm, W_t = 0.7 μm, L_G = 2.8 μm, and A = 0.053 cm^2. Red circles indicate A_{PG} values for D_G = 10, 30, and 90 μm, respectively.

Experimental Results

Dynamic Characteristics. Fig. 4 (a) and (b) present the turn-off waveforms of V_{DS} at room temperature (RT). The switching conditions were as follows: gate-source voltage (V_{GS}) = +20/–5 V; DC bus voltage (V_{bus}) = 300 V; external gate resistance (R_G) = 75 Ω; drain current (I_D) = 18 A; and

inductance (L) = 1 mH. Focusing on the starting time of the rise in V_{DS} in the turn-off waveforms, a shift to the right is observed in Fig. 4 (a), with a reduction in W_{cell}, whereas no D_G dependence is noticed in Fig. 4 (b). In contrast, focusing on dV/dt, no W_{cell} dependence is observed in Fig. 4 (a), while it increases with D_G shortening, as shown in Fig. 4 (b). The switching losses (E_{SW}) shown in Fig. 4 (c) and (d) reflect the dV/dt trends, especially the turn-off losses (E_{off}), indicating that shortening of D_G was effective in reducing E_{SW}.

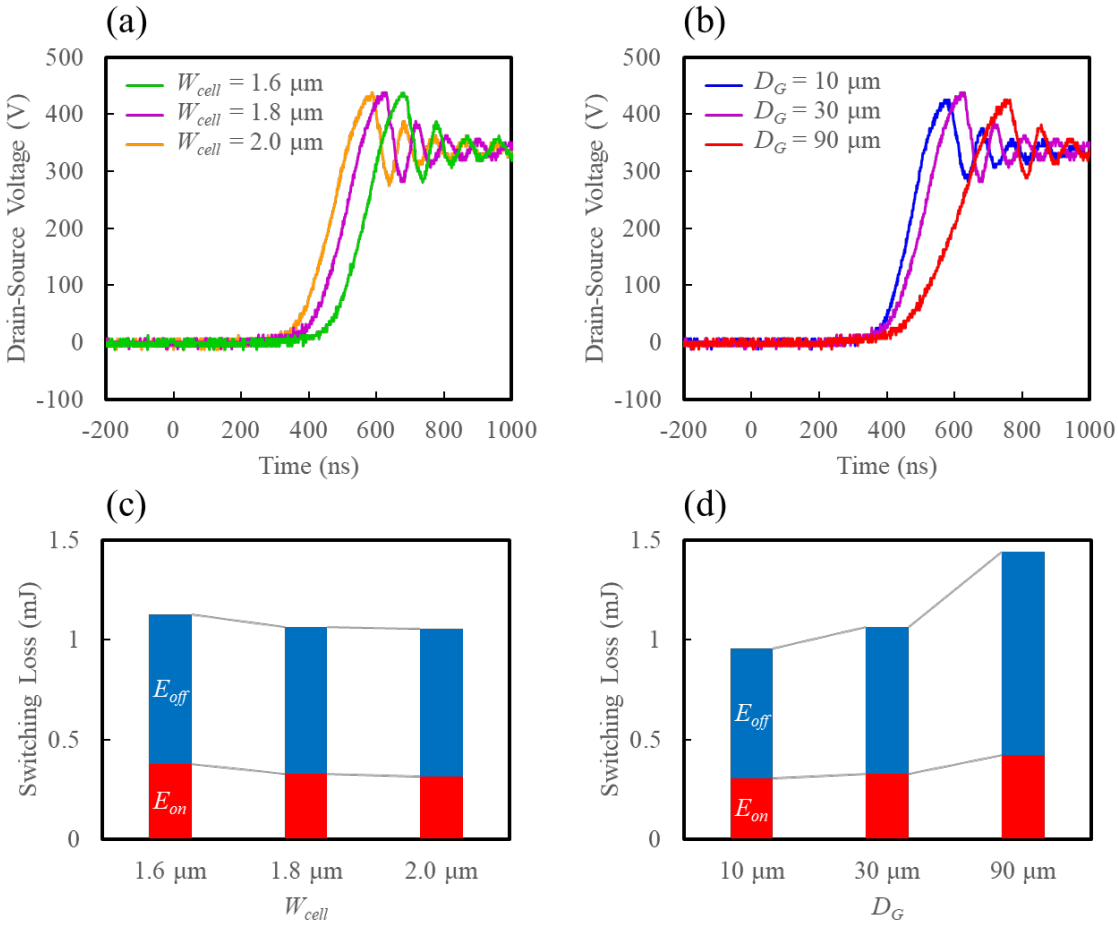

Fig. 4. Turn-off waveforms of V_{DS} for (a) W_{cell} and (b) D_G dependence. Switching losses for (c) W_{cell} and (d) D_G dependence.

Fig. 5 shows the dependence of the capacitance characteristics on V_{DS} at a frequency (f) of 1 kHz. As shown in Fig. 5 (a), the input capacitance (C_{iss}) (sum of gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD})) increased with the narrowing of W_{cell}, resulting in an increase in the gate charge (Q_G) and gate-delay time, as shown in Fig. 4 (a). The difference near V_{DS} = 10 V was due to W_{JFET}, indicating that the pinch-off voltage (V_P) decreased with the narrowing of W_{JFET}. In contrast, Fig. 5 (b) shows an increase in C_{GS} and a decrease in C_{GD} with the shortening of D_G. A reduction in D_G meant that a portion of C_{GD} was replaced with C_{GS}, while C_{iss} and Q_G remained unchanged. Thus, there was no difference in the gate-delay time, as shown in Fig. 4 (b).

Fig. 6 shows the dependence of the capacitance characteristics on f at V_{DS} = 300 V. Almost no dependence of the capacitance on W_{cell} is observed in the measured f range in Fig. 6 (a). However, as shown in Fig. 6 (b), there is D_G dependence, with C_{GS} and C_{DS} decreasing, and C_{GD} increasing in the high-f range. As shown in Fig. 2, the extension of D_G contributed to the longer charging time of C_{DS}, suggesting that the potential of the p^+ shielding region, especially far from the grounding point, was increased by V_{DS}. Consequently, C_{GS} and C_{DS} were transiently replaced by C_{GD} in the high-f range, where C_{DS} charging was insufficient. The D_G dependence of dV/dt shown in Fig. 4 (b) reflects the charging time of C_{DS}, and fast charging of C_{DS} contributed to a reduction in E_{SW}.

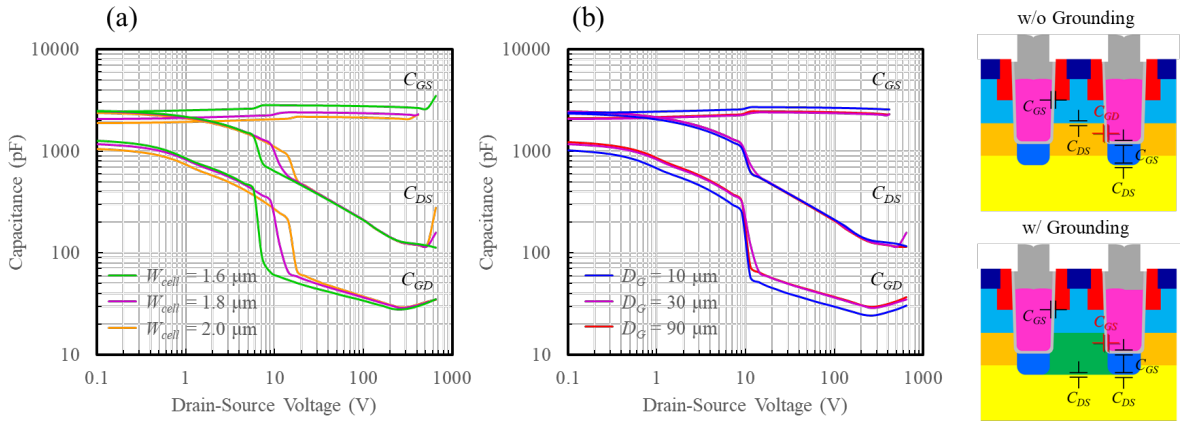

Fig. 5. Variation of capacitance characteristics with V_{DS} at f = 1 kHz for different values of (a) W_{cell} and (b) D_G.

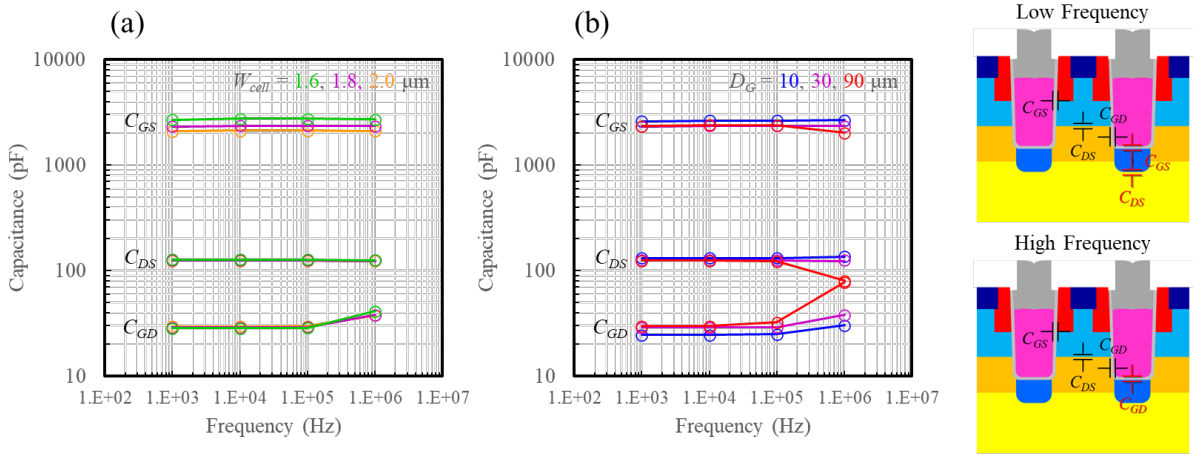

Fig. 6. Variation of capacitance characteristics with f at V_{DS} = 300 V for different values of (a) W_{cell} and (b) D_G.

Short-Circuit Capability. Fig. 7 (a) and (b) present the short-circuit waveforms at RT for the final test before the device destruction. The test conditions were as follows: V_{GS} = +20/0 V; V_{bus} = 300 V; on-side external gate resistance ($R_{G(on)}$) = 22.4 Ω; and off-side external gate resistance ($R_{G(off)}$) = 500 Ω. In Fig. 7 (a), a slight increase in the drain peak current ($I_{SC(peak)}$) and a decrease in the short-circuit withstand time (t_{SC}) are observed with the narrowing of W_{cell}. This may be attributed to the balance between the reduction in V_P due to the narrowing of W_{JFET}, and the increase in the channel density. However, in Fig. 7 (b), a relatively large decrease in $I_{SC(peak)}$ and an increase in t_{SC} are observed with the shortening of D_G. This suggests that in addition to the lower channel density, the improved RC delay in the p^+ shielding region, as given by Eq. 1 allowed for a fast pinch-off in the JFET region, which resulted in a lower $I_{SC(peak)}$ and longer t_{SC}. Fig. 7 (c) shows the f dependence of the drain-source impedance, and D_G dependence is observed above f = 10 MHz. The gate and source were connected to the ground potential, and the drain-source DC voltage = 1 V. This D_G dependence implies a difference in the pulse period below 100 ns; furthermore, a fast depletion of the p^+ shielding region owing to the low impedance contributes to t_{SC} improvement.

Avalanche Capability. Fig. 8 (a) and (b) show the unclamped inductive switching (UIS) waveforms at RT for the final test before the device destruction. The test conditions were as follows: V_{GS} = +20/0 V; V_{bus} = 300 V; $R_{G(on)}$ = 22.4 Ω; $R_{G(off)}$ = 500 Ω; and L = 1 mH. An increase in the avalanche current density through the active area ($J_{AV} = I_{AV}/A$) was observed for both W_{cell} narrowing and D_G shortening. From Eq. 2, the avalanche current density through A_{PG} ($J_{PG} = I_{AV}/A_{PG}$) is expected to decrease because A_{PG}/A increases with W_{cell} narrowing and D_G shortening. Considering the device heating due to J_{PG}, a reduction in J_{PG} implies an increase in the avalanche energy (E_{AV}). A_{PG}

dependence of E_{AV}, presented in Fig. 8 (c), shows an increase in E_{AV} with A_{PG} expansion. Thus, W_{cell} narrowing and D_G shortening contributed to an increase in E_{AV}.

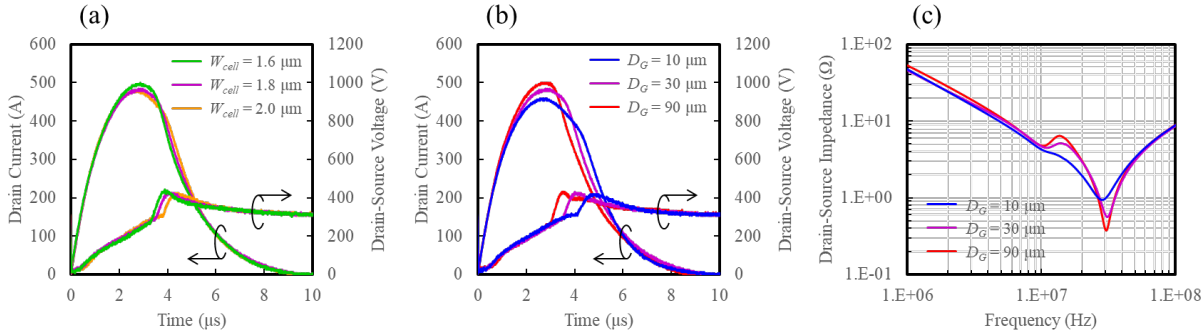

Fig. 7. Short-circuit waveforms at RT for the final test before the device destruction for (a) W_{cell} and (b) D_G dependence. (c) f dependence of absolute value of drain-source impedance.

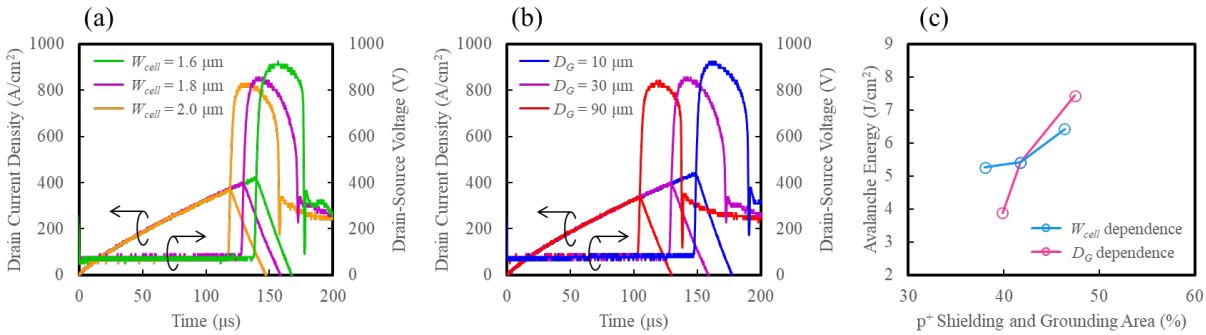

Fig. 8. UIS waveforms at RT for the final test before the device destruction for (a) W_{cell} and (b) D_G dependence. (c) A_{PG} dependence of E_{AV}.

Trade-offs with $R_{on}A$. Fig. 9 (a), (b), and (c) show the $R_{on}A$ dependence of E_{SW}, t_{SC}, and E_{AV}, respectively. As shown by the trade-off between E_{SW} and $R_{on}A$, shown in Fig. 9 (a), the slope of D_G dependence was larger than that of the W_{cell} dependence. Therefore, D_G shortening was more advantageous than W_{cell} widening to reduce E_{SW}. The trade-off between t_{SC} and $R_{on}A$, shown in Fig. 9 (b), implies that the slope of D_G dependence was larger than that of the W_{cell} dependence, indicating that D_G shortening was more effective for increasing t_{SC}. The relationship between E_{AV} and $R_{on}A$, shown in Fig. 9 (c), reveals that both W_{cell} narrowing and D_G shortening could improve E_{AV}. From the above, it is desirable to reduce $R_{on}A$ as much as possible by W_{cell} narrowing and then improve the transient characteristics by D_G shortening.

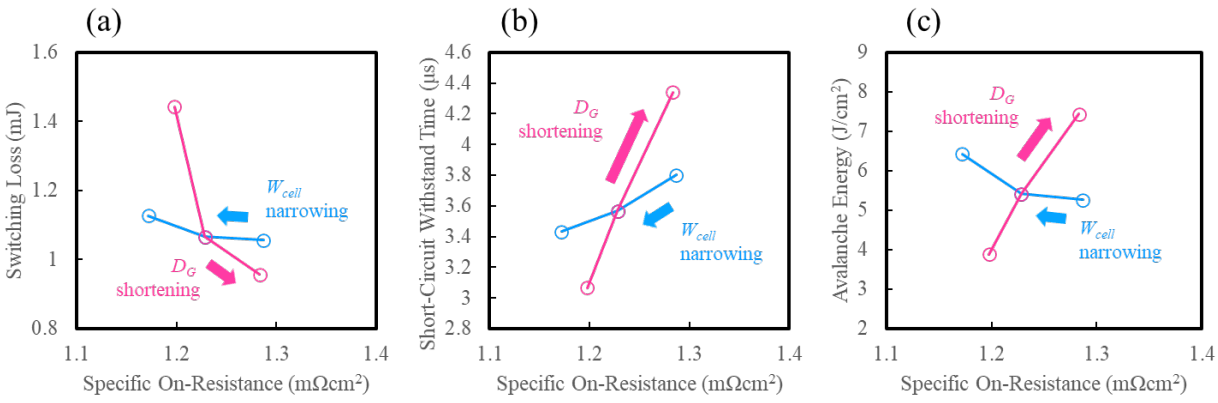

Fig. 9. $R_{on}A$ dependence of (a) E_{SW}, (b) t_{SC} and (c) E_{AV}.

Summary

Design guidelines for channel density control through W_{cell} and D_G were proposed. Under the design conditions investigated in this study, (W_{cell} = 2.0 μm and D_G = 30 μm), and (W_{cell} = 1.8 μm and D_G = 10 μm) yielded almost the same channel density and $R_{on}A$. However, E_{SW}, t_{SC}, and E_{AV} in the latter condition showed a clear improvement compared to the former. The lower channel density due to D_G shortening resulted in a faster depletion of the p^+ shielding region when V_{DS} was applied, thus improving dV/dt in the turn-off waveform and t_{SC} in the short-circuit mode. Furthermore, a larger grounding area reduced the avalanche current density in the current path and improved E_{AV} in the avalanche mode. These effects were larger than the reduction in channel density due to W_{cell} narrowing. To effectively improve the trade-offs between $R_{on}A$ and transient characteristics in structural design, the design guidelines of $R_{on}A$ reduction by W_{cell} narrowing and transient characteristics improvement by D_G shortening are important.

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References

[1] S. Kimoto, et al., Key Eng. Mater. 947, 63 (2023).

[2] M. Sampath, et al., Mater. Sci. Forum 1004, 751 (2020).

[3] Y. Fukui, et al., Mater. Sci. Forum 1004, 764 (2020).

[4] R. Tanaka, et al., Proceedings of the 26th ISPSD, Waikoloa, HI, USA, 75-78 (2014).

[5] Y. Kagawa, et al., Mater. Sci. Forum 778-780, 919 (2014).