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Analysis of On-State and Short-Circuit Capability in 3D Trench SiC MOSFET Designs

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Abstract. Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are successfully replacing traditional silicon insulated gate bipolar transistors (Si IGBTs) in power applications. Nonetheless, two crucial challenges persist: gate-oxide reliability and a reduced short circuit (SC) withstand time. This paper explores a novel MOSFET structure, which is designed to address these concerns and compares it with existing designs through extensive 3D TCAD simulations. The proposed MOSFET structure features a p-region under the gate, providing a unique configuration for improved performance during SC events. This novel structure is then compared to two commercially realized MOSFET structures. Our structure has a superior on-state performance with a specific resistance of 1.48 mΩ /cm^2, showing an improvement by 25 % and 15 %, respectively. It also increases the blocking capability by 100 V and SC withstand time in comparison to the double-trench MOSFET.

Introduction

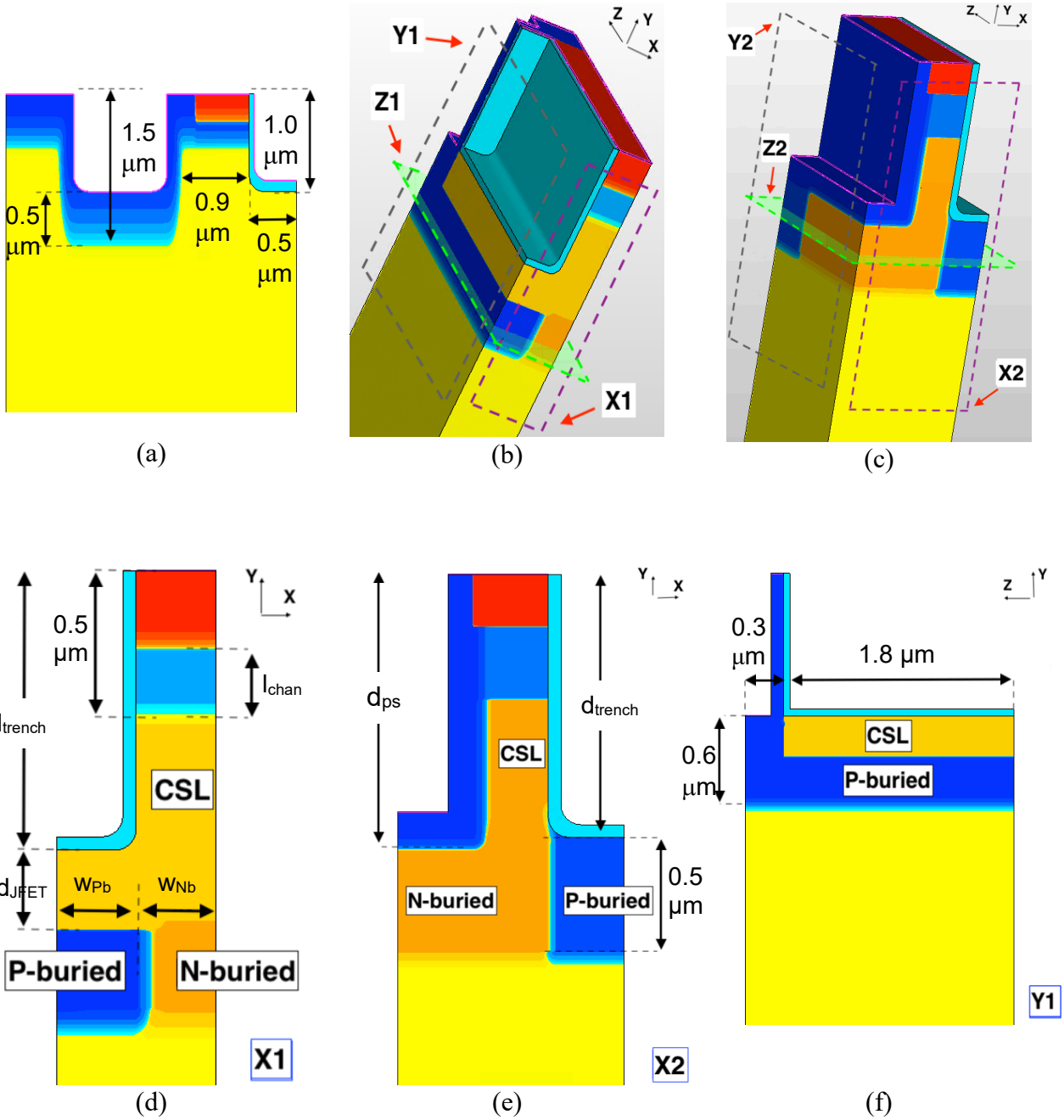
SiC MOSFETs have been gradually replacing Si IGBTs in the power traction applications due to their superior switching loss performance and increased power density [1]. However, there are two major reliability concerns regarding SiC MOSFETs, including increased electric fields (EFs) and trap densities in the gate-oxide, making it a vulnerable region. In comparison to Si IGBTs, the higher thermal conductivity events can lead to a faster oxide failure during SC events and shorting of the gate-source contacts before reaching the critical melting temperature of 4H-SiC [2,3]. Hence, these devices cannot match typical Si IGBT withstand times of 10 µs SC or higher without permanently damaging the device or severely altering its on-state characteristics [4].

There are several device designs have been developed to overcome this shortcoming, most prominently super junction (SJ) MOSFETs [5], trench-etched-double-diffused MOS (TEDMOS) [6], scaled gate-charge MOSFET [7] and MOSFETs with an incorporated body JFET region [4]. However, SJ MOSFET and TEDMOS devices are costly to fabricate due to their requirement for deep implantations and multiple trench formations. In the scaled gate-charge MOSFET, it is possible to reduce the saturation current and increase the SC withstand time by reducing the oxide thicknesses below 50 nm [7]. However, the reliability of thin oxides has been shown to be problematic, and threshold voltage shift of commercial SiC devices is already an issue when deploying typical oxide thicknesses of 50 nm or higher [8]. The integrated JFET MOSFET structure proposed in [4] reduces the saturation current, which results in a longer SC withstand time. However, the gate oxide is still exposed to high EFs and temperatures.

In this work, we present a new MOSFET structure, with a source-connected p-region under the gate and compare it to the state-of-the-art topologies using 3D TCAD simulations. Three structures are analysed, namely the double trench MOSFET serving as a benchmark [3], MOSFET with the incorporated p-layer between active trenches, and the presented novel MOSFET design. On-state, off-state, transfer and short-circuit simulation results will be compared for all three structures and presented in the sub-sections below.

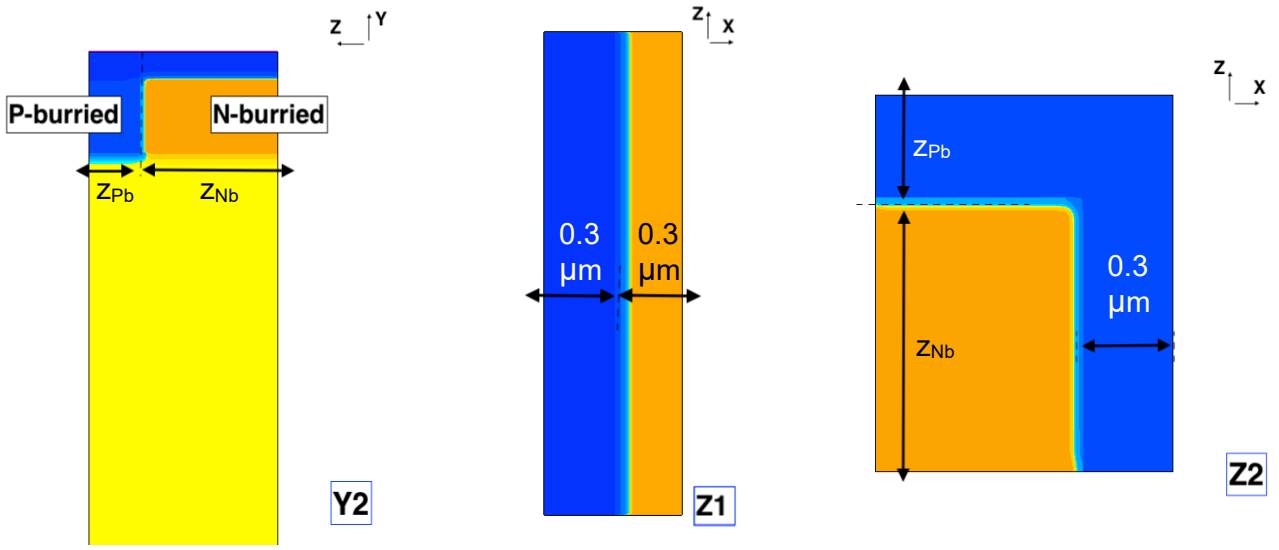
Structure Description

All three structures are shown in Fig. 1 together with their key physical dimensions and detailed cross-sectional images. It is important to note that the double trench MOSFET and the device that represents a commercial patent are named as *structure A* and *structure B* throughout the paper. For a fair comparison, all three devices have the same drift layer thickness and doping concentration, set as 10 µm and $9x10^{15}$ cm^{-3}. The trench depth (d_{trench}) is 1 μm, channel length (l_{chan}) is 0.3 µm and oxide thickness is kept at 50 nm in all designs. The half-cell pitch for the *structure A* is 3 µm, 0.6 µm for the *structure B* design and 0.9 µm in the proposed MOSFET. Note, that all structures are matched with an area factor to provide a current density in A/cm^2.



(a) (b) (c)

(d) (e) (f)



(g) (h) (i)

Fig. 1. Structure Description: (a) *Structure A* MOSFET, (b) *Structure B* MOSFET, (c) Proposed MOSFET, (d) XY cutline X1, (e) XY cutline X2, (f) ZY cutline Y1, (g) ZY cutline Y2, (h) XZ cutline Z1 and (i) XZ cutline Z2.

All physical dimensions of the double-trench MOSFET are depicted in the Fig.1 (a), interpreted from the source [3]. The charge spreading layer (CSL), p-buried and n-buried layers of both the proposed structure and *structure B* MOSFETs are denoted in the Fig. 1 (d-g). The formed JFET in *structure B* with p and n-buried layers is 0.3 µm (d_{JFET}) deep under the trench, with openings in the x-direction of 0.3 μm ($w_{Pb.}$ and w_{Nb}) wide and deep. As shown in the Fig. 1 (f), the 6 to 1 (1.8 µm to 0.3 µm) half-cell ratio was selected in the Z-direction between active and p-source trench, for *structure B*. The following parameter controls the on-state resistance and, as a result, the SC characteristics. Through additional simulations, results of which are not shown in this paper, the 6 to 1 ratio was found to be ideal, where the on-state performance saturates if the ratio is increased and worsens if the ratio is lowered. Additionally, higher ratios will increase the size of the mesh, leading to a significant computational burden.

The distinctive feature of the proposed structure is the introduction of a trench p-source contact with a p-layer extending directly under the gate trenches, partially covering this area, whilst fully covering the active trench. The p-source trench is 1.1 µm (d_{ps}) deep and has a doping concentration of $5x10^{18}cm^{-3}$. The half-cell width of the p-source trench is 0.3 µm, same as half-cell width of the active trench in both, proposed and *structure B*. The opening of p and n-buried layers in the Z-direction is 0.3 µm (z_{Pb}) and 0.8 µm (z_{Nb}) wide, respectively. Both layers are 0.5 µm deep in the proposed MOSFET, as shown in the Fig. 1 (e). The p-buried layer in the proposed MOSFET is $1x10^{18}cm^{-3}$ doped, while the p-source trench and p-buried layer in the *structure B* is doped with $5x10^{18}cm^{-3}$ concentration.

On-State and Off-State Performance

To select the appropriate doping concentrations of the CSL and n-buried layers, off-state simulations were studied to assess the limit of the maximum doping. The optimization criteria includes that at near breakdown, the EF is not concentrated at the gate oxide and can be kept below 3 MV/cm [cooper, TDDB]. As a result, this will mitigate gate-oxide reliability concerns and push the EF under the gate trench, thereby addressing a primary factor in the formation of localized hotspots during short-circuit (SC) conditions [4,5]. Higher doping concentrations of the CSL and n-buried layer lead to an improved on-state performance at expense of blocking capability and increased oxide EF. The off-state and on-state simulations of the *structure A*, optimized *structure B* and proposed MOSFET can be seen in the Fig. 2:

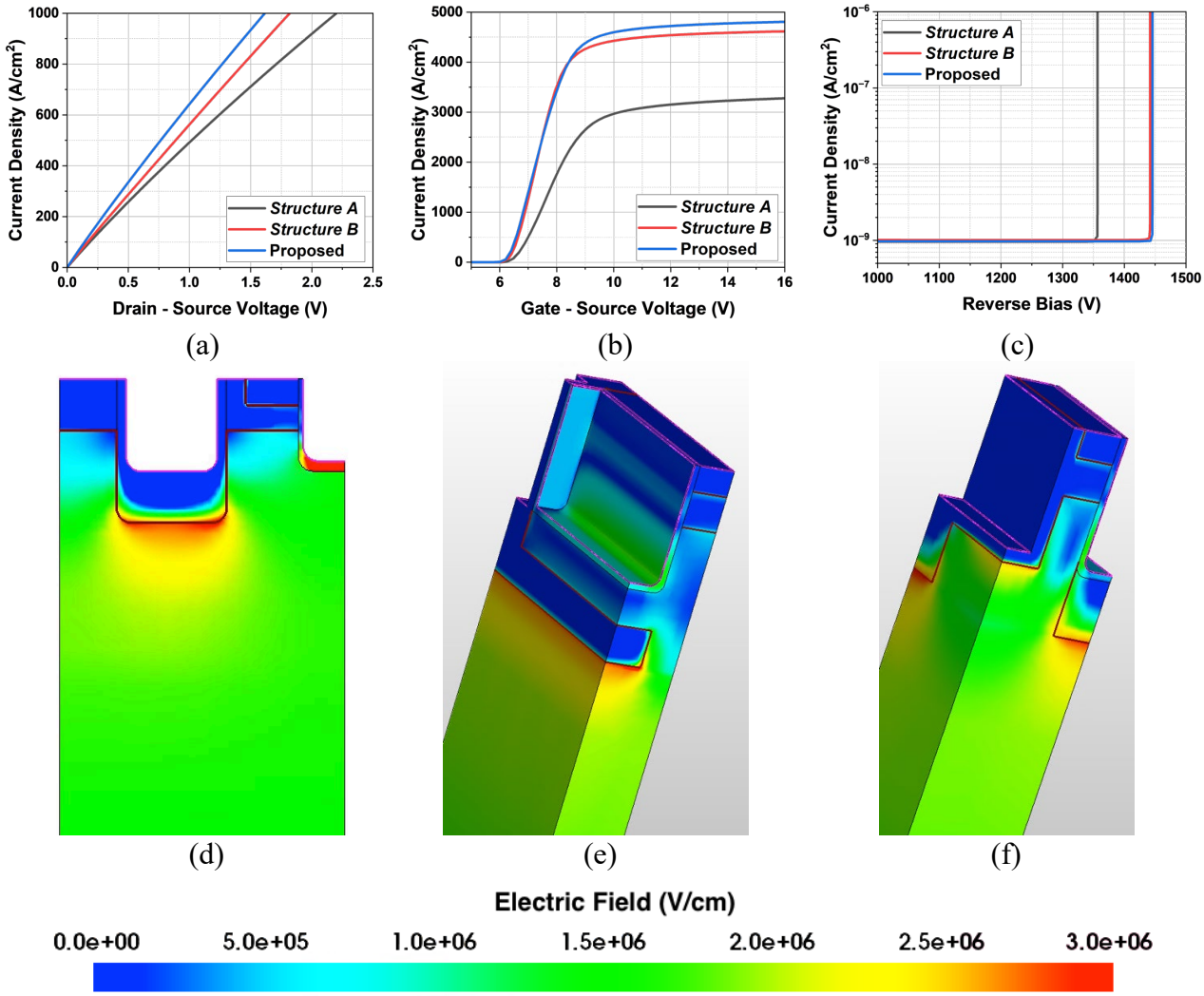


Fig. 2. (a) On-State curves, (b) Transfer characteristics, (c) Off-State curves; Electric Field @ 1.2 kV: (d) *Structure A*, (e) *Structure B* and (f) Proposed MOSFET.

The EF distribution at 1.2 kV can be seen in Fig. 2 (d-f). The maximum EF in the gate oxide for *structure A* is 4.2 MV/cm, *structure B* is 1.8 MV/cm and the proposed MOSFET is 2.1 MV/cm. The EF in the oxide below 3 MV/cm was achieved by selecting the CSL/N-buried layer doping of $1x10^{17}$ cm^{-3} and $2x10^{17}$ cm^{-3} in the *structure B* and $3x10^{17}$ /$2x10^{17}$ cm^{-3} in the proposed MOSFET, respectively. Based on Fig. 2 (a), at 300 A/cm^2: *structure A* R_{on} is 1.96 mΩ/cm^2, *structure B* R_{on} is 1.74 mΩ/cm^2 and our structure's R_{on} is 1.48 mΩ/cm^2. The threshold voltage, as shown in the Fig. 2 (b) is approximately 6.5 V of all three devices. In the off state, both the *structure B* and the proposed structures manage to block 100 V more than the benchmark device with the proposed device achieving over 1400 V blocking voltage.

To summarise, the proposed trench MOSFET design outperforms its competitors, showing the lowest on-state resistance of the entire investigation of 1.48 mΩ/cm^2, which is a reduction of 25 % and 15 % compared to double trench MOSFET and *Structure B*. It also maintains excellent blocking voltage capability, with a breakdown of 1445 V.

Short-Circuit Comparison

The Short-Circuit conditions were simulated at 800 V drain-source and gate resistance of 10 Ω, with the following parasitic components: drain (R_D) and source (R_S) resistance of 1 mΩ; drain (L_D) and source (L_E) inductance of 1 nH. Parasitic components and simulation parameters were calibrated

to result in SC failure of the benchmark device i.e. *structure A* about 7 µs from experimental results in [3]. Lattice temperature reaches 2000 K at this point. Drain current and maximum lattice temperature is recorded in Fig. 3:

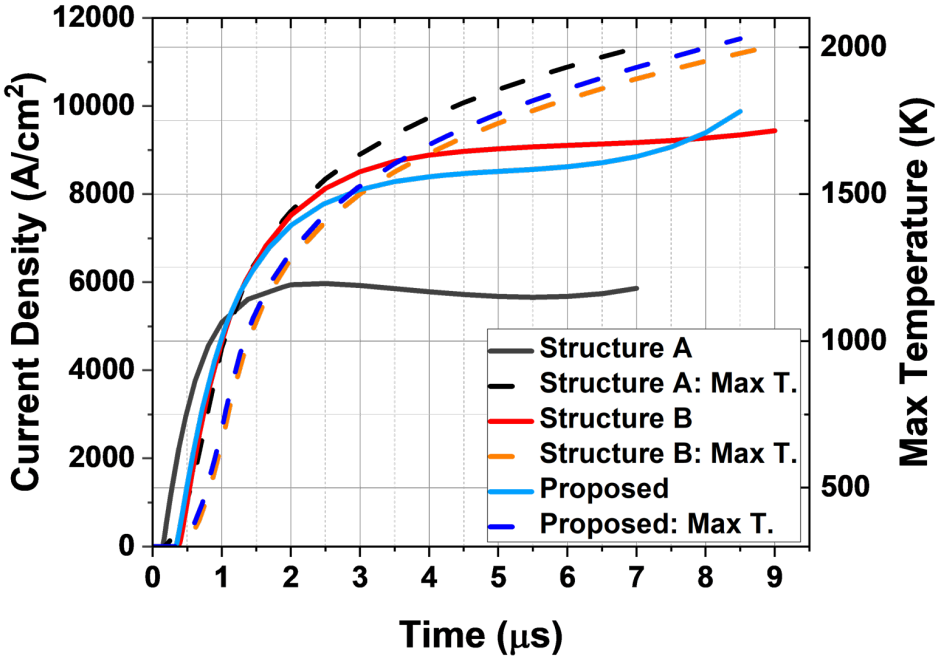


Fig. 3. SC current density (Y-left) and Maximum lattice Temperature (Y-right) vs SC Time.

In Fig. 3, the temperature of 2000 K is reached after 7.0 µs for the *Structure A*, 9 µs for the *Structure B* and 8.5 µs for the proposed structure. To confirm the SC failure mechanism, simulations were performed with and without the influence of the impact ionization. These are not shown in this paper. Results remained the same and there was no significant change in the drain current. This means that the failure of the devices is independent of the temperature and due to a very high current density due to parasitic BJT latch-up [9]. The layout with p-buried layers protects the gate oxide region by pushing the EF below the trench. This feature, combined with high current density, localizes the hot-spot below the trench and prolongs the SC withstand time.

To summarise, the SC performance of the proposed structure is superior to the double-trench MOSFET and comparable to *Structure B*. The following can be addressed by a further optimization of the CSL/n-buried layers and making those layers deeper into the bulk of the device.

Conclusion

Compared to Si IGBTs, SiC MOSFETs exhibit a much lower SC withstand time. Being a significant reliability concern in power applications, where the SC withstand time must be above 10 µs. We investigated static and dynamic characteristics of the double trench, commercially patented MOSFET and the novel MOSFET structure, using 3D TCAD simulation. The advantage of our proposed structure: is a possible reduction in fabrication steps, compared to the Structure B; improvement in the on-state performance by 25 % and 15 % compared to double trench MOSFET and *Structure B*, respectively; blocking voltage improvement by 100 V and SC performance compared to the double trench MOSFET. Furthermore, the on-state performance of our device can be further improved through the introduction of additional active trenches. This is in contrast to the performance of the *Structure B*, which is limited by the minimum opening of the p-trench incorporated between gates.

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