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Metal Contact Processing Experiments Towards Realizing 500°C Durable RF 4H-SiC BJTs

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Abstract. This paper presents results from metal contact processing experiments towards the implementation of durable 500 ºC high-frequency 4H-SiC bipolar junction transistors (BJTs). Specifically, *p*-type ohmic contacts have been demonstrated on a 0.25 µm-thick *p*-type homoepitaxial layer of doping 8 x 10^{18} ± 4 x 10^{18} cm^{-3}. Finally, preliminary current-voltage characteristics of fabricated BJTs are presented.

Introduction

The 60-day mission concept for Venus exploration, the Long-Lived (or Long-Life) In-Situ Solar System Explorer (LLISSE), requires the gathering and periodic wireless transmission of surface meteorological data to an orbiter [1]. Towards enabling such a mission, 4H-SiC integrated circuits (ICs) fabricated by NASA Glenn Research Center based on junction field effect transistors and resistors (JFET-R) have demonstrated operation for 60 days directly exposed to Venus surface atmospheric conditions [2] and 500 °C for more than a year in air ambient [3]. However, this transistor topology is unable to meet the ~100 MHz radio frequency (RF) power amplifier metric necessary for propagation and transmission of signals through the Venus atmosphere. A parallel development process is therefore underway at NASA Glenn to realize a similarly Venus (500 °C) durable higher frequency SiC RF BJTs as the signal gain devices for a 100 MHz transmitter. While this SiC BJT can leverage most of the 500 °C durable technical foundations of the SiC JFET, far lower parasitic series resistances are required from the metals/contacts, especially including low-resistance *p*-type base contacts for the *npn* BJT. This paper presents results from metal contact process development.

Experimental

***p*-type contact:** The development focus was on the *npn* rather than the *pnp* BJT to leverage the higher electron mobility. Circular Transfer Length Method (CTLM) structures were used to evaluate the contacts. The starting substrate (a single wafer was the source of all the test samples) was a 100 mm 4H-SiC *n*-type wafer with a 0.5 µm-thick *n*-type buffer layer of doping 1 x 10^{18} cm^{-3} followed by a 0.25 µm-thick *p*-type homoepitaxial layer of doping 8 x 10^{18} ± 4 x 10^{18} cm^{-3}. Based on literature [4,5] and prior unpublished data, all experiments were conducted with Al/Ti/Al (5 nm/10 nm/10 nm) that was deposited in a multi-source ultra-high vacuum E-beam evaporation system without breaking vacuum between layers. The experiments focused on evaluating the annealing process: furnace annealing versus rapid thermal annealing (RTA) over a range of temperatures. Furnace anneals were performed at 820 ºC, 850 ºC, 900 ºC and 950 ºC for 30 min. in a forming gas atmosphere (2% Hydrogen in Argon) at a flow rate of 3.6 slm during ramp up and anneal steps. Load temperature was 150 ºC and temperature ramp rate was ~15.5 ºC/min. RTA was performed at 750 ºC, 800 ºC, 850 ºC, 900 ºC and 950 ºC for 30 sec. in vacuum < 3 µTorr. The anneals were followed by electrical probe

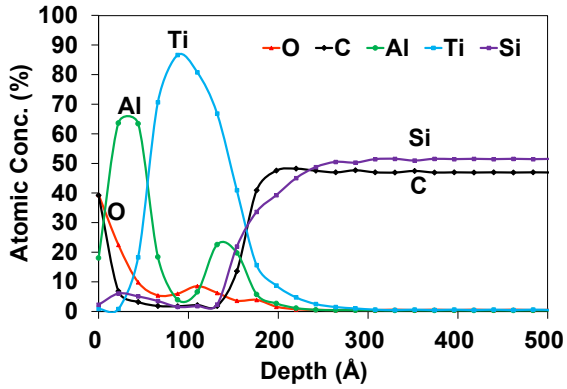

Fig. 1 Auger depth profile of sample with as-deposited Al/Ti/Al.

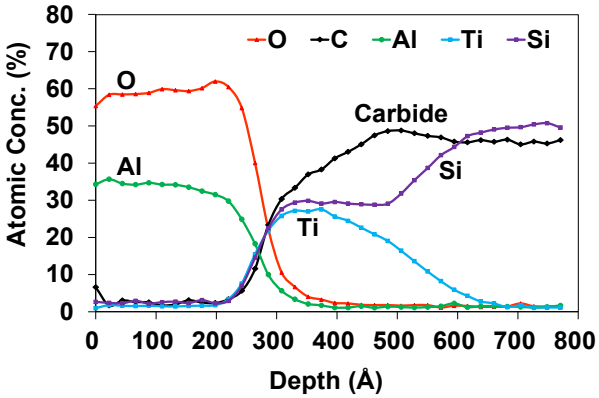

Fig. 2. Auger depth profile of contact following 820 °C forming gas furnace anneal.

measurements (I-V sweeps with a curve trace) and materials analyses (Auger depth profiling). Figure 1 shows the Auger analyses and depth profile of the as-deposited metal stack. Figure 2 shows the depth profile of the sample furnace annealed at 820 °C for 30 min. Post anneal, Fig. 2 indicates the aluminum forms a thick oxide layer on top of a $Ti_xSi_yC_z$ layer which could affect measured electrical properties. This oxide layer also prevents any carbon or titanium from reaching the surface. Figure 3 shows the CTLM structure used for all measurements (inset) and I-V measurements of similar rectifying characteristics for the samples furnace annealed at 820 °C, 850 °C, 900 °C and 950 °C.

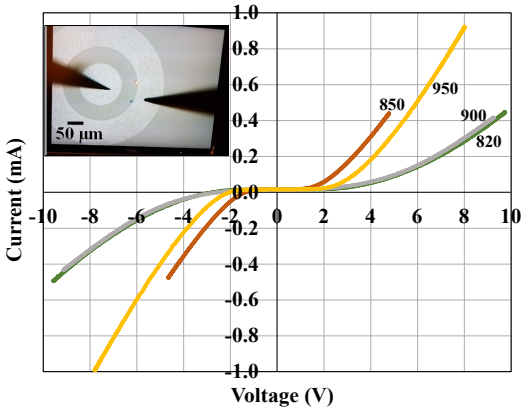

Fig. 3. CTLM structure being probed (inset) and measured I-V characteristics for different furnace anneal temperatures in °C.

Figures 4 through 7 show Auger depth profiles of RTA samples. At 750°C the aluminum coalesces towards the surface and oxidizes. The silicon and carbon from SiC begin to react to form both silicide and carbide with the titanium layer. Not all the titanium is reacted. At 800°C, there is an aluminum oxide layer at the surface. The titanium is fully reacted with the carbon and silicon, forming a $Ti_xSi_yC_z$ compound. At 850°C, the reacted products are very similar to the 800°C sample, except that the carbon has reached the surface, along with a small amount of titanium and silicon. The carbon is in a metal carbide oxidation state. The $Ti_xSi_yC_z$ layer is again formed. At 900 °C, even more of the carbon and titanium are found at the surface. The composition of the reacted inner film has changed in that there is much less silicide present in the $Ti_xSi_yC_z$ compound formed. Oxygen from the surface is also

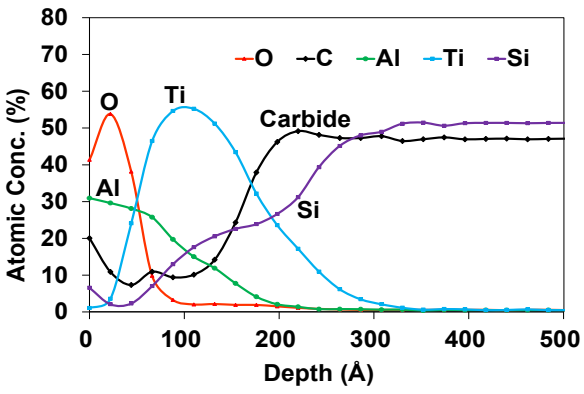

Fig. 4. Auger depth profile of contact following 750 °C RTA.

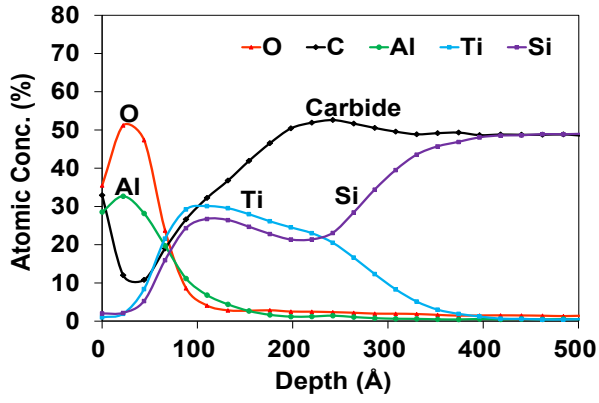

Fig. 5. Auger depth profile of contact following 800 °C RTA.

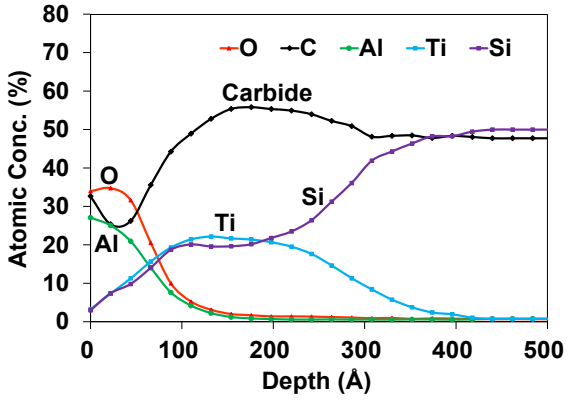

Fig. 6. Auger depth profile of contact following 850 ºC RTA.

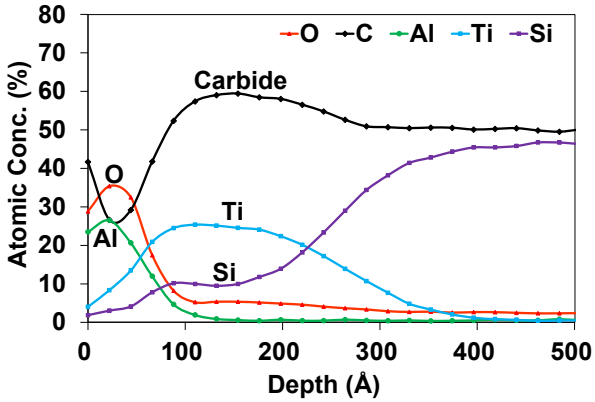

Fig. 7. Auger depth profile of contact following 900 ºC RTA.

beginning to migrate into the contact. Figure 8 plots comparative circular contact I-V results for RTA samples annealed from 750 °C to 950 °C. The I-V sweep transitions to linearity when increasing anneal temperature reaches 850 °C. This is consistent with the materials analysis that shows the titanium is fully reacted with the carbon and silicon forming the preferred $Ti_xSi_yC_z$ compound [5,6,7].

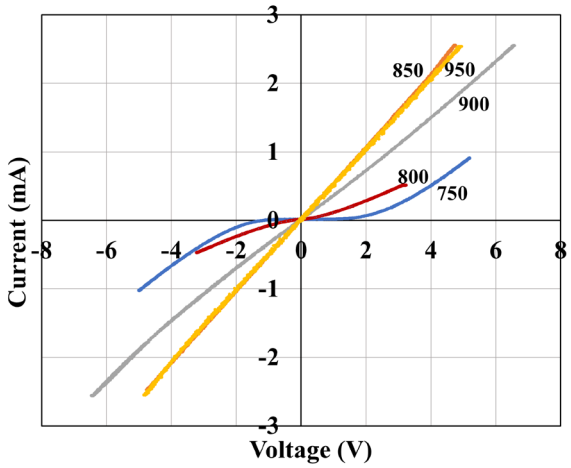

Fig. 8. I-V characteristics for different RTA temperatures in ºC.

Table 1 lists the rms roughness measured by AFM of two locations, the metal contact, and the 4H-SiC surface immediately next to the contact, of the same samples analyzed by Auger (before anneal, 820 °C forming gas anneal, 750 °C RTA, 800 °C RTA, 850 °C RTA and 900 °C RTA). Figures 9a and 9b show images from the AFM scan of the SiC and as-deposited metal (before anneal). Figures 10a and 10b show AFM images of the SiC and metal annealed at 850 °C. The major contribution to the roughness is from step bunching of the epitaxial layer with some contribution from metal roughening following the anneal.

Table 1. AFM roughness measurements of two locations, the metal contact, and the 4H-SiC surface immediately next to the contact, of the same samples analyzed by Auger.

Roughness (Rq)	Before anneal (nm)	820 °C forming gas (nm)	750 °C RTA (nm)	800 °C RTA (nm)	850 °C RTA (nm)	900 °C RTA (nm)
4H-SiC surface	2.55	3.02	3.91	2.98	2.54	2.99
Metal contact	3.27	4.37	4.17	3.69	4.39	3.58

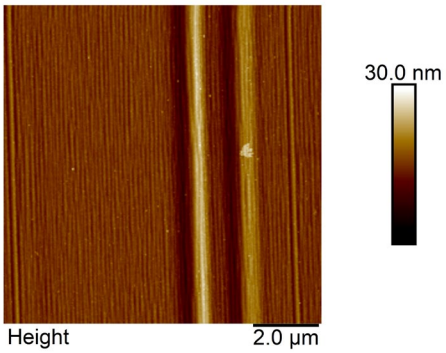

Fig. 9a. AFM scan of 4H-SiC surface next to as-deposited Al/Ti/Al.

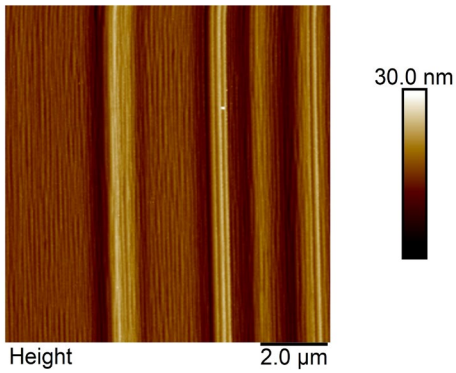

Fig. 9b. AFM scan of as-deposited Al/Ti/Al.

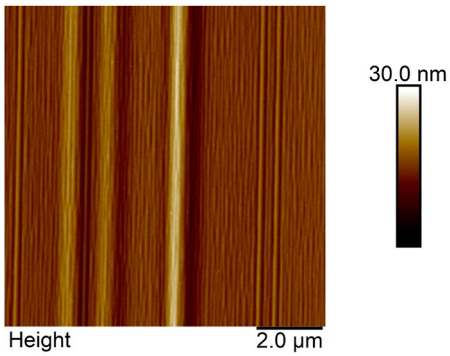

Fig. 10a. AFM scan of 4H-SiC surface following 850 ºC RTA.

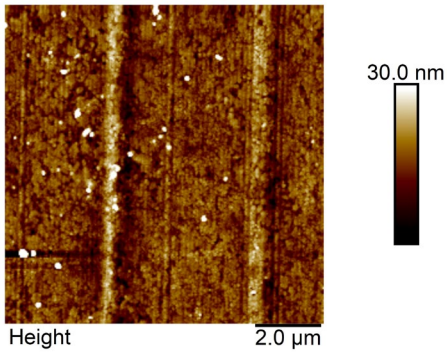

Fig. 10b. AFM scan of Al/Ti/Al following 850 ºC RTA.

The 850 °C RTA anneal had the lowest thermal budget that also met the electrical and materials analysis criteria and was chosen as the preferred process.

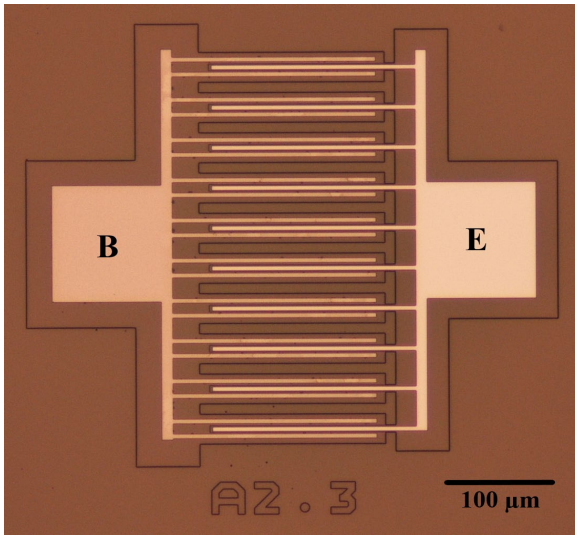

Fig. 11. Optical micrograph of a partially fabricated BJT; E, emitter; B, base (bottom contact, not yet metallized is the collector).

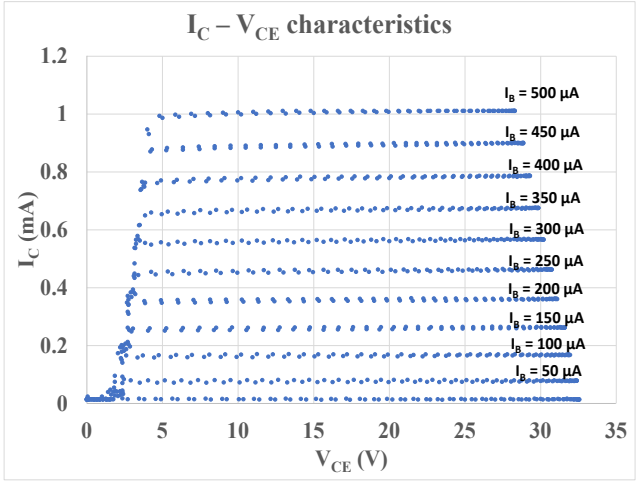

Fig. 12. I-V characteristics of a fabricated BJT at room temperature.

BJT characteristics: Figure 11 depicts an optical micrograph of a partially fabricated BJT design with interdigitated fingers. The BJT measured at this step incorporates the annealed *p*-type contact and the unannealed *n*-type contact. No thick conductive metal over the metal contacts has been deposited and patterned to crucially minimize base-emitter resistance. Figure 10 is a plot of the I-V characteristic. The low current gain is in part attributed to rectifying n-type emitter contacts which have not yet been annealed and the absence of back-side collector contacts (to be deposited during final processing steps).

Conclusion

A *p*-type contact process, without the use of ion implantation to reduce contact resistance, towards the realization of a Venus-durable BJT was successfully developed. Preliminary room-temperature I-V measurements of partially fabricated BJTs show promise. Further processing to complete SiC BJT fabrication by (1) adding thick conductive fingers on top of thin ohmic contact fingers, (2) adding robust wire bonding metal, and (3) annealing n-type contacts is on-going. Future tests will include RF performance validation (gain and frequency response) versus temperature and long-duration demonstration in Venus surface environmental conditions.

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