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Comparative Study of the Self-Aligned Channel Processes for 4H-SiC VDMOSFET

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Abstract. In this study, a novel self-aligned process is proposed to reduce the specific channel resistance, and the electrical characteristics affected by process variation are also verified through TCAD simulation. Also, when compared to other self-aligned processes, the process introduced in this paper offers the advantages of stable electrical characteristics and lower process costs.

Introduction

For high power devices, silicon carbide (SiC) is a promising material due to its superior properties [1, 2]. Compared with silicon (Si), SiC has a wider band-gap and higher critical electric field, which makes SiC devices have higher breakdown voltage than Si-based devices with the same doping concentration. In other words, SiC devices can significantly reduce power loss because of the lower on-resistance resulting from the thinner epi-layer thickness and higher doping concentration when operated at the same voltage rating.

Specific on-resistance ($R_{on,sp}$) is one of the most important specifications of power MOSFETs. Unfortunately, the poor interface between silicon dioxide and 4H-SiC leads to the higher interface trap density and much lower channel mobility, especially in the power MOSFETs with inversion mode channels [3]. As a result, among the components contributing to the total $R_{on,sp}$, specific channel resistance ($R_{ch,sp}$) plays a significant role in low and medium voltage-rated SiC power MOSFETs [4]. To reduce the $R_{ch,sp}$, in addition to enhancing the channel electron mobility, shortening the channel length is also an effective method. Over the past decade, several self-aligned processes have been proposed to achieve shorter and more symmetric channels in vertical double-implanted MOSFETs (VDMOSFETs) [5-8]. In this study, we introduce a new self-aligned channel (SAC) process and conduct a comparative analysis on the performance variation of VDMOSFETs fabricated with different SAC processes.

Experiment

There are three SAC processes evaluated by using Sentaurus TCAD. They are the p-base ion implantation before poly-Si hard mask oxidation (SAC-1) process [5, 6], the poly-Si spacer (SAC-2) process [7], and the p-base ion implantation after poly-Si hard mask oxidation (SAC-3) process. The main process steps are depicted in Fig. 1. In the SAC-1 process, the channel length is controlled by the volume expansion of the oxidation of the poly-Si hard mask, which is roughly twice the oxidation thickness. In the SAC-2 process, the channel length is controlled by the poly-Si spacer length. In the SAC-3 process, the channel length is directly determined by the oxidation thickness of the poly-Si hard mask, meaning that the channel length is nearly equal to the oxidation thickness.

Assuming the variation of ion implantation is ignored, the channel length deviations (δL_{ch}) of SAC-1 and SAC-3 are attributed only to the oxidation deviation, while the δL_{ch} of SAC-2 consists of poly-Si thickness and spacer etching deviations. In a typical sub-μm process technology, the three standard deviations of oxidation, low pressure chemical vapor deposition (LPCVD), and spacer

etching processes are 5%, 7%, and 7%, respectively. Therefore, based on the process conditions illustrated in Fig. 1, the δL_{ch} of SAC-1, SAC-2, and SAC-3 processes are 5%, 10%, and 5%. This implies that with L_{ch} being 0.5 μm, the target values for δL_{ch} are 25 nm, 50 nm, and 25 nm, respectively. Additionally, Table 1 lists the device parameters used in TCAD simulation.

Table 1. Common device parameters used in the simulation of device performance with different self-aligned channel processes.

Drift Layer	P-base	N^+-source	JFET	Gate oxide thickness	Channel length	Channel electron mobility	Cell pitch
$5.3x10^{15}$ cm^{-3} 15 μm	$1.83x10^{18}$ cm^{-3} Depth 1.1 μm	$1x10^{20}$ cm^{-3} Depth 0.4 μm	$1.56x10^{17}$ cm^{-3} Width 2.0 μm	50 nm	0.5 μm	20 cm^2/V-sec	7.4 μm

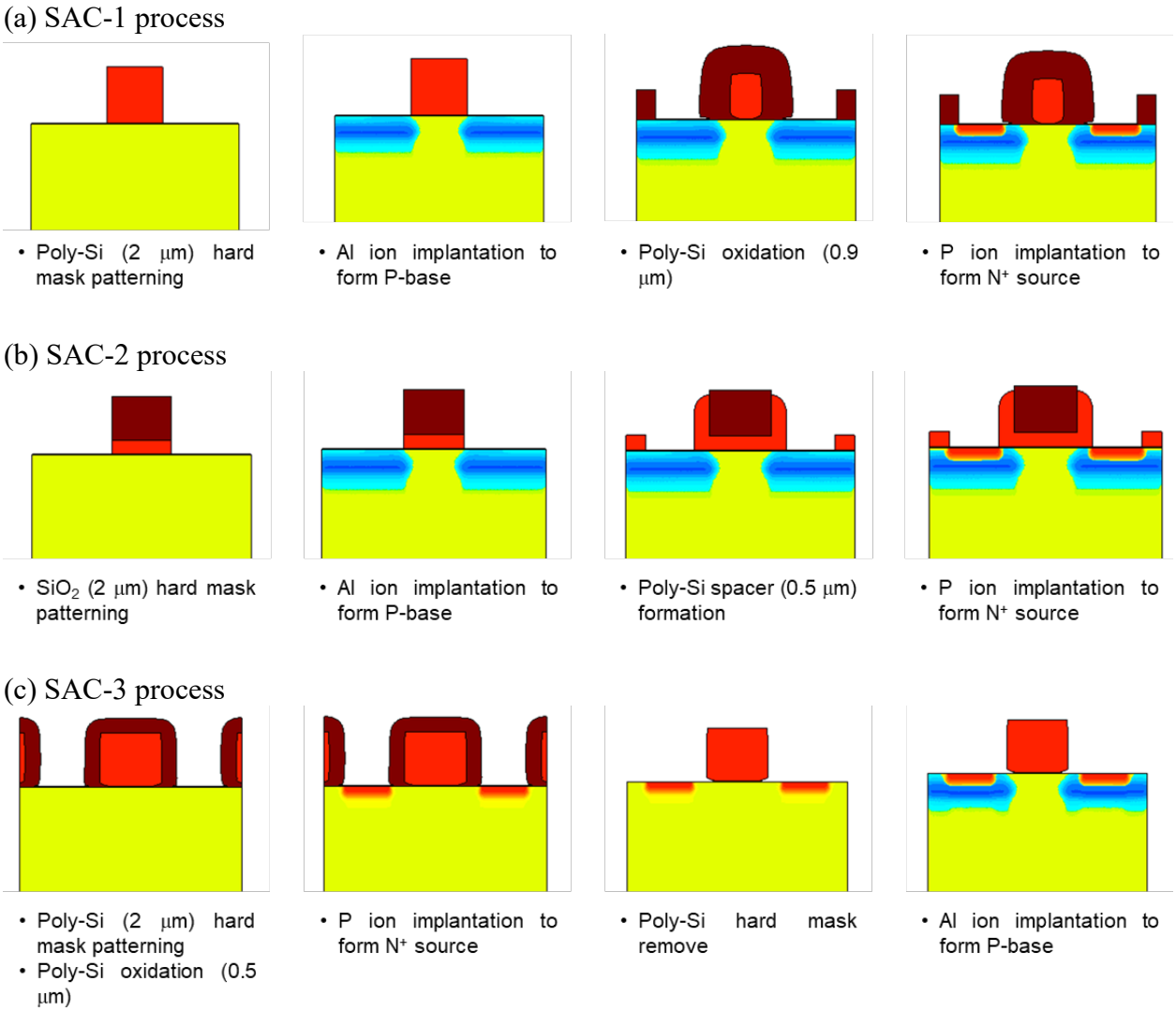

Fig. 1. Process flow of (a) p-base ion implantation before poly-Si hard mask oxidation (SAC-1) process [5, 6], (b) poly-Si spacer (SAC-2) process [7], and (c) p-base ion implantation after poly-Si hard mask oxidation (SAC-3) process.

Results and Discussion

Fig. 2 shows the net carrier profiles across the channel region of the SAC-1 VDMOSFET. Due to the lateral straggling of the p-base ion implantation, the carrier concentration is not uniform in the channel region. Thus, the threshold voltage (V_{th}) increases as L_{ch} increases as shown in Fig. 3. The output characteristics, as displayed in Figure 4, indicate that $R_{on,sp}$ also increases with the increasing L_{ch}. On the other hand, Fig. 5 illustrates that the blocking characteristic does not degrade as L_{ch} decreases. In Figures 6, 7, and 8, we present the transfer, output, and blocking characteristics of the SAC-2 VDMOSFET, respectively. Similar to the SAC-1 VDMOSFET, Figures 6 and 7 reveal that L_{ch} has a positive correlation with both V_{th} and $R_{on,sp}$. However, in Figure 8, early breakdown happens due to the channel punch-through as L_{ch} decreases to 0.45 μm.

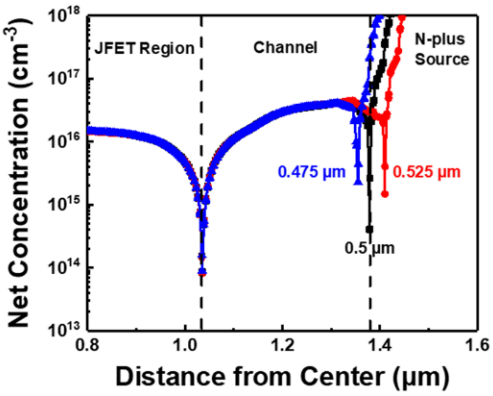

Fig. 2. Net carrier profiles across the channel region of the SAC-1 VDMOSFET.

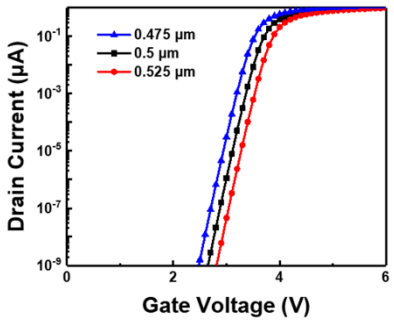

Fig. 3. Transfer characteristics of the SAC-1 VDMOSFET.

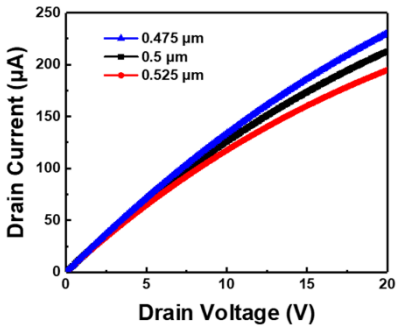

Fig. 4. Output characteristics of the SAC-1 VDMOSFET.

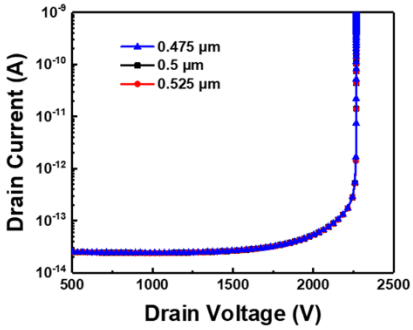

Fig. 5. Blocking characteristics of the SAC-1 VDMOSFET.

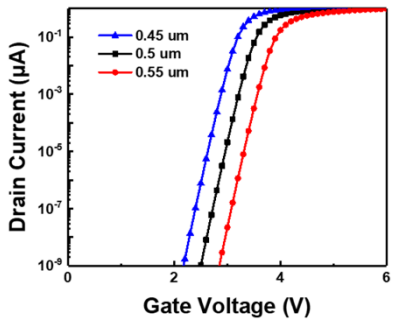

Fig. 6. Transfer characteristics of the SAC-2 VDMOSFET.

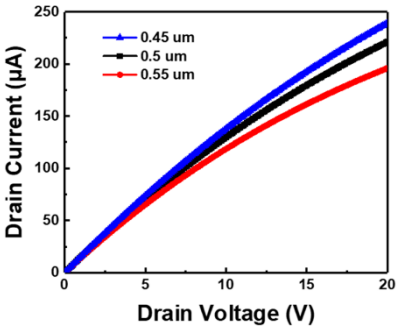

Fig. 7. Output characteristics of the SAC-2 VDMOSFET.

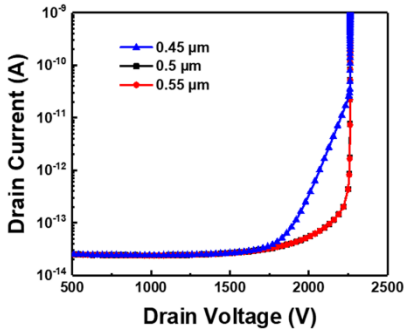

Fig. 8. Blocking characteristics of the SAC-2 VDMOSFET.

Figs. 9, 10, and 11 show the transfer, output, and blocking characteristics, respectively, of the SAC-3 VDMOSFET. It can be observed that both V_{th} and $R_{on,sp}$ also exhibit positive correlations with L_{ch}. Furthermore, regarding the off-state characteristics, even as L_{ch} decrease, the blocking voltage does not degrade significantly. In figs. 12 and 13, the deviations of V_{th} and $R_{on,sp}$ are compared respectively, for the three SAC VDMOSFETs. Since the δL_{ch} of the SAC-1 and SAC-3 processes is

smaller than that of the SAC-2 process, the deviation in device performance is also smaller. Moreover, to obtain the same L_{ch}, the sidewall oxidation thickness of the SAC-1 process is 1.8 times that of the SAC-3 process. As a result, it is worth noting that the SAC-3 process will have the advantages of shorter oxidation time, less SiC consumption, and improvement of throughput.

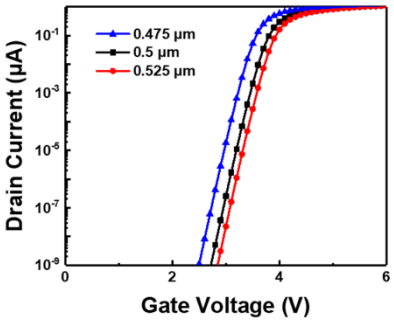

Fig. 9. Transfer characteristics of the SAC-3 VDMOSFET.

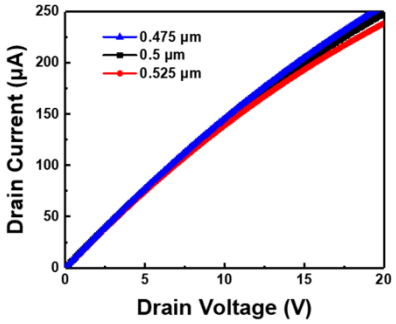

Fig. 10. Output characteristics of the SAC-3 VDMOSFET.

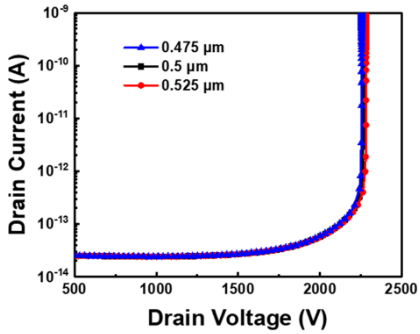

Fig. 11. Blocking characteristics of the SAC-3 VDMOSFET.

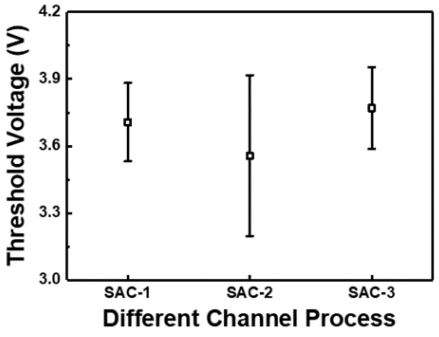

Fig. 12. The threshold voltage (V_{th}) distribution of the VDMOSFET fabrication with the SAC-1, SAC-2, and SAC-3 processes.

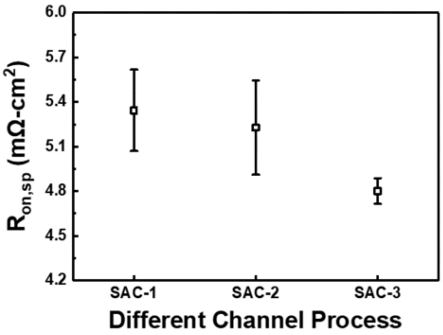

Fig. 13. The specific on-resistance ($R_{on,sp}$) of the VDMOSFET fabrication with the SAC-1, SAC-2, and SAC-3 processes.

Summary

In summary, a new process (SAC-3) to achieve lower on-resistance is proposed in this study. What's more, the three SAC processes are evaluated from the perspectives of device deviation and process cost. When compared to the other two SAC processes, the SAC-3 process offers numerous advantages, such as stable electrical characteristics and reduced oxidation time, among others. Even in the presence of process variations, VDMOSFETs utilizing the SAC-3 process can still operate reliably without early breakdown. Consequently, it is suggested that the SAC-3 process is a better choice to reduce the L_{ch} to the extreme.

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