

Demonstration of Low Interface Trap Density ($\sim 3 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$) SiC/SiO₂ MOS Capacitor with Excellent Performance Using H₂+NO POA Treatment for SiC Power Devices

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Abstract: In this work, we report on the engineering of the SiC/SiO₂ MOS interface using H₂ treatments along with NO POA to improve the interface characteristics and device reliability. Significantly low D_{it} of $3 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$, stable threshold voltage, and long gate oxide lifetime $> 10^5 \text{s}$ have been achieved by H₂ annealing before NO POA of thermal SiO₂. Through device electrical characterization and material analysis, we show that the performance enhancement is due to the reduction of interface defects and trapped charges in the SiO₂ surface layer after the POA treatment, which in turn, significantly suppresses the threshold voltage instability.

Introduction

While silicon carbide (SiC) power MOSFETs are commercially available, the on-resistance of a medium-class ($\sim 1 \text{kV}$) MOSFET continues to be much higher than expected based on the physical properties of bulk SiC, due to low channel mobility [1,2]. This is attributable to the high interface state density (D_{it}) in the SiC/SiO₂ structure [2,3]. Although the exact cause for the high D_{it} has yet to be identified, the carbon atoms remaining at the interface are generally considered to be plausible culprits. Currently, post-oxidation annealing (POA) in NO gas ambient is a standard process to reduce D_{it} and improve channel mobility of SiC MOSFETs [4,5]. This process results in nitrogen incorporation on the SiC side of the interface, which is thought to play a key role in improving channel mobility [6]. However, the nitrogen incorporation is also reported to degrade reliability metrics such as threshold voltage stability for the SiC MOS devices [7].

In this work, we report on the engineering of the SiC/SiO₂ interface using different oxidation and post oxidation annealing (POA) treatments to improve the SiC/SiO₂ MOS interface. C-V results show that the interface trap density (D_{it}) was significantly reduced to $3 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$.

Results and Discussion

SiC/SiO₂ MOS capacitors were fabricated on a highly doped n-type 4° off-cut (0001) 4H-SiC wafer, with a 10 μm thick nitrogen doped homo-epilayer. Key aspects of the process flow are illustrated in Fig. 1. The samples were subjected to thermal oxidation, POA, and H₂ treatments in various sequences. Thermal oxidation was done at 1350 °C in O₂ ambient for 18 min to grow 50 nm thick SiO₂ layers, while POA was performed at 1300 °C in NO and H₂ gases for 30 min. The sample conditions are designated as follows, henceforth: oxidation (As-Ox), oxidation+NO POA (ONO), H₂ treatment+oxidation+NO POA (HONO) and oxidation+H₂ treatment+NO POA (OHNO).

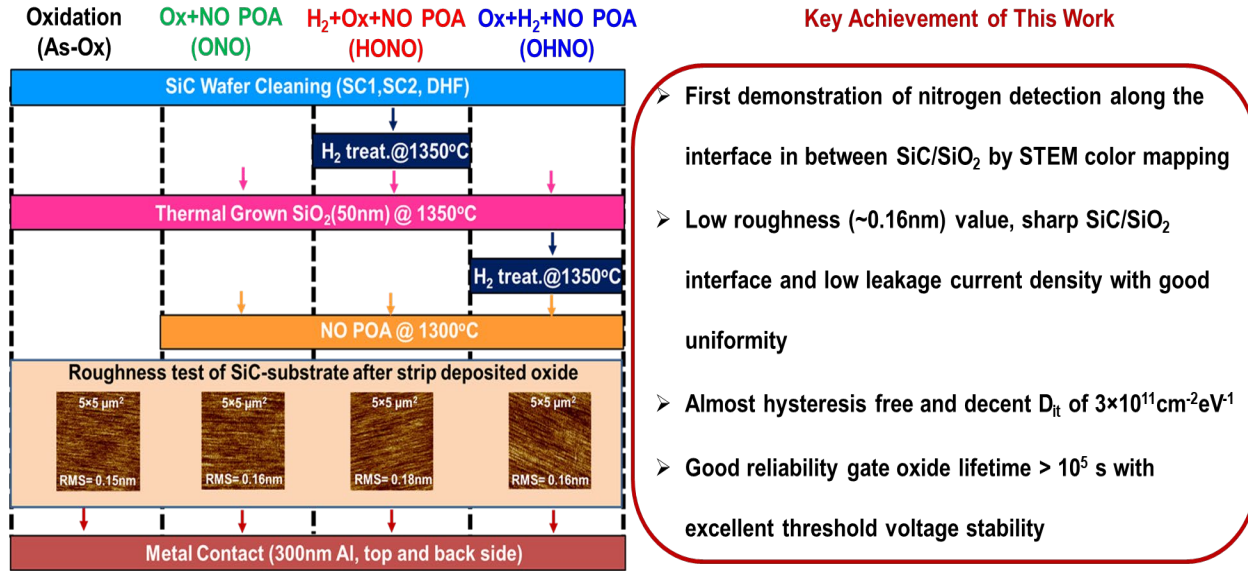


Fig. 1 Fabrication process flow for the SiC/SiO₂ MOS capacitors, AFM maps for SiC substrate after stripping the thermal SiO₂, and key achievements of this work.

Atomic force microscopy (AFM) characterization was carried out to investigate the superficial morphology of the SiC substrate after stripping the thermal SiO₂. The calculated root mean square roughness is slightly higher (~0.18 nm) for the HONO sample as compared to the fresh SiC and other samples, indicating that H₂ annealing may not be fully optimized, thus causing sizable atomic migration. In addition, high-resolution transmission electron microscopy (HRTEM) images were acquired for all the samples to examine the existence of additional layers at the SiC/SiO₂ interface after POA (Fig 2(a)). A mildly blurred interface can be seen in as-Ox devices as compared to the sharper interface observed for other devices, implying that the POA treatment process has improved the SiC/SiO₂ interface. However, terrace height growth or step bunching at the SiC surface is observed pre-H₂ treatment due to the higher surface energy of the edges as compared to the terrace [8]. Furthermore, scanning transmission electron microscopy (STEM-EDX) color elemental mapping profiles of the samples have been acquired, which support the existence of a slightly nitrogen-rich layer at the SiC/SiO₂ interface (Fig. 2(b)) after POA.

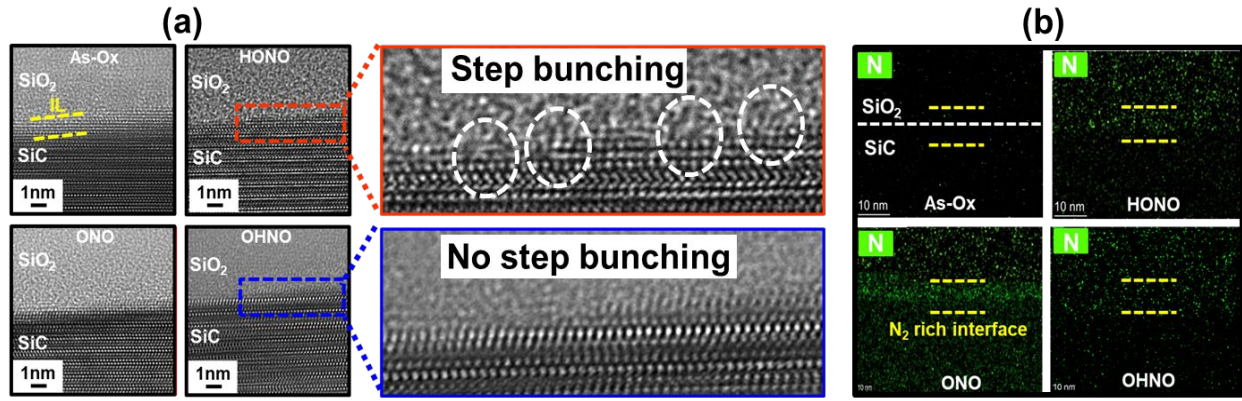


Fig. 2 (a) Cross-sectional TEM of the SiC/SiO₂ interface for all the samples and (b) STEM-EDX elemental mapping confirming the presence of elemental N at the interface in all the samples.

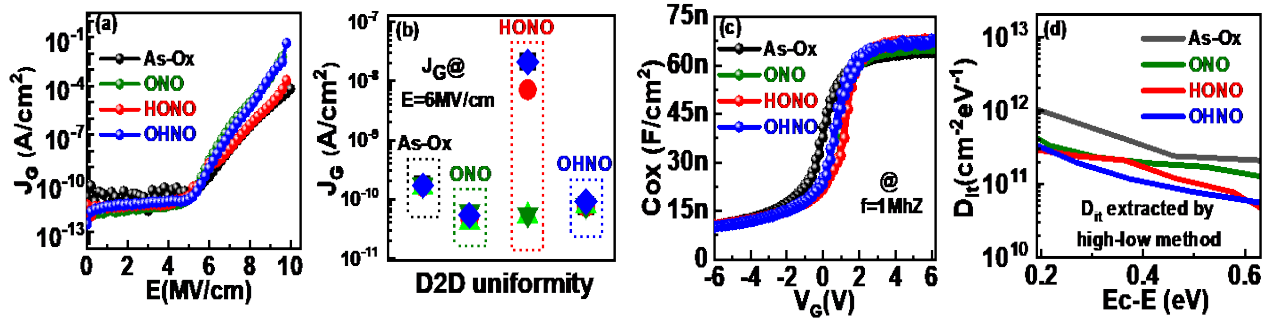


Fig. 3 (a) J_G - V_G for the SiC/SiO₂ MOS capacitors (b) Distribution of gate leakage density for randomly selected devices (c) Typical C_{ox} - V_G double sweep curves of the SiC/SiO₂ MOS capacitors and (d) D_{it} extracted by the high-low method for the SiC/SiO₂ MOS capacitors[2].

Fig 3(a), which shows the gate leakage current density (J_G) plotted as a function of V_G , may be used to interpret the SiO₂ gate dielectric film quality. The J_G value of 10^{-10} A/cm² for the whole range of applied electric field up to 6 MV/cm for 50 nm SiO₂ suggests superior SiO₂ gate dielectric film quality. The HONO device, however, shows a wider distribution of the gate leakage density compared to the other device types (Fig. 3(b)), which may be attributed to the non-uniform SiO₂/SiC interface observed in the TEM image.

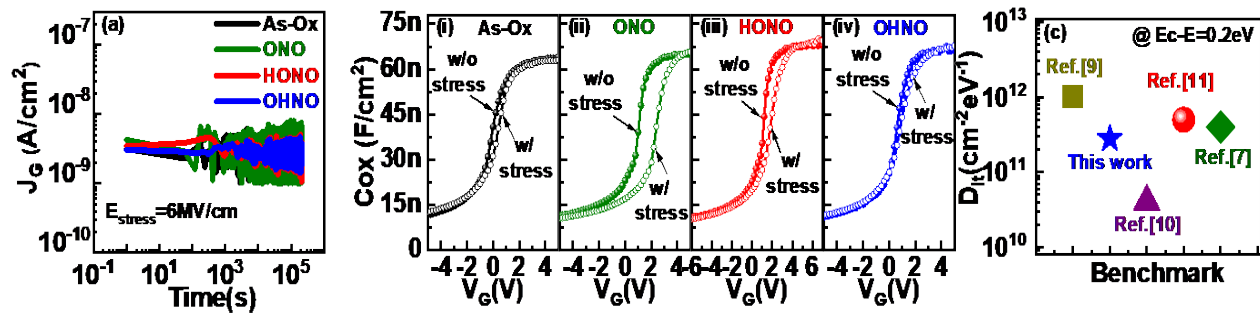


Fig. 4 (a) Time to breakdown for the SiO₂/SiC MOS capacitors at a forward stress of 6 MV/cm at room temperature (b) Effect of stress on C_{ox} - V_G curve shift for the SiC/SiO₂ MOS capacitors. The results before and after stress are compared and (c) Benchmark plot for D_{it} showing satisfactory D_{it} .

Next, capacitance-voltage (C-V) data were acquired under forward and reverse gate bias sweeps to investigate the effect of POA on the SiC/SiO₂ interface (Fig. 3(c)). All the devices exhibit very small clockwise hysteresis indicating low trap count at the SiC/SiO₂ interface. The POA process is found to be effective in reducing D_{it} to $3 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ (Fig. 3(d)). Besides removing the carbon defects, the incorporation of hydrogen along with nitrogen may have passivated the dangling bonds at the SiC/SiO₂ interface leading to low D_{it} . Further, Fig 4(a) shows the gate oxide lifetime of the MOS capacitors studied by the constant voltage time-dependent dielectric breakdown (TDDB) test, which was conducted to assess the impact of POA treatment on device reliability. The gate oxide lifetime extrapolates to $>10^5 \text{ s}$ at a stress bias corresponding to the oxide field of +6 MV/cm at room temperature. Finally, we investigated the threshold voltage stability of the SiC/SiO₂ MOS capacitors by conducting a positive bias stress test. Here, a constant voltage stress corresponding to an oxide field of +6 MV/cm was applied up to 10^5 s (Fig. 4(b)). A slightly larger V_{FB} shift is seen for the ONO device as compared to the other devices after the stress test due to increased nitrogen at the interface. The improved threshold voltage stability for the H₂ treated devices could be a result of nitrogen removal from the SiO₂ side at the SiC/SiO₂ interface. Fig. 4(c) benchmarks the D_{it} of SiC/SiO₂ MOS capacitors obtained in this study with those of other reported SiC-based MOS capacitors. It is reasonable to conclude that the device with OHNO sequence in this study has achieved a satisfactory D_{it} value ($3 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$).

Conclusion

In this work, we have presented the effect of POA(H₂+NO) treatments on the interfacial characteristics and device reliability of SiC/SiO₂ MOS capacitors. Interestingly, it has been found that the SiC/SiO₂ interface is positively influenced by the combination of H₂+NO POA treatment of the SiO₂ layer and this is an effective method for improving the threshold voltage stability without deteriorating the interfacial properties. Satisfactory D_{it} , almost hysteresis-free CV behavior, and good reliability have been experimentally demonstrated.

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