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Demonstrating SiC *In Situ* Rounded Trench Processing Technologies for Future Power Trench MOSFET Applications

B. Jones[1,a *], A. Croot[2,b], J. Mitchell[2,c], C. Bolton[2,d], J. Evans[1,e], F. Monaghan[1,f], K. Riddell[2,g], M. Jennings[1,h], O. Guy[1,i] and H. Ashraf[2,j]

[1]Swansea University, Singleton Park, SA2 8PP, Swansea, UK

[2]KLA Corporation (SPTS Division), Ringland Way, NP18 2TA, Newport, UK

[a]828129@swansea.ac.uk, [b]alex.croot@kla.com, [c]jacob.mitchell@kla.com, [d]chris.bolton@kla.com, [e]j.e.evans@swansea.ac.uk, [f]909302@swansea.ac.uk, [g]kevin.riddell@kla.com, [h]m.r.jennings@swansea.ac.uk, [i]o.j.guy@swansea.ac.uk, [j]huma.ashraf@kla.com

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Abstract Effective control of device geometry is key to mitigating high localized electric fields in next-generation SiC power devices. Advanced trench processing allows for highly tunable trench-gate architectures in trench MOSFETs. By utilizing a two-step inductively coupled plasma reactive ion etch (ICP-RIE) process, a high degree of trench base corner rounding can be achieved, irrespective of trench opening corner geometry prior to post etch treatments. Sentaurus TCAD device modelling highlights the importance of effective electric field dispersion at the gate oxide using rounded trench corners, while *I-V* characterization of fabricated trench MOS-capacitor devices demonstrate the influence of trench base corner rounding on gate oxide breakdown.

Introduction

Next generation SiC power devices will utilize a trench MOSFET structure [1]. By incorporating a trench gate structure, the total on-resistance and efficiency of the device are improved [2]. SiC trenches, typically of widths >0.5μm and depths <3μm are etched using reactive ion etching (RIE). Eliminating rough sidewalls and micro trenches has been a topic of interest [3], however the control of trench corner profile has had comparatively fewer investigations. Sharp corners at the trench base result in sites of intense electric field crowding in operational SiC trench MOSFETs, causing premature gate dielectric breakdown [4]. Since the electric field in a given material is inversely proportional to the dielectric constant, the field in the gate oxide can be up to 3 times greater than in the SiC. As the maximum breakdown electric field in SiC is >3 MV/cm, the corresponding oxide electric field is also operating in the region of dielectric breakdown at ~ 9 MV/cm.

Previously, studies have reported using post-etch high temperature annealing in SiH_4/Ar and H_2 at >1500˚C to develop the rounded corner features in SiC trench structures [5, 6 & 7]. While this is a repeatable process, this method increases device fabrication time and inherently rounds both the top and base corners of the trench with comparable radii. It is desirable to have more rounding at the base of the trench compared to the trench opening for effective localized electric field dissipation. Excessive radii at the trench opening serves to increase cell pitch by shifting the area of the surface implantations away from the trench. Further, larger corner rounding radii requires longer annealing time, potentially increasing device fabrication cost. An industry-ready *in situ* rounded trench etch process developed by KLA reduces geometry-altering post-etch anneal requirements, while offering preferential trench base corner rounding. Building on previously presented modelling and etch process development work [8], a fully realized *in situ* SiC rounded trench etch has been implemented and used to fabricate trench MOS-capacitors. These devices have been used to show the influence of trench radius of curvature on gate oxide dielectric breakdown voltage.

Experimental

SiC trench etching was performed at KLA using an SPTS Synapse™ ICP-RIE tool, on epi-ready SiC substrates with a 2μm thick SiO_2 etch mask deposited using an SPTS plasma enhanced chemical vapor deposition (PECVD) tool. The round-based trenches were produced using a novel two step etch process [9]. Following an initial etch step to achieve most of the final depth, a subsequent passivation rich etch step was performed, which reduced the dimensions of the trench opening during processing. The passivation rich step resulted in a greater amount of material etched from the trench center, causing rounding of the trench base corners. Table 1 outlines the typical SiC rounded trench etch process parameter ranges.

Two sets of etched SiC samples were produced: the first with conventional square trench corners, and the second with rounded trench base corners. This resulted in 1296 devices; 50% of which had rounded architecture. Following trench processing, SiC trench MOS-capacitors were fabricated using an Al_2O_3 dielectric, deposited using an SPTS 300™ molecular vapor deposition (MVD) tool, selected for the high degree of film conformity. Nickel contacts deposited using a Kurt J Lesker 75™ physical vapor deposition (PVD) tool. *I-V* testing was performed on the trench MOS-capacitors to assess the effect of rounded corners vs. sharp corners on gate dielectric breakdown voltage, using a Keithley 2636B source meter, and an Everbeing C-2 probe station with a test sweep from 0-150V.

Table 1. Typical SiC rounded trench etch processing parameters ranges.

Parameter [Units]	*Step 1*		*Step 2*	
	Min	*Max*	*Min*	*Max*
Time [s]	50	200	45	125
Pressure [mTorr]	4	20	6	10
Source coil power [W]	900	2400	1200	1600
Platen power [W]	900	1500	180	800
O_2 flow [sccm]	15	50	12	130
H_2 flow [sccm]	0	30	0	0
Etch gas flow [sccm]	90	140	0	0
Passivation gas flow [sccm]	10	30	100	170

SiC Trench Gate MOSFET Corner Modelling

Synopsys Sentaurus TCAD was used to model the influence of trench corner rounding on trench MOSFET breakdown voltage. A trench MOSFET half-cell structure was modelled with a 4μm wide N-type drift region dopant concentration of $1x10^{16}$ cm^{-3}, corresponding to a parallel plane breakdown voltage of 3000V, shown in Fig. 1.

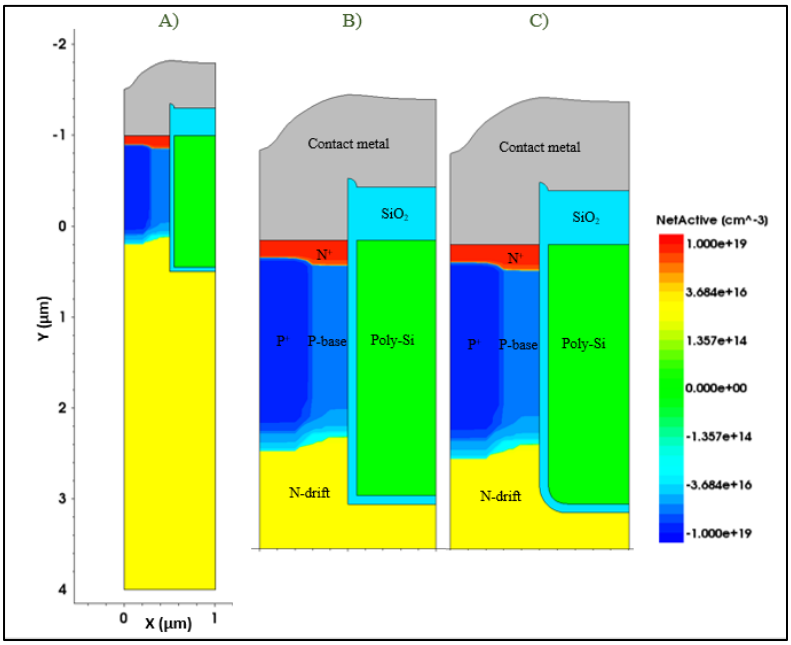

Fig 1. A) SiC trench gate MOSFET half-cell structure. Trench base corner radius variable – B) sharp corner, C) 250nm rounded corner.

The importance of effective electric field distribution is depicted in Fig. 2, which shows the trench gate MOSFET test structure oxide corner at a fixed reverse drain bias of 750 V. The acute localized high electric field present (Fig. 2 A) is typical of a sharp corner. The 50nm radius (Fig.2 B) is sufficient to spread the field, thus averting a high local field. By comparison, a 250nm radius of curvature eliminates any electric field above 5 MV/cm.

Gate oxide breakdown was simulated for varying trench corner radii of curvature, by ramping the blocking voltage until the electric field in the gate oxide reached a predetermined field magnitude (5 MV/cm, 7 MV/cm, or 9 MV/cm) and recording the voltage at this point. The dielectric breakdown simulation results are shown in Fig. 3. While SiO_2 can exhibit dielectric strengths as high as 9 MV/cm, this value greatly depends on oxide film quality and disregards operational fatigue induced during the device lifetime [10 & 11]. For SiC trench devices, the trench geometry is a governing factor in the life expectancy of the gate dielectric. Eliminating features responsible for high acute electric fields reduces the likelihood of premature gate dielectric failure. Unsurprisingly, the intense localized electric field associated with a sharp trench corner model resulted in low dielectric breakdown values. Increasing trench corner radius results in a more evenly distributed electric field, thus increasing the overall blocking voltage supported before dielectric failure. Between 150 nm and 250 nm corner radius, there are more modest improvements in breakdown voltage for all plotted dielectric field values. The marked improvement in breakdown voltage between 0 nm and 150 nm highlights that simply eliminating a sharp corner has the greatest impact on electric field distribution. Fig. 3 A, B and C show the electric field distribution of various trench corner radii at breakdown (7 MV/cm electric field in this instance). The field distribution is acute in Fig. 3. A, due to the field crowding typical of a sharp corner. An important distinction to make is that, while this field does not spread a great deal from the corner, it is still great enough at inception to cause dielectric breakdown at the comparatively low voltage of 98 V. The 150 nm rounded corner example (Fig.3 B) is an improvement on the sharp corner, with a more even electric field distribution and a simulated dielectric breakdown voltage of 390 V Fig. 3 C displays an even greater field dissipation, corresponding to a higher dielectric breakdown voltage of 610 V.

Ultimately, the model presented only considers the impact of trench geometry on dielectric breakdown of the trench gate oxide. In practice, protective measures such as sidewall implants, a trench base sinker, or relief trenches parallel to the device would be employed to further reduce areas of acute electric field and improve the breakdown voltage in a real device.

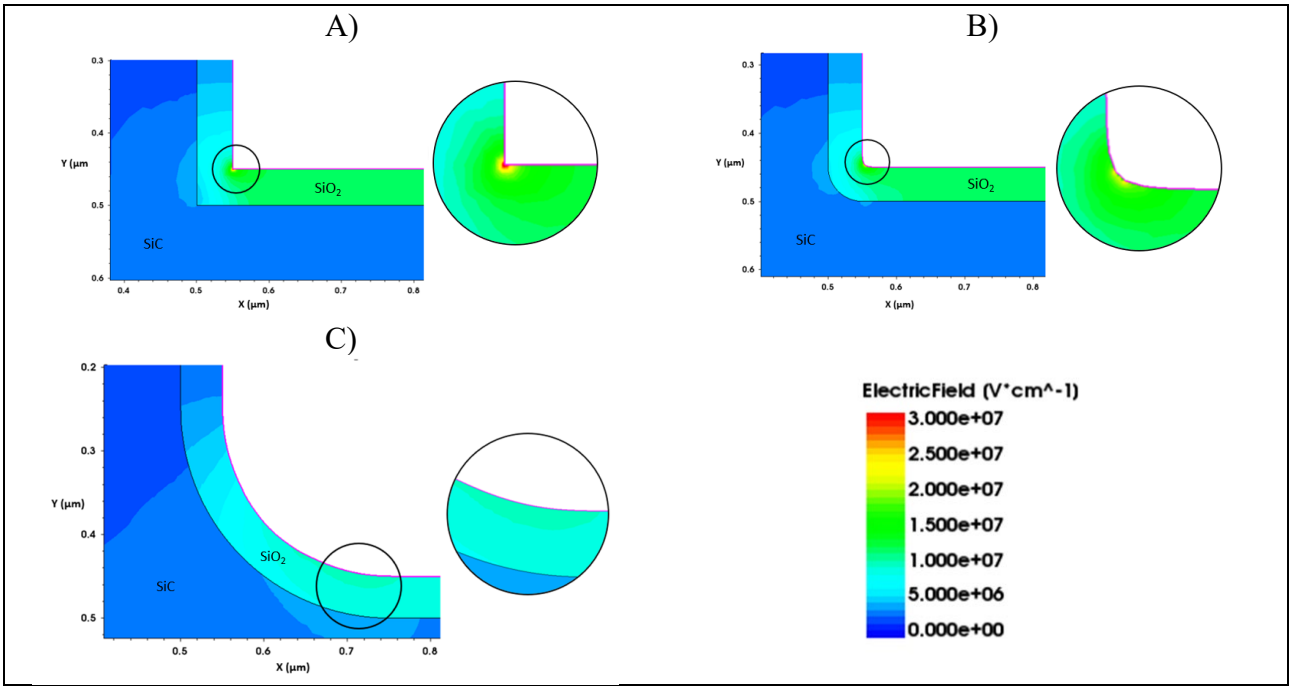

Fig 2. SiC trench gate MOSFET electric field distributions at 750 V reverse bias. A) Sharp corner, B) 50nm radius of curvature, and C) Radius of curvature of 250 nm.

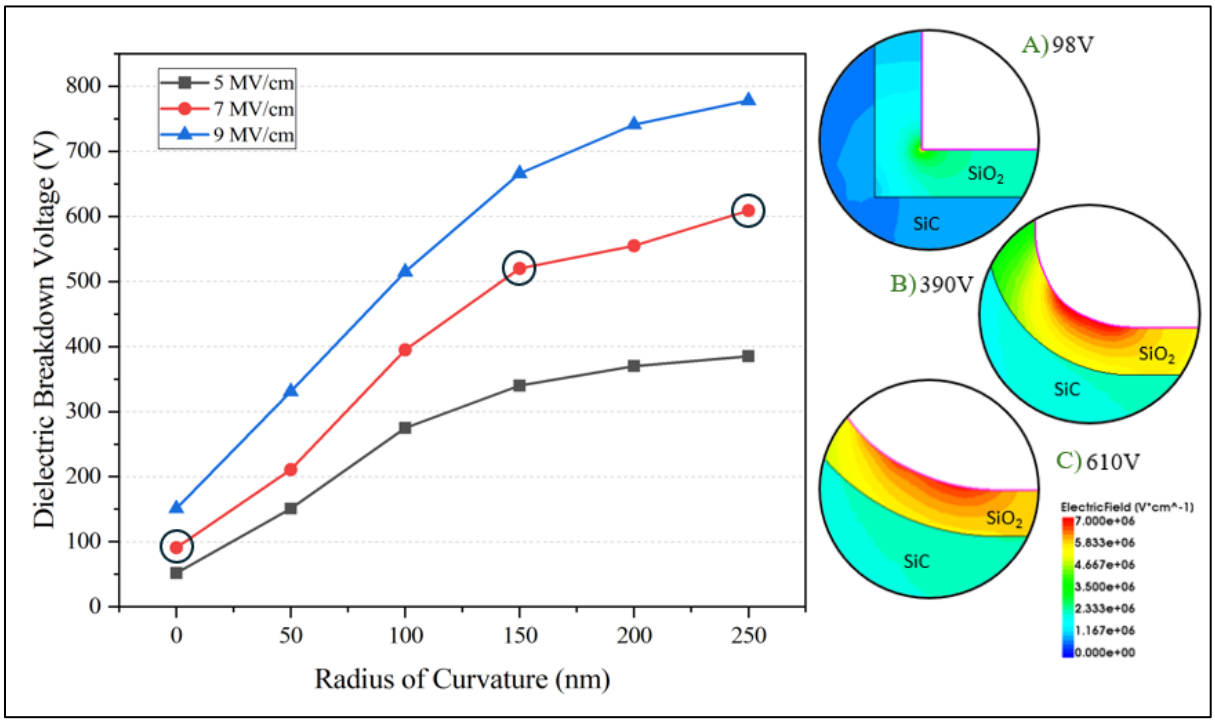

Fig 3. SiC trench gate MOSFET gate oxide breakdown study. Dielectric breakdown electric field value set to 5 MV/cm, 7 MV/cm and 9 MV/cm. Electric field profiles at breakdown (7 MV/cm) are shown, along with corresponding dielectric breakdown voltage, for A) sharp corner, B) 150nm corner, and C) 250nm corner.

SiC Rounded Trench Etch

The novel two step SiC rounded trench etch method is detailed in Fig. 4. The first step is typical of a directional ICP-RIE SiC process; while the rounding step can be adjusted to yield specific radii. The Synapse™ high density etch source is detailed in Fig. 5. An adjustable wafer chuck height allows improved control over near-wafer plasma density, etch rate and cross-wafer etch uniformity.

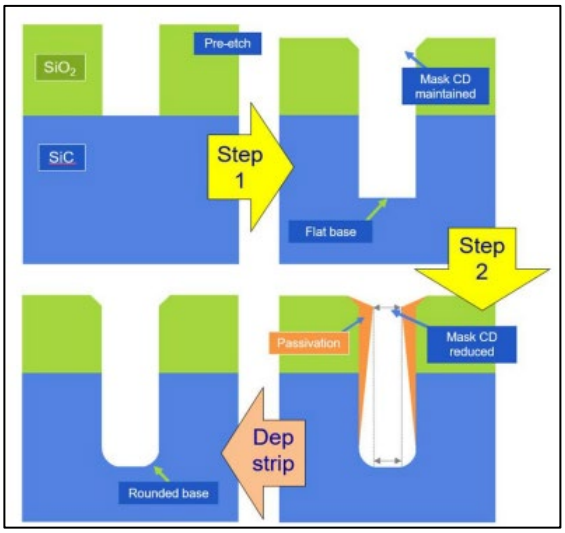

Fig 4. SiC rounded trench etch process flow. Sidewall passivation buildup is visible at step 2.

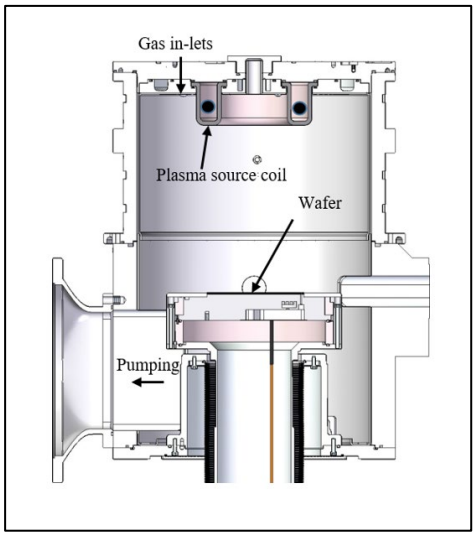

Fig 5. Schematic of the SPTS Synapse™ plasma etch chamber. The wafer chuck is raised during processing, maximizing ion density at the wafer surface for improved etch rates.

SiC rounded trench etch results are presented in Fig. 6 and Fig. 7. Fig. 6 shows the influence of the passivation build up as the etch step progresses, resulting in the effective narrowing of the etch area (exposed SiC). This process mechanism holds true for varying trench widths. The 2-step etch process exhibits an overall etch rate of 500 nm/min, 3.5 : 1 selectivity to the SiO_2 mask and a cross-wafer depth non-uniformity of ±3% at an edge exclusion of 4 mm.

The 1µm wide trench seen in Fig. 7 has undergone O_2 plasma cleaning to remove the side wall passivation. The SiO_2 hardmask is still visible however, and is later removed using wet etch methods, a common step in the production of SiC devices. The corners in the trench (Fig. 8) have a radius of ~250 nm, the depth is 1.4µm, the trench top width is 2.0µm and the side-wall profile angle is 88.8°.

Given that most device manufacturers will implement mobility recovery annealing regardless of trench architecture [12, 13, 14 & 15], the presented rounded trench etch offers the benefit of tunable trench base corner rounding without excessive alteration to the trench opening corners. Likewise, it is predicted that if a typical post-etch anneal for sidewall smoothing is performed following the rounded trench etch, the resulting trench base corners will be rounded to a greater extent than the trench opening corners.

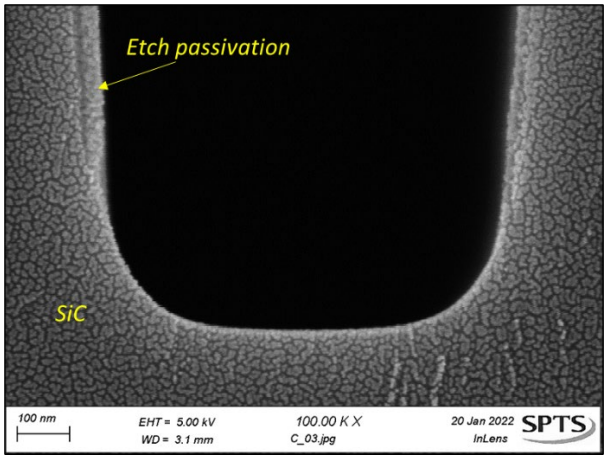

Fig 6. SiC rounded trench etch. Trench opening width of 1 µm. Etch side wall passivation is visible, deposited during the second step of the etch.

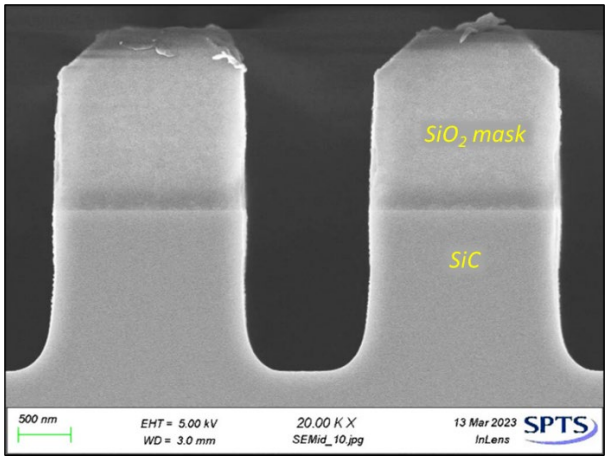

Fig 7. SiC rounded trench etch following initial passivation strip by O_2 plasma clean, prior to oxide mask removal. Trench opening width of 1µm. Distinct trench base corner rounding is visible, while the trench opening corners are less affected.

SiC Trench MOS Capacitor Study

Fig. 8 details the two trench MOS-capacitor corner structures. Each individual device consists of multiple trench rows in a 50 μm^2 area.

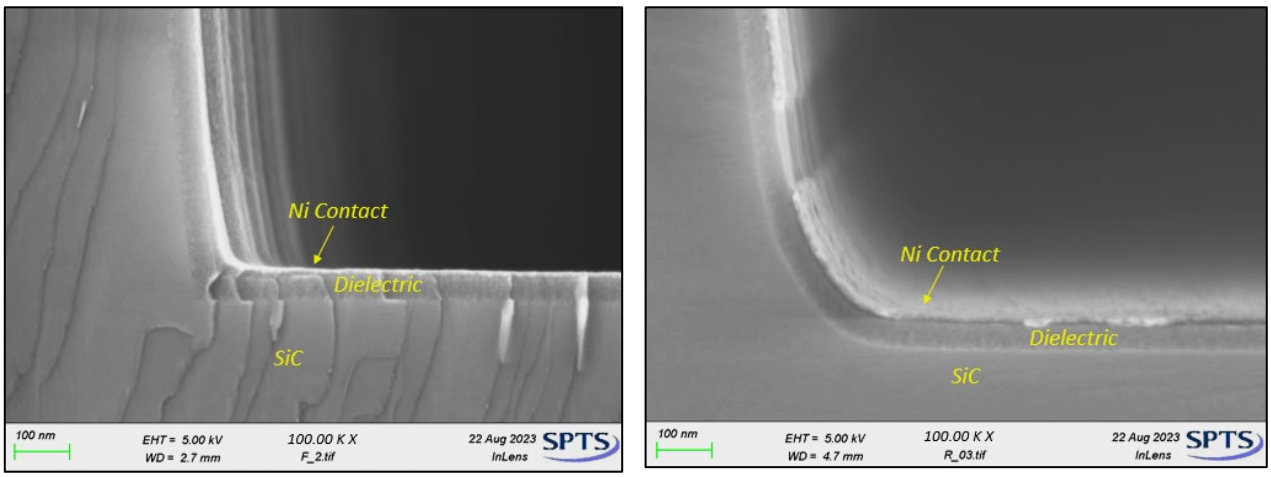

Fig 8. A) Sharp trench MOS-capacitor corner cross section, and B) rounded trench MOS-capacitor corner cross section. 50 nm Al_2O_3 dielectric layer and 20 nm Ni contact coat the trench, while a base Ni contact is not shown.

The MOS-capacitors featuring rounded corners at their base exhibited a greater breakdown voltage on average than the MOS-capacitors featuring square based trenches. The lower breakdown voltage of the square based devices is suggested to be due to electric field concentration at the sharp corners of the trench leading to localized dielectric breakdown at a lower voltage. This is supported by the simulation results (Fig. 3), showing dissipation of electric field, increasingly so with greater corner rounding. Fig. 9 displays *I-V* curves of a pair of 2.0 μm trench width MOS-capacitors (flat vs. rounded architecture) obtained during breakdown voltage *I-V* testing, with the rounded trench example exhibiting leakage at higher voltage before gate oxide failure.

Fig. 10 indicates that the middle 50% of flat-based trench devices failed between 25 V and 32 V, while the round-based devices skewed towards a 26-43 V breakdown voltage range. The round-based devices show a much wider spread of results. The flat-based device population has a lower median, by about 7 V, as well as fewer incidents of outlier results. Further analysis of leakage rates prior to breakdown, and time-dependent dielectric breakdown (TDDB) studies are planned in the future, as this may give an indication of failure mode. Additionally, an in-depth study on etch uniformity concerning the degree of corner rounding achieved across the wafer is also planned. Devices with rounded trenches likely maintained lower localized electric fields, resulting in breakdown voltages improved by up to 21.7% on average, when compared with the sharp corner devices.

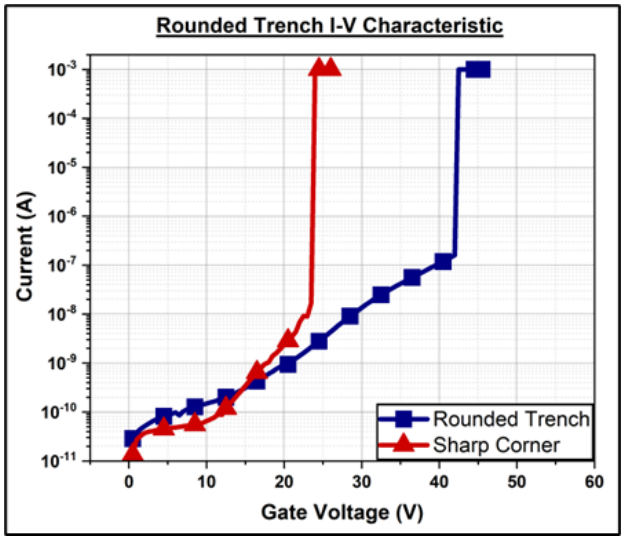

Fig 9. Plot comparing *I/V* measurements of rounded vs. flat trench devices. Device trenches of width 2.0 µm to 2.0 µm depth.

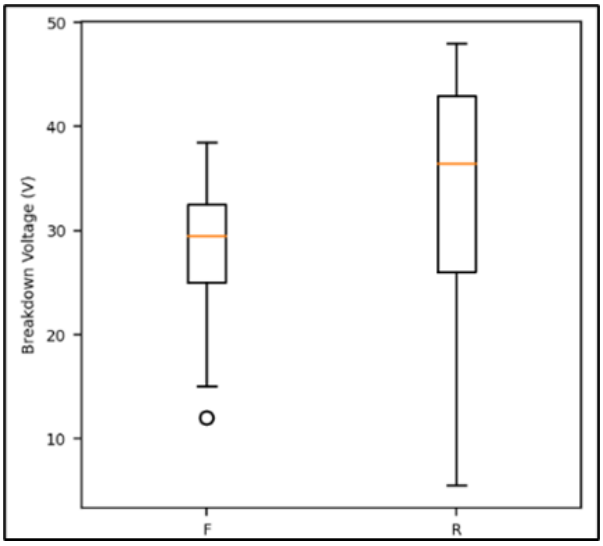

Fig 10. Box plot comparing the measured breakdown voltages of devices with sharp trench bases (F) vs devices with rounded trench bases (R).

Conclusions

The impact of trench geometry on electric field distribution in SiC trench devices is well understood, but fabricating ideal trenches with tailored corner radii is not straightforward. Sentaurus TCAD modelling confirms that electric field crowding at the trench MOSFET base corner has a direct impact on gate dielectric breakdown. In conjunction, dielectric breakdown measurements of fabricated SiC trench MOS-capacitors indicate that the presence of a trench corner radii increases the overall dielectric breakdown voltage. Implementing a SiC etch process capable of tunable trench base corner radii offers a great amount of freedom to device designers and manufacturers in the future. Processes such as post-etch H_2 anneal for sidewall smoothing and mobility recovery remain useful in the fabrication of SiC trench power devices. However, utilizing these post-etch processes in conjunction with an etch process for *in situ* corner rounding, such as presented here, offers the capability to reduce post-etch processing times, while achieving improved trench geometries.

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