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High Mobility 4H-SiC p-MOSFET via Ultrathin ALD B_2O_3 Interlayer between SiC and SiO_2

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Abstract. This article presents an innovative approach to achieve a high channel mobility for 4H-SiC p-MOSFET via dielectric-semiconductor interface engineering involving atomic layer deposition (ALD) of ultrathin B_2O_3 and SiO_2 stacks. The application of ultrathin boron oxide via ALD introduces a highly manufacturable solution for the passivation of SiC interface. The interface states near valence band reduces the channel mobility for SiC p-MOSFETs and increases the threshold voltage. The introduction of ultrathin B_2O_3 interlayer reduces the threshold voltage and improves the field effect mobility to 12.60 cm^2/Vs while the p-MOSFET without the interlayer provides the mobility of 8.91 cm^2/Vs. This work also includes the optimization of the post-deposition annealing (PDA) conditions specific to ultrathin B_2O_3 and bulk SiO_2 dielectric stack to obtain high field effect channel mobility for SiO_2/SiC p-MOSFETs.

Introduction

Silicon Carbide (SiC) has emerged as a promising material for high temperature power electronics due to its capacity to function at extreme environment. The inherent capability to maintain operational efficiency at high temperature, high electric field and high radiation has spurred significant research endeavors in past few decades [1]. To address the challenges posed by extreme environments, researchers have been exploring wide bandgap materials as an alternative to traditional silicon technology for several decades [2], [3], [4], [5]. Among the various wide bandgap semiconductors, SiC stands out as having the greatest potential for achieving not only for power devices but also Complementary MOS technology and integrated power ICs for high-temperature and high voltage applications. This is mainly attributed to its capability for both p-type and n-type implantation, as well as its advanced level of process maturity. SiC's remarkable ability to function effectively at elevated and cryogenic temperatures also allows for the integration of control electronics on the wafer level alongside discrete high-power devices [6] resulting in the reduction of the need for costly cooling systems and minimizes space requirements, decreases gate driver delays, and enhances the overall stability of the system. SiC boasts significant advantages over silicon, including a higher critical electric field (approximately 10 times), a larger bandgap (roughly 3 times), and superior thermal conductivity (around 3 times). Remarkably, it maintains crystallographic similarity and bulk mobility with silicon, making SiC a more compelling option compared to other wide bandgap semiconductors. Its ability to offer low leakage currents and reduced conduction loss at high field and temperature has garnered considerable research interest in SiC CMOS technology [7], [8].

Integrated circuits (ICs) based on SiC have been successfully demonstrated on both 4H- and 6H-SiC substrates, surpassing the performance of silicon-based ICs at high temperatures [9], [10], [11], [12], [13], [14]. Nevertheless, the majority of SiC ICs rely primarily on n-MOSFETs, primarily due to the subpar performance of p-MOSFETs, which exhibit low field-effect mobility and high threshold voltage. Despite the numerous advantages offered by CMOS technology, such as faster high-to-low transitions thanks to the use of p-MOSFETs instead of load resistors, the ability to achieve pure logic zero and one, and improved noise immunity, there is a need to explore and develop high-performance p-MOSFETs. While SiC power MOSFETs are available in the market, and SiC ICs have been

demonstrated, their performance still falls short due to the presence of traps (D_{it}) at the SiO_2/SiC interface, which negatively impacts the inversion channel mobility [15]. In pursuit of this goal, several techniques have been successfully demonstrated to enhance the interface traps near the conduction band, ultimately leading to the development of high-mobility SiC n-MOSFETs or n-JFETs. These techniques and their details can be found in the review by *M. Cabello et al*. [16].

As of now, advancements in SiC p-MOSFET technology have not yielded a high-performance solution. The inherent low bulk hole mobility along with the traps near valence band is liable for poor p-MOSFET behavior. The performance of p-channel MOSFETs is heavily influenced by traps near the valence band, a characteristic that is challenging to predict using capacitance-voltage (CV) characteristics due to the extremely low inversion carrier concentration in MOS structures. Notably, the interface trap density near the valence band in SiO_2/SiC MOS structures is considerably higher compared to that near the conduction band [17]. Reported literatures have very low mobility for p-MOSFETs due to aforementioned reason [2], [12], [18], [19], [20] and higher mobility has been obtained for the p-MOSFET with very low channel doping which is not feasible for CMOS application due to short channel effects. In this study, a highly manufacturable non-rare earth solution is presented, involving the use of a simple atomic layer deposition (ALD) technique to create an ultrathin boron oxide interlayer. This innovative approach has been shown to enhance the field-effect mobility and lower the threshold voltage of 4H-SiC p-MOSFETs. The results were compared to without boron oxide interlayer to emphasis on the importance of the interlayer. This report also includes the PDA parameters – annealing duration and annealing temperature optimization and establishes that 1100˚C annealing for 30 minutes in diluted N_2O/Ar environment for 30 minutes is the best post deposition annealing for SiO_2/SiC p-MOSFET with boron oxide interlayer.

Experiments

Lateral p-MOSFETs were fabricated on 4H-SiC epi layer grown 4˚ off-axis from 1120 plane. The epi layer doping $3x10^{16}$ /cm^3 to align with our previous CMOS results [6]. Aluminum ion implantation was performed on a 4-inch wafer to form the p+ junctions with a doping concentration of $1x10^{19}$ /cm^3 and annealed at 1700˚C for 10 minutes for activation. The same wafer was then diced into 1.5 cm x 1.5 cm for gate oxide split conditions for the p-MOSFET fabrications, so they only have the oxide condition as varying parameter. The gate oxide split is shown in the table. 1. MOSCAPs were also fabricated. Unless otherwise specified, the samples were cleaned with 3:1 piranha solution for 5 minutes followed by 10:1 BOE solution diluted by 50% in DI water for another 5 minutes prior to the dielectric deposition. 10 cycles of atomic layer deposition (ALD) of boron oxide were performed at 52˚C with Tris(dimethylamino)borane (TDMAB) and O_3 precursors to form an ultrathin (0.5-0.8 nm) boron oxide followed by 300 cycles of ALD SiO_2 (38-40 nm) at 270˚C using bis(diethylamino)silane (BDEAS) and O_3 precursors. The samples were annealed at different split conditions in diluted (20%) N_2O/Ar environment in a furnace.

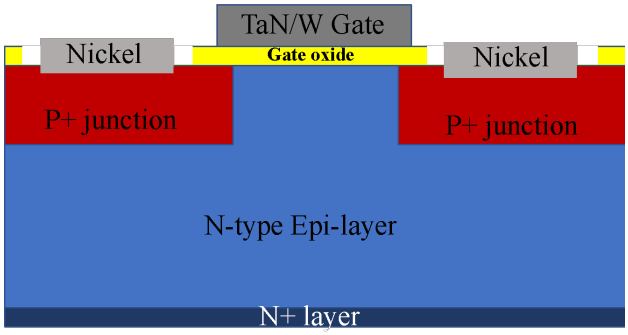

Fig. 1. Cross-sectional view of the p-MOSFETs presented in the report. Nickel junctions were used as source/drain and the N+ layer on the back side was used as the substrate contact. For the rest of the report, substrate and source is considered as ground (0V).

After the gate oxide formation and annealing, TaN and W were deposited to form gate electrode. The junctions were etched and 50 nm nickel was deposited to form source/drain contacts. The devices were annealed at 950˚C for 45 seconds in rapid thermal annealing system for ohmic contact formation. The cross-sectional view of the p-MOSFETs is shown in Fig. 1.

Table 1. Gate oxide split conditions.

Sample #	Piranha Clean (minutes)	BOE Clean (minutes)	ALD	PDA	
				Temperature (˚C)	Duration (minutes)
1	5	5	B_2O_3+SiO_2	1100	60
2			B_2O_3+SiO_2	1100	30
3			B_2O_3+SiO_2	1100	15
4			B_2O_3+SiO_2	1000	60
5			B_2O_3+SiO_2	900	60
6			B_2O_3+*SiO_2	1100	30
7			SiO_2	1100	60
8			SiO_2	1100	30
● Reduced physical thickness to obtain same EOT as SiO_2 only conditions					

Results and Discussions

Initial Characterizations on MOS Capacitors. Metal-Oxide-Semiconductor (MOS) capacitors were fabricated in order to accurately measure the effective oxide thickness (EOT) which is very crucial for mobility calculation. Also, MOS capacitors provide a baseline for the interface quality for typical MOS structure. Fig. 2 (a) and (b) show the frequency dispersion of n-MOSCAP on SiO_2 only condition (#8) and ultrathin B_2O_3 and SiO_2 bilayer condition (#6). Although both conditions show excellent frequency dispersion behavior, boron treated sample exhibits slightly better dispersion characteristics. Boron treated sample also shows less hysteresis as compared to the sample without boron incorporation. The amount of ΔV_{FB} from the hysteresis plot (Fig. 2(c) and (d)) is 0.085 V and 0.149 V for capacitors with and without boron incorporation respectively. All measurements were performed at room temperature. CV characteristics were carried out for all the conditions presented in the study and effective oxide thickness was extracted using [21].

Fig. 3 (a) shows the density of interface states from the frequency dispersion data. The D_{it} was extracted using Terman method using 100kHz frequency C-V as C_{HF} and 500 Hz frequency C-V as C_{LF} [22]. Although this assumption of low frequency CV underestimate the Dit value since it ignores the traps with a lifetime of 2 ms or more, it provides a good qualitative understanding about the interface quality with boron incorporation. One drawback with ALD SiO_2 process is the requirement of high temperature post deposition anneal (PDA) in order to densify the dielectric and anneal out all the defects inside the SiO_2 dielectric. This high temperature PDA process causes a growth of low quality oxide at SiO_2/SiC interface [23]. Our hypothesis is that the ultrathin boron oxide prevents this low quality oxidation via SiO_2 and B_2O_3 reaction which reduces the density of interface traps. This argument is further attested in Fig. 3(b) that shows the leakage current characteristics at room temperature as well as at 150˚C of the MOS capacitors. Boron incorporated samples have better gate leakage characteristic compared to SiO_2 only conditions. Incorporation of ultrathin Boron did not alter the breakdown strength as the breakdown field is little over 10MV/cm. At higher temperature, since there are more thermally generated carriers, more interface traps get activated resulting higher Fowler-Nordheim (FN) tunneling currents [24] for all conditions.

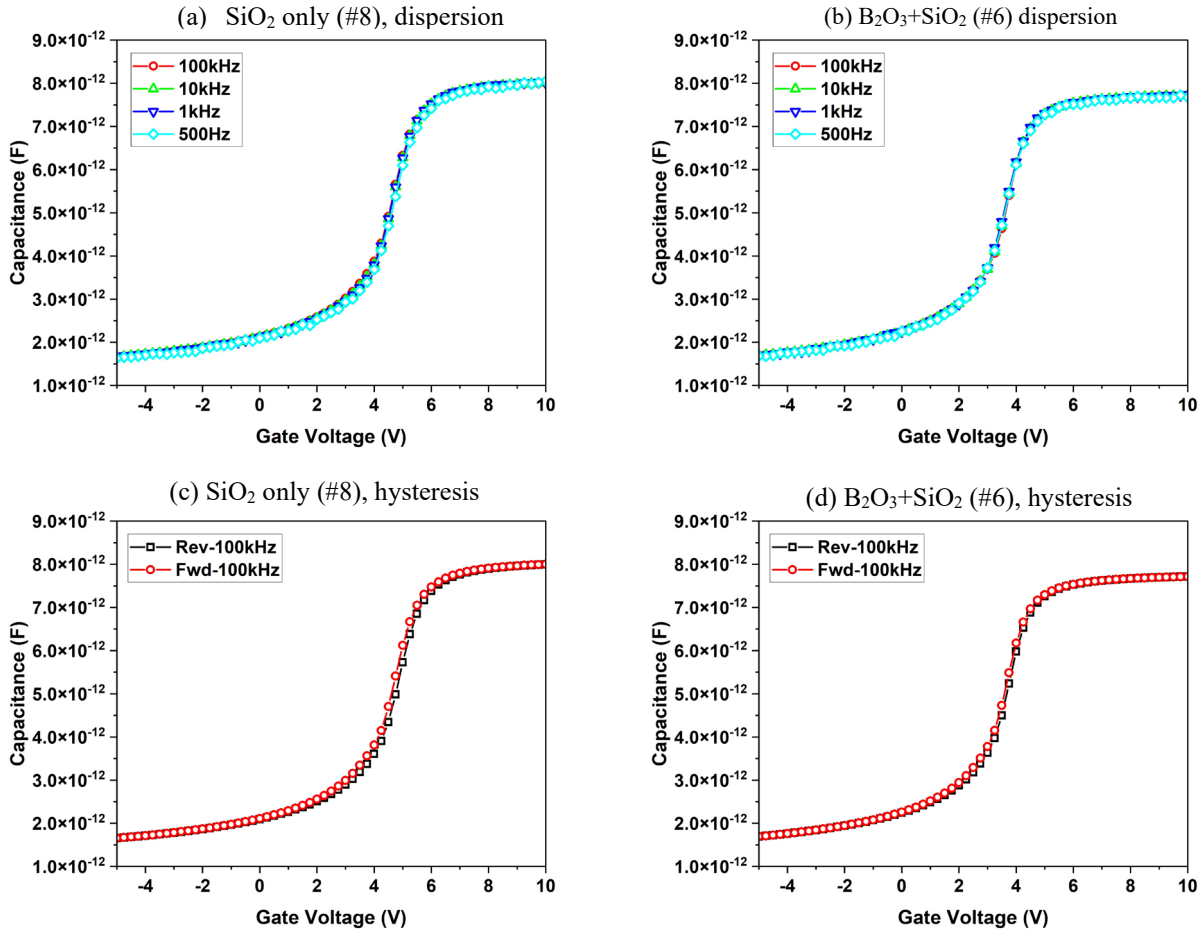

Fig. 2. Room temperature Capacitance vs Voltage Characteristics. (a) and (b) are C-V characteristics at different frequencies. (c) and (d) are the hysteresis behavior conducted at 100 kHz frequency.

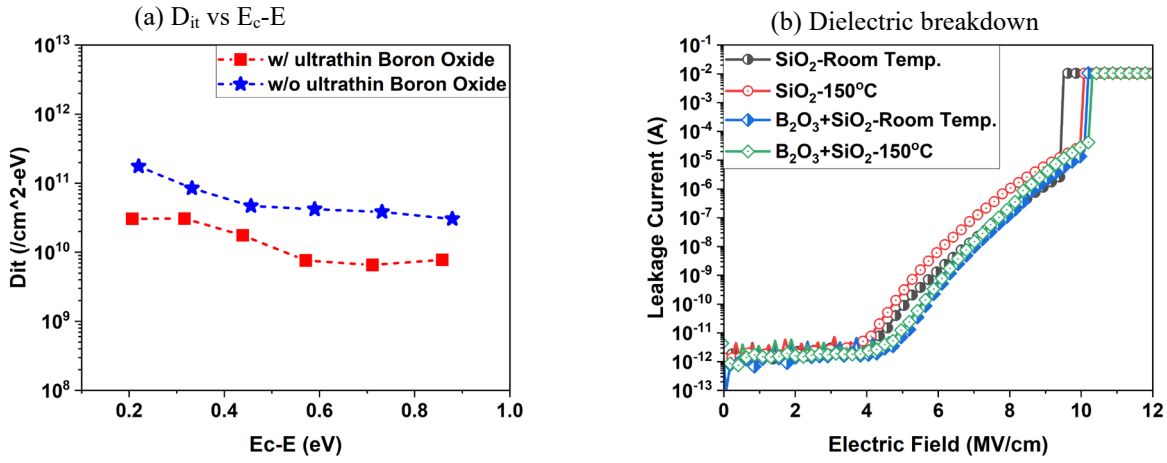

Fig. 3. (a) density of interface traps extracted using Terman method. (b) Gate oxide breakdown comparison for boron incorporated and SiO_2-only conditions at room temperature and 150˚C.

Optimization of Post deposition annealing (PDA). Fig. 4 (a) shows the transfer characteristics of p-MOSFET with boron incorporated sample annealed at 900˚C, 1000˚C, and 1100˚C. The mobility of 900˚C annealed sample is 7.64 cm^2/V-s. This low mobility is possibly originated from lack of densification and oxygen vacancy reduction due to lower temperature [25] and the un-passivated B_2O_3 at the interface that acts as trapping centers. As the annealing temperature increased to 1000˚C,

the mobility improves to 9.01 cm^2/Vs indicating better interface. 1100˚C annealing improves the mobility further to 10.18 cm^2/V-s. The threshold voltages for 900˚C, 1000˚C and 1100˚C were -11.33, -13.79 and -13.97 V which is due to larger EOT formed during higher temperature oxidations. It is noted that the mobility of boron incorporated p-MOSFET reduced when annealed at 1200˚C (not shown). Therefore, 1100˚C PDA provides the best annealing temperature for 0.5 nm boron incorporation (10 cycle).

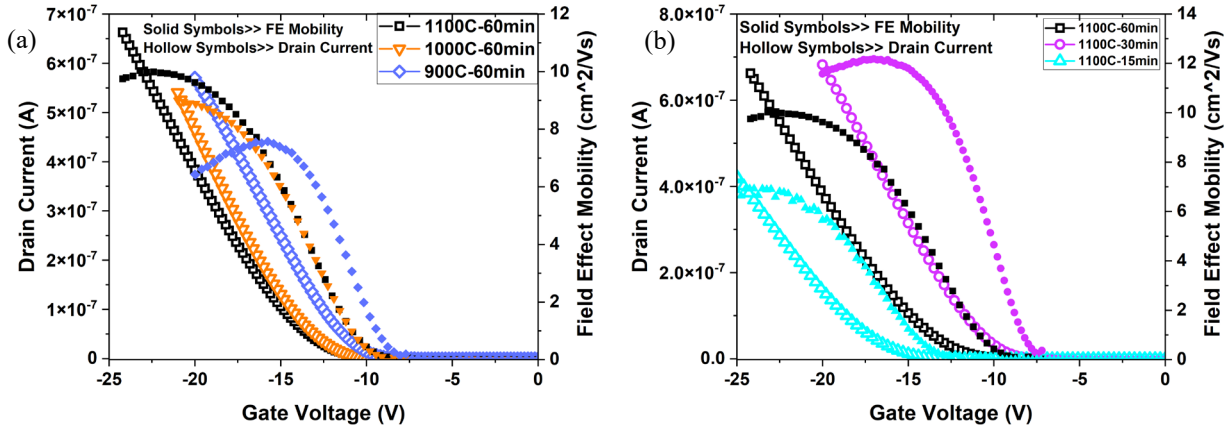

Fig. 4. (a) Transfer characteristics of 10 cycles boron oxide and 300 cycles SiO_2 with 900-1100˚C PDA for 60 minutes (samples #1, #4 and #5). (b) Transfer characteristics of condition #1, #2 and #3. 60 minutes anneal is too long and produces low quality oxide with carbon related clusters while 15 minutes anneal is too short for the densification of SiO_2

Fig. 4 (b) shows the transfer characteristics (I_D vs. V_{GS}) of the p-MOSFET annealed at 1100˚C in N_2O/Ar (20% N_2O) with three different anneal times 15, 30, and 60 minutes). 15 minutes of anneal time is not enough as the mobility value of 6.95 cm^2/Vs with a large threshold voltage of -16.51 V. The mobility of this condition (1100˚C 15 minutes) is less than 1000˚C 60 minutes. In addition, 15 minutes of annealing time is short duration to densify SiO_2. Sample with 30 minutes anneal produces the highest mobility of 12.23 cm^2/Vs and low threshold voltage of -12.23 V. It was found that 60 minutes of annealing actually decrease the mobility to 10.18 cm^2/V-s and the threshold voltage increases to -13.97V. This can be explained by the fact that oxidation takes over the SiC interface and dilute the effect of boron passivation. We have observed the same effect with La_2O_3 passivation on SiC [26].

Effect of Ultrathin Boron Oxide. Since the 1100˚C annealed sample is the best with 0.5nm boron incorporation, we keep our focuses on the 1100˚C annealed conditions only. Fig. 5 (a) compares the mobility with and without boron oxide after 1100˚C annealing. 300 cycles of ALD deposited 38nm SiO_2. When PDA is done at 1100C in N_2O/Ar environment, densification, N_2O passivation, and oxidation occur at the same time. The longer the sample was annealed, the thicker the gate oxide. There was 4 nm increase in oxide thickness after 30 minutes of annealing (#8) at 1100˚C whereas there was 17 nm increase in oxide thickness for the 60 minutes of annealing (#7). This increase in oxide thickness also increases in threshold voltage as seen in Figure 5 (a). 30 minutes of annealing is not the most optimized condition for boron-free conditions as it lacks densification of ALD SiO_2. The EOTs extracted for boronated SiO_2 conditions are 51.66 nm (#1) and 49.76 nm (#2). The ultrathin boron oxide interlayer does not form borosilicate layer like lanthanum oxide interlayer [26] as there is no solid solubility line in the phase diagram of B_2O_3-SiO_2 [27]. According the Gibbs' free energy of formation [28] boron oxide breaks down and supply free oxygen to the SiO_2/SiC interface. Oxygen further reduces the oxygen vacancies along with the N_2O annealing while free boron possibly passivates π-bonded carbon clusters by reducing the charges of π-bonds. A TEM image of sample #6 is shown in Fig. 5 (b). Unlike common SiO_2/SiC interfaces [29], there is a much smooth transition from SiC to SiO_2 which indicates the boron oxide incorporation suppresses the low-quality

oxidations. Boron was not detected due to the size of the boron atoms. The inclusion of boron oxide at the interface forms a boron-rich interfacial oxide that counteracts the SiC/SiO_2 interface traps and provides enhancement of FE mobility in the SiC p-MOSFETs. The FE mobility of boron-free samples are 8.91 cm^2/Vs (30 minutes annealed) and 9.61 cm^2/Vs (60 minutes annealed).

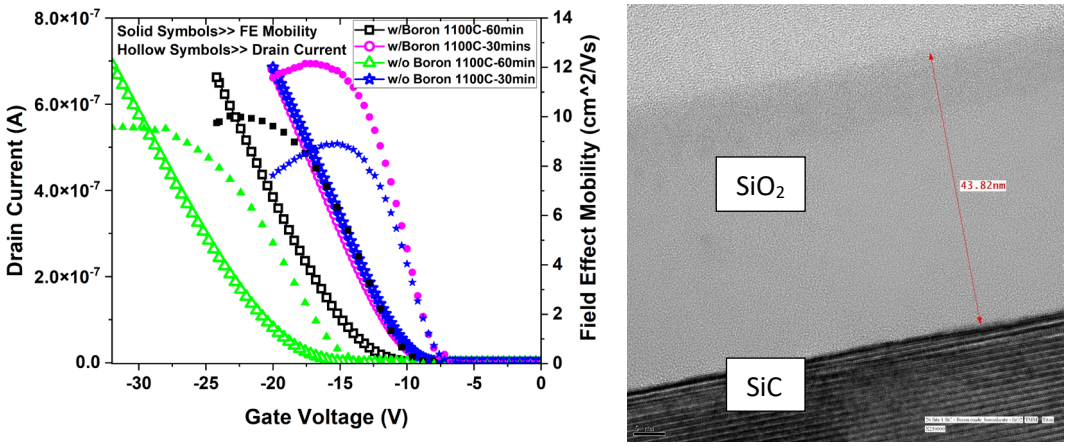

Fig. 5. (a) Mobility enhancement with ultrathin boron oxide interlayer between SiC and bulk SiO_2. The transfer characteristics are compared for 30 minutes, and 60 minutes anneal devices with their corresponding boron-free devices. (b) TEM image of boron incorporated sample (1100˚C-30 minute).

As we observe from the boron-free conditions (#7 and #8) that 300 cycles SiO_2 require more than 30 minutes of annealing, and 1100˚C 30 minutes annealed samples with and without boron incorporation has a large EOT difference, so the bulk SiO_2 ALD deposition cycle was reduced from 300 (#2) to 250 (#6), which results in similar EOT as the SiO_2-only conditions. The field effect mobility of boron-incorporated samples further improves as the thickness of bulk SiO_2 is reduced and it has enough thermal budget for densification. The highest mobility condition is thereby observed at a value 12.60 cm^2/Vs with threshold voltage going to the lowest 9.15 V due to suppressed interfacial oxidation and better densification. The transfer characteristics of boron-incorporated and boron-free device with EOT-matched conditions at room temperature and 150˚C measurement temperature are presented in Fig. 6. Notably, the FE mobility increases from 12.60 cm^2/Vs to 14.5 cm^2/Vs and the threshold voltage reduces form -9.15 V to -3.65 V for the boron-incorporated samples while similar trend is observed for all other conditions. This indicates the FE mobilities reported here are still coulombic scattering limited.

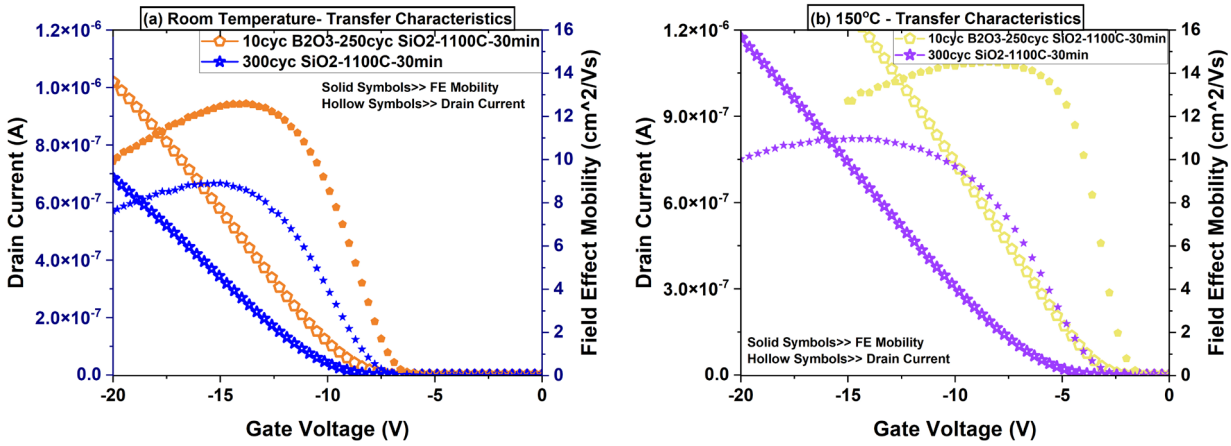

Fig. 6. Transfer characteristics at (a) room temperature and (b) elevated temperature (150˚C). 30 minutes annealed with and without boron oxide conditions (#6 and #8) are compared. The threshold voltage decreases, and the FE mobility increases which indicates the mobility is coulombic scattering limited.

The output characteristics (I_D vs V_{DS}) of the 30-minute annealed device with (#6) and without (#8) boron incorporation is presented in Fig. 7. The saturation current is doubled due to a combination of mobility enhancement and threshold voltage decrease with same oxide capacitance.

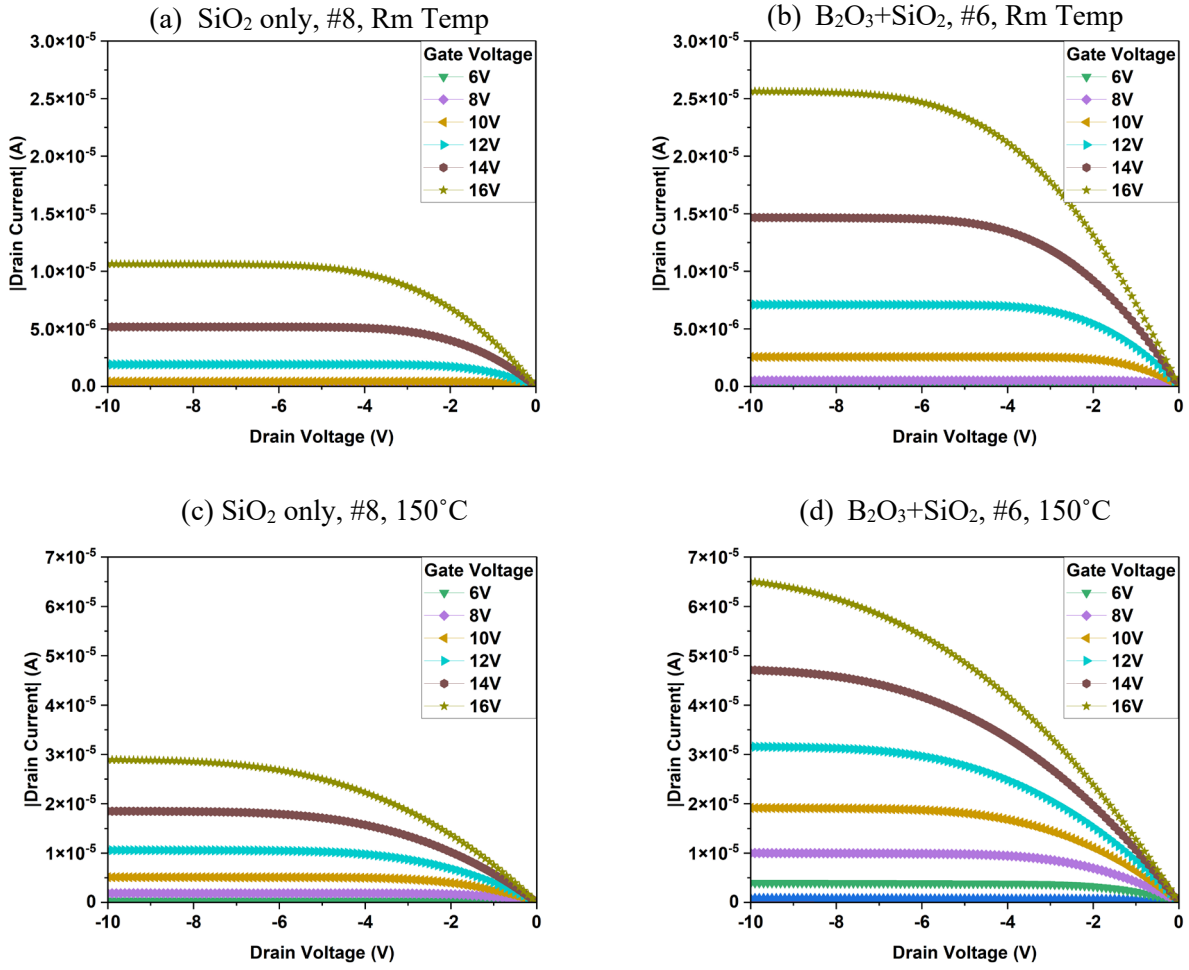

Fig. 7. The output characteristics (I_D vs V_{DS}) of 300 cycles ALD SiO_2-1100˚C annealed 30 minutes at (a) room temperature and (c) elevated temperature and 10 cycles ALD B_2O_3+250 cycles ALD SiO_2-1100˚C annealed 30 minutes samples at (b) room temperature and (d) elevated temperature.

To thoroughly assess the enhancement of interface properties through the incorporation of a boron oxide interlayer, we analyzed the samples with (sample #6) and without (sample #8) this interlayer in MOSFETs' transfer characteristics. This analysis focused on observing the hysteresis of the transfer characteristics in log scale, as depicted in Fig. 8. The transfer characteristics were evaluated, transitioning from the cut-off region to the saturation region and then back from saturation to cut-off. Remarkably, the samples with the boron oxide interlayer exhibited a significantly reduced hysteresis, less than 0.3V, in contrast to those without the interlayer, which demonstrated a hysteresis greater than 1.6V. This substantial reduction highlights the efficacy of the boron oxide passivation approach in mitigating oxygen vacancies and passivating π-bonded carbon clusters. Consequently, this technique anticipates significant enhancement in the reliability of ALD SiO_2 layers for SiC MOS transistors, showcasing the pivotal role of boron oxide in interface improvement.

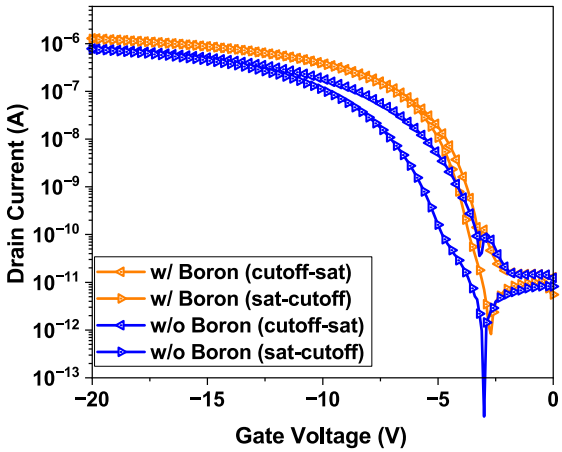

Fig. 8. The hysteresis of transfer characteristics in log scale. Samples with boron interlayer (#6) show 0.299V while samples without the interlayer (#8) show 1.6V of hysteresis in the log scale transfer characteristics in room temperature.

Conclusion

This paper reports a new method to boost the performance of SiC p-MOSFETs by passivation of the interface states using ultrathin boron oxide interlayer. The use of ALD boron oxide provides a practical way to incorporate SiC into CMOS technology without relying on rare-earth materials. This solution helps overcome two main issues with SiC p-MOSFETs: high threshold voltage and low channel mobility. The improved mobility due to the ultrathin boron oxide treatment suggests better interface conditions, which could help reduce instability under harsh conditions, although further research is needed in the future. Importantly, our tests at 150°C showed that the device maintains its performance avoiding any temperature related degradations.

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