# A Comparison between Different Post Grinding Processes on 4H-SiC Wafers

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Abstract. The need of removing the mechanical damage and the stress introduced during the thinning step of device process flow is challenging for manufacturing of high quality SiC-based devices. In this respect we have identified two different back finishing approaches, based on material removal and material rearrangement. The first one includes dry polishing (DP) and chemical mechanical polishing (CMP); the second one includes bulk and laser annealing. Systematical investigation on wafer warpage, sample morphology and die mechanical reliability have been conducted and comparison between the two approaches has been done. The CMP and DP processes can remove the damage produced by back grinding, recovering wafer warpage and resulting in a smoother surface. Bulk thermal annealing has provided better roughness levels and has been successful in stress relief, although the wafer permanence at high temperature is not compliant with the device process flow. Under laser annealing process, the surface features keep almost unchanged as well as warpage level. Despite being not effective in stress relief, from a mechanical point of view, the laser annealing process, does not impact die reliability, representing a suitable back finishing process especially in the optic of its use in backside ohmic contact formation.

#### Introduction

Silicon carbide (SiC) is having a wide use in power electronics technology due to its excellent physical and chemical properties, e.g., wide band gap, high breakdown field and high thermal conductivity [¹]. In the fabrication process of metal oxide semiconductor field effect transistor (MOSFET) devices, the Rds(on), for low voltage devices (650V) is primarily a function of the device thickness and hence of the whole thickness of the wafer. Wafer thinning using conventional backgrinding process thus must be carried out to improve device performances, reduce undesired power dissipation and provide greater package miniaturization. One of the major drawbacks of wafer thinning is the generation of residual stress that increases wafer warpage and makes it fragile, causing breakage event during handling or further processing as well as reducing die yield. Thus, it is very important to restore both the mechanical strength and the wafer warpage to their original status by performing a stress relief process.

The thinning process performed on SiC substrates shows instability effect related to the grinding process itself and, in some case, to the intrinsic characteristic of the material such as mechanical properties, doping concentration as well as defect density in correspondence of the damaged area [²]. Conventional grinding process causes deep SSD (sub-surface damage), with cracks and amorphous regions clearly visible by morphological analysis, which induce wafer warpage. The thinned part of the substrate can be considered as a film which causes variations on wafer bowing, introducing a compressive stress on the wafer surface [³, ⁴], whose thickness depends on the size of grinding wheel used [⁵]. In order to reduce the stress, increase the wafer strength and reduce the wafer level warpage, a stress relief process becomes necessary. Currently, stress relief in Silicon wafers is carried out by wet-etch process with acid etchants. However, 4H-SiC has a very high hardness and a remarkable chemical inertness compared to silicon, which makes difficult to chemically relief the stress. Alternative ways to relief the stress induced by grinding such as polishing with fine grained wheel

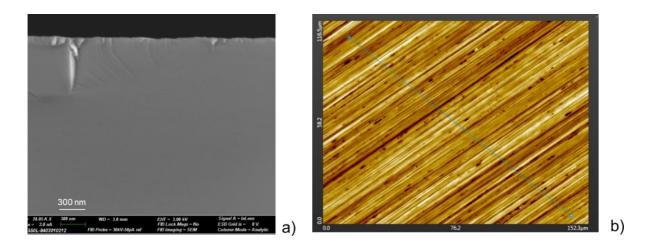
(dry polishing), chemical mechanical polishing (CMP) as well as thermal approaches will be considered in our work. To this purpose, commercially available 150 mm 4H-SiC substrates have been used. Samples have been characterized in terms of morphology and warpage. Effectiveness of the different stress relief processes has been evaluated with particular emphasis on the laser annealing process for which the goal has been to provide comprehension of the mechanism governing the temperature and stress distribution on the irradiated region. Finally, die flexural strength measurements have been reported.

## 2. Experimental Details

4H-SiC substrates with 4° off-angle towards <11-20> and 350 μm thickness have been used in this work. Wafers have been thinned down to 180 µm by performing a mechanical grinding on the C-face using a conventional in-feed grinding process. Different post grinding treatments have been performed to remove the grinding subsurface damaged region. On a set of wafers Dry Polishing process (DP) has been performed at a maximum load of 90 N and a current value of 7 A. On another set of wafers Chemical Mechanical Polishing (CMP) in acid ambient has been performed. Bulk thermal treatment has also been considered by performing two different thermal processes: a bulk treatment in oxygen atmosphere at a plateau temperature of 1050 °C for 30 min and a bulk annealing in argon atmosphere at a plateau temperature of 1675 °C for 30 min. A final group of wafers has been laser irradiated in nitrogen atmosphere at a pulse duration of 160 ns, a wavelength of 308 nm and an energy density in the range between 3 and 4 J/cm<sup>2</sup>. Warpage measurements have been performed by E+H MX 102-204-RA-2C tool. Surface morphology changes upon different post grinding treatments have been highlighted by optical profilometry analysis by MicroXAM-800, KLA TENCOR, to quantify the surface roughness by the RMS parameter (Sq) and the peak to valley height line parameter (Rt). Cross sectional TEM and FIB analyses have been performed to study sample structure. Three-point bending test (3pb, Instron 5566) has been performed on a variety of 5x4 mm die extracted from each wafer, to calculate the stress σ the die can withstand at breakage (flexural strength) [6]. Tool accuracy is of 0.5% and the support span length is of 3 mm. Load has been applied in correspondence of the center of the span length and has been increased at a constant rate of 0.5 mm/min.

#### 3. Results and Discussion

Figure 1 shows morphological analysis performed on as ground 4H SiC substrates. Wafer thinning process, that is the mechanical removal of SiC material, introduces damages in the form of residual stress and cracks in the SiC surface as shown in Figure 1a, which will have a major influence on the mechanical properties of the material. Several studies have shown the formation of a region in correspondence of the surface which acts as a layer of compressive stress [7,8,9], whose effect can be qualitatively understood by considering the grinding process as a superposition of multiple indentations with randomly shaped abrasive grains producing a plastically deformed volume in the material that is proportional in size to the indenter shape [10]. When the load is higher than a critical value crack will be generated, one lateral parallel to the surface and one radial along the groove normal to the surface. The combination of overlapping plastically deformed volume elements and thermal induced stress will give the zone of compressive stress. In our case large area FIB analyses (Figure 1a) have shown a damaged region induced by grinding that extends for about 650 nm and it is composed by subsurface median cracks perpendicular to the surface, initiated at the point where the loading stress level exceeded the tensile strength of the material, and lateral cracks originated in the surface region when the abrasive grain move away (scratch groove region) and the elastic-plastic deformation restores [11,12]. We associated to the grinding process a residual stress of about -450 MPa by substrate curvature changes calculation [13]. Optical profilometer analyses of SiC C-face performed after grinding are shown in Figure 1b. Grinding wheel marks are visible. The sample surface has an Sq value of about 4.6 nm and a Rt value of about 29 nm.



**Fig. 1.** (a) Cross sectional FIB and (b) plan view optical microscopy image of the 4H-SiC C-face after thinning process. Cracks extending up to 600nm below the SiC surface as well as rifling of the surface, fingerprints of the grinding process, are visible.

Figure 2 shows warpage values W normalized to the initial value W0 (as received wafers) after wafer thinning and after different subsequent surface finishing treatments. The thinning process causes an increase in warpage of about 8 times the original value. To be effective as a stress relief process, the post grinding treatment should bring the warpage value to the one measured before the grinding step (W/W0 $\approx$ 1). It has been found that performing a thermal treatment at 1050 °C makes the warpage value about 5 times higher than the pre grinding one. For bulk annealing temperature higher than 1675 °C, a drop on warpage value occurs, being in this case W/W0 $\approx$ 1. Slight changes in W/W0 values have also been noticed if mechanical-chemical CMP surface polishing or DP with a fine wheel mesh is used. Also note that, as a consequence of laser thermal treatment, the wafer warpage value keeps quite similar to the one measured after grinding, the fluence value under investigation having no impact (here not shown).

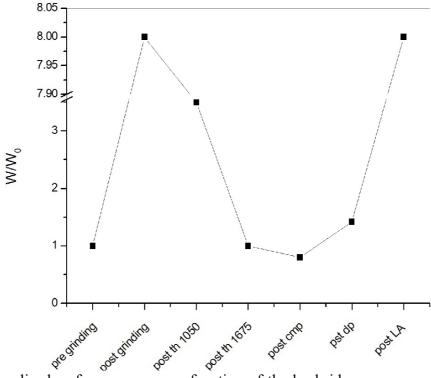
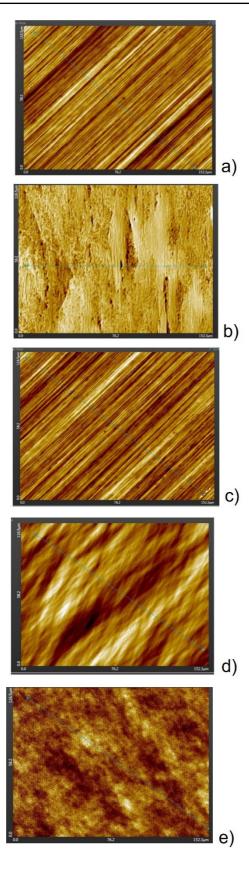


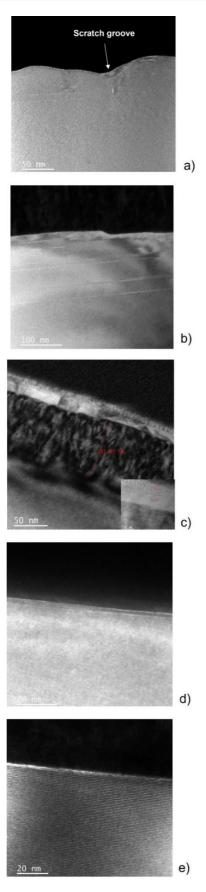
Fig. 2. Normalized wafer warpage as a function of the backside process as obtained by curvature measurements. An increase in  $W/W_0$  has been observed after thinning process. Subsequent surface treatments cause variations of wafer warpage suggestive of the impact the process can have on surface morphology.

Changes in wafer warpage represent a first indication of the morphological adjustments occurring on the thinned surface as shown by means of optical profilometer analyses on 4H-SiC C-face performed after post grinding treatment under investigation (Figure 3). Bulk thermal annealing at 1050 °C (Figure. 3a) carries no changes on sample surface with respect to the as ground samples (Figure 1b); the Sq and the Rt value being respectively of 4.5 nm and 20 nm in this case. The onset of surface morphology changes occurs at annealing temperatures higher than 1500 °C. This thermal budget causes SiC C-face rearrangements with large canyons along the sample, the surface wheel marks totally disappearing. As an example, an increasing in Sq value by a factor of 5 and in Rt value by a factor of 3 if compared with the reference ground surface has been observed for samples treated at 1675 °C (see Figure 3b). Note that, apart from the temperature value, it is quite important the thermal supplying mechanism, whether continuous or pulsed, as it is possible to see from Figure 3c showing the attempt of recovering SiC C-face after grinding by means of a laser annealing treatment at an energy density higher than 3.6 J/cm<sup>2</sup>. In this case, even if the temperature value is high enough to locally rearrange Si and C atoms at wafer surface, the surface morphology on laser annealed samples does not changes with respect to the reference as ground (Sq=4 nm, Rt= 20.8 nm). Quite flat SiC Cface can be observed in case of DP surface recovery attempt as well as in case of CMP, with Sq and Rt value respectively of 2.5 nm and 6 nm for DP and 0.6 m, and 3 nm for CMP (Figure 3d) and 3e)).



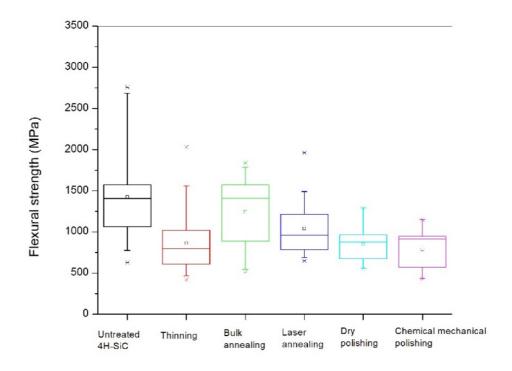
**Fig. 3.** Optical profilometer images showing morphological variations on SiC C-face surface (a) after bulk thermal treatment at 1050 °C, (b) 1675 °C, (c) after laser annealing, (d) after dry polishing and (e) after CMP process.

To deep insight structure and surface sample characteristics, cross section transmission electron microscopy (TEM) analysis has been performed (Fig4). After thermal annealing at 1050 °C the Cface damage due to thinning process persists (Figure 4a). The surface keeps the undulate topography already observed by profilometer investigation (Figure 3a) and some scratch groove regions, with V shaped amorphous deformation induced by the thinning process, are still evident [14]. Sample with thermal annealing at 1675 °C (Figure 4b) shows 4° off terraces of multiple height steps, imputable to a spontaneous atomic movement towards a free energy minimization during crystal rearrangement [15], and stacking faults generated by the movement of dislocations induced by the strain gradient inside the damaged ground region [16,17]. No cracks and evidence of scratch groove have been found. Laser annealing process in the fluence range between 3.6 and 4 J/cm<sup>2</sup> causes structural changes on SiC monocrystal due to the high temperature involved. The cross-sectional TEM image captured in case of leaser irradiation at 3.6 J/cm<sup>2</sup> shows a three-layer structure with a reconstructed region 80 nm thick at the interface with bulk SiC (Figure 4c), a Si layer 12 nm thick and a C layer 8 nm thick in correspondence of the surface (see inset of Figure 4c). The effect of DP and CMP approaches to stress relief grinding induced damages is an optimal surface quality with no defects and cracks (Figure 4d and 4e respectively). Dry polishing and CMP are effective as stress relief processes because they based on material removal: the damaged region is in fact mechanically chemically/mechanically removed. The wafer surface (Figure 3 d and e) is in these cases quite similar, in terms of roughness to the original not-ground one as well as the wafer warpage is restored to the not-ground levels (Figure 2). However, when dealing with SiC based devices fabrication, it is mandatory to guarantee a certain amount of surface roughness, after wafer thinning, to promote back side metal adhesion. In this respect, surface finishing treatments based on material rearrangement, i.e. the attempt to stress relief by thermal processing approached in this work, are more effective (Figure 3). Nevertheless, the way the thermal budget is delivered, whether continuous for prolonged time or with short impulses in the nanoseconds scale, is the discriminating factor to be successful in stress relief.



**Fig. 4.** Cross sectional TEM images of the SiC C-face after (a) bulk thermal treatment at 1050 °C, (b) at 1675 °C, (c) after laser annealing process, (d) after dry polishing process, and (e) CMP process.

Three-point bending test [<sup>18</sup>,<sup>19</sup>] performed on untreated 4H-SiC substrate, thinned, bulk thermally treated and laser annealed substrates are shown in Figure 5. The thinning process causes a worsening of flexural strength, whose median value reduces from 1423 MPa to 780 MPa due to subsurface damage in the form of microcracks and cracks. The flexural strength median value obtained for wafers subjected to bulk annealing is comparable with the corresponding value obtained for untreated substrate. No significative changes in flexural strength values have been observed after laser thermal treatment, dry polishing and chemical mechanical polishing.



**Fig. 5.** Variations of flexural strength as a function of the surface finishing process performed. The flexural strength value of bare SiC substrate is reported for comparison.

### 5. Conclusions

In this paper, finishing methods to recover the surface of thinned 4H-SiC substrates have been compared. Dry polishing (DP), chemical mechanical polishing (CMP), bulk and laser thermal annealing processes have been accounted and systematic investigations on wafer warpage, backside SiC wafer morphology have been conducted. The mechanical reliability at a die level has also been examined. Collected data reveal the efficiency of material removal-based finishing methods such as DP and CMP in restoring wafer warpage and surface quality to the original, not ground, level. Nevertheless, a certain value of surface roughness is necessary to promote at the final stage of the device fabrication flow, when SiC wafer is thinned to the final device operating thickness, the back side ohmic contact formation and the back side metal adhesion. In this respect, finishing methods based on material rearrangement, i.e., the attempt to restore the wafer warpage and surface quality by thermal processing used in this work, proved to be more efficient. In case of bulk thermal annealing, a high enough thermal budget is supplied for prolonged time in a way to guarantee atomic movement and rearrangement. We specifically found that at a bulk annealing temperature higher than 1500 °C, atoms in the damaged region rearrange towards a minimum free energy producing an irregular, terraced surface. The surface features can be eventually tuned by properly adjusting the thermal process in terms of maximum temperature and annealing time. Besides, the wafer warpage in this case is close to the original, before grinding process. The bulk thermal treatment hence demonstrated to be a good compromise between surface roughness and stress relief. However, the high temperature involved is not compliant with the device fabrication process flow. In case of laser annealing, in a significant part of the fluence range under investigation, the process melts the first 80 nm of the 4H-SiC monocrystal and causes surface rearrangement in a three-layer configuration with a reconstructed SiC at the interface with monocrystalline SiC, followed by a thin Si and C layers. The surface morphology keeps grinding wheel marks still visible; the wafer warpage value is almost unchanged with respect to the value we found on as ground wafer. This means that the process is not acting as a stress relief for damage induced by grinding. Moreover, cracks form, due to fast thermal changes between adjacent regions. The flexural stress of laser treated sample is comparable with the corresponding values found for samples whose backside surface has been treated, after back grinding, with DP or CMP. From a mechanical point of view, the laser annealing process, does not impact die reliability, despite the presence of cracks, representing a suitable back finishing process especially in the optic of its use in backside ohmic contact formation [20] Those findings address the research direction in a way to suitably tailor the laser process to give valid solution as a finishing method for thinned 4H-SiC wafers.

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