Solid State Phenomena
ISSN: 1662-9779, Vol. 359, pp 211-215
doi:10.4028/p-j9uFNJ

Submitted: 2023-09-05
Accepted: 2024-04-10
Online: 2024-08-22

Influence of Active Area Etching Method on the Integrity of Gate Oxide on 4H-SiC

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Keywords: surface roughness, gate oxide, interface state density, dry etching, deep-level transient spectroscopy

Abstract. Etching active area by dry etching method can precisely control the length and width of the devices, but it may damage the SiC surface. In this paper, we fabricated metal-oxide-semiconductor capacitors (MOSC) using different etching methods to compare the effect of etching methods on the SiO_2/SiC interface and dielectric breakdown. It is observed that dry etching will degrade the surface roughness of SiC and the interface state density at the SiO_2/SiC interface. Post-oxidation NO annealing cannot passivate the interface effectively. The breakdown field of gate oxide on the dry etched sample is also degraded. These results indicate that dry etching of SiC surface should be avoided when fabricating MOS devices.

Introduction

Silicon carbide (SiC) with a wide-bandgap characteristic becomes a promising material to replace silicon (Si) in high temperature and high power applications. Surface quality, including step bunching and surface roughness, is an important factor affecting the performance of 4H-SiC devices, especially the gate oxide quality [1-2]. In the fabrication process, active area etching is a process that directly affects the surface roughness. For power MOSFET, the active area is relatively large, usually larger than 1 mm × 1 mm, thus the active area can be defined by wet etching process. In this case, the SiC would not be damaged because typical HF-based oxide etchants do not react with SiC. However, SiC CMOS ICs require small active areas. The lateral etching of wet etching process would result in large deviation of device dimension. However, dry etching has the risk of damage the SiC surface, which would degrade gate oxide integrity.

K. Kutsuki et al. have investigated the effect of surface roughness of trench MOSFETs. Since high density plasma is used to etch trench to precisely control shape and morphology, it inevitably degrades sidewall surfaces and increases roughness. When the surface roughness is higher, the charge-to-breakdown of the gate oxide gradually decreases [2]. Although surface roughness scattering mobility has little correlation with surface morphology and contributes little to total field effect mobility, high surface roughness deteriorates gate oxide reliability which is important for 4H-SiC devices [3]. Furthermore, K. Kawahara et al. have reported that deep levels are generated during reactive ion etching [4]. However, the impact of dry etching induced damages on interface state density after thermal oxidation has not been comprehensively investigated. In this work, we performed a comprehensive study on the influence of active area etching method on the gate oxide quality on 4H-SiC.

Experimental Conditions

Metal-oxide-semiconductor capacitors (MOSC) were fabricated on nitrogen-doped (0001) 4H-SiC substrate with a nitrogen-doped epi-layer. The thickness and the doping concentration of the epi-

layer are 5.5 μm and $1x10^{16}$ cm^{-3}, respectively. A 1000-nm-thick field oxide was deposited on the surface by chemical vapor deposition. After a photolithography process, the active area was opened by two methods, namely wet etching and dry etching. Dry etching was performed using a high-density plasma etcher, while wet etching was performed with a buffered oxide etch (BOE) solution. Next, different conditions of thermal oxidation and nitric oxide post-oxidation annealing (NO-POA) were performed, and the detailed conditions are listed in Table 1. Afterwards, a Ti/TiN/Al stack was sputtered and patterned as the gate electrode. Fig. 1 shows the schematic cross-sectional structure of the fabricated capacitor.

Table 1. Thermal oxidation and post-oxidation annealing (POA) conditions for all samples.

Sample ID	Etching method	Oxidation condition	POA condition	Thickness
D_1200	Dry etching	Dry/1200°C/30 min	1200°C/15 min	23.3 nm
D_1300	Dry etching	Wet/1050°C/4 hr	1300°C/10 min	26.3 nm
W_1300	Wet etching	Wet/1050°C/3.5 hr	1300°C/10 min	24.2 nm

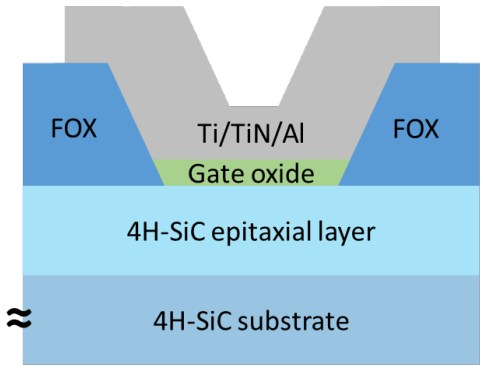

Fig. 1. Schematic cross-sectional structure of the 4H-SiC MOS capacitor used in this work. The active area was wet etched.

Results and Discussion

Figs. 2, 3, and 4 show the high-frequency (HF) at 100 kHz and quasi-static (QS) capacitance-voltage (C-V) characteristics of the samples D_1200, D_1300, and W_1300, respectively. The interface state density (D_{it}) distribution in the band gap near the conduction band extracted by the high-low frequency method is shown in Fig. 5. Looking first at the dry-etched MOSC, the higher the NO-POA temperature, the faster and more the nitrogen atoms diffuse to the interface, and thus the lower D_{it}. However, under the same NO-POA condition, the D_{it} of the dry-etched MOSC is higher than that of the wet-etched MOSC. Therefore, the following discussions are based on the effect of etching methods with similar oxidation and POA conditions, namely the samples D_1300 and W_1300.

Secondary-ion mass spectrometry (SIMS) was used to analyze the nitrogen atoms distribution in samples, as shown in Fig. 6. The concentration of nitrogen atoms at the interface of the dry-etched MOSC is slightly higher than that of the wet-etched MOSC, which does not correspond to the D_{it} distribution. Therefore, there seems to be other reasons why NO-POA does not improve the interface of the dry-etched sample as much as the wet-etched sample.

Since the SiC surface may be damaged by ion bombardment during dry etching, atomic force microscope (AFM) was used to examine the effect of dry etching on the SiC surface. The metal and oxide layers above the SiC surface were removed prior to AFM measurement. As shown in Fig. 7, the root mean square roughness of the dry-etched sample is higher than that of the wet-etched sample. The higher roughness of the dry-etched sample implies that the higher D_{it} of the dry-etched MOSC may originate from the defects generated by the etching process.

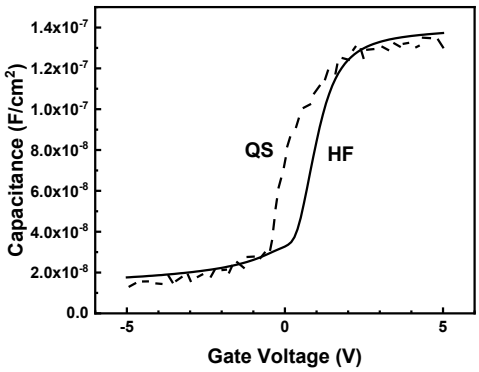

Fig. 2. High frequency (HF) and quasi static (QS) capacitance-voltage (C-V) characteristics of the sample D_1200.

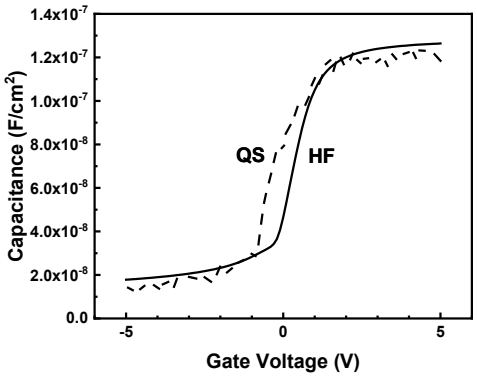

Fig. 3. High frequency (HF) and quasi static (QS) capacitance-voltage (C-V) characteristics of the sample D_1300.

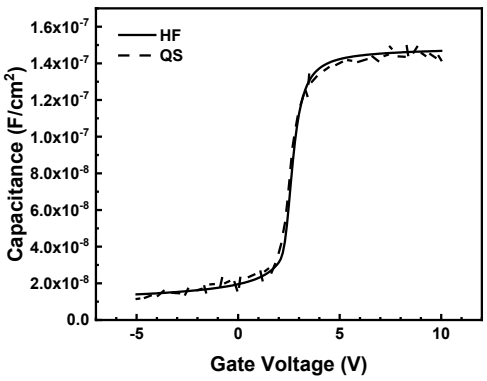

Fig. 4. High frequency (HF) and quasi static (QS) capacitance-voltage (C-V) characteristics of the sample W_1300.

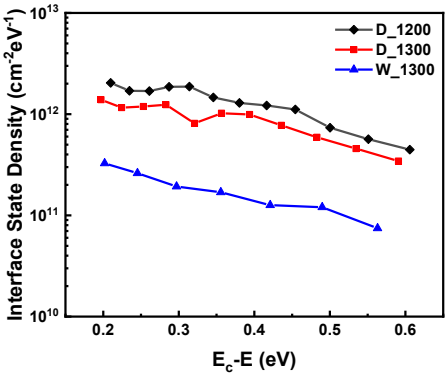

Fig. 5. Interface state density (D_{it}) distribution for all samples.

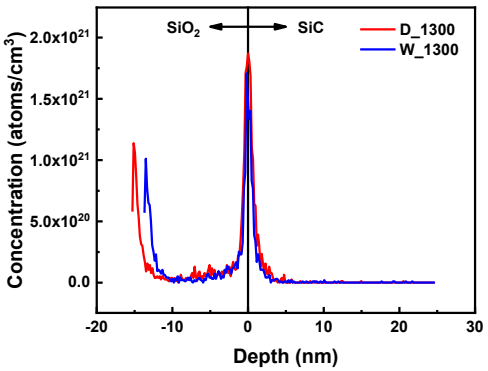

Fig. 6. Nitrogen concentration depth profiles measured by SIMS.

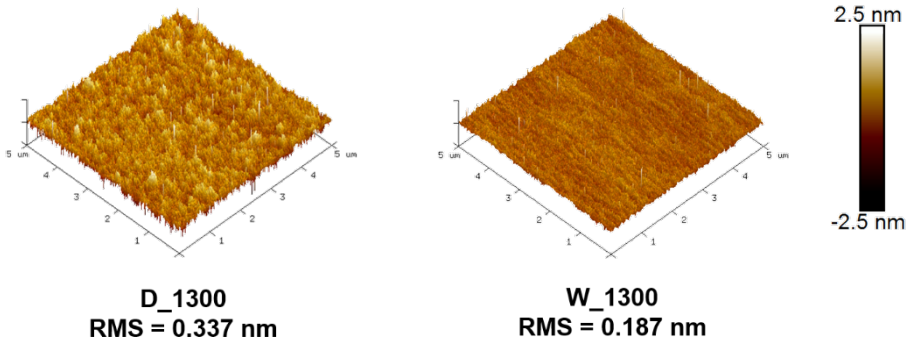

Fig. 7. Atomic force microscopic morphology of the Si surface after gate oxide remove.

Defects types were investigated using deep-level transient spectroscopy (DLTS), with the measurement parameters listed in Table 2. As shown in Fig. 8, the DLTS spectrum of the dry-etched MOSC has two major peaks, one at around 200 K and the other at around 330K. The peak at around 200K is a broad peak made up of multiple defects, resulting from interface states generated through thermal oxidation [5]. The peak at around 330K is most likely EH_4 center and IN5 center [6, 7]. Additionally, a small signal at 400 ~ 500K may correspond to $RD_{1/2}$ center and IN6 center [6, 8]. On the other hand, the DLTS spectrum of the wet-etched MOSC shown in Fig. 9 only has a noticeable peak at around 200K. As a result, DLTS measurements reveal that dry etching damages the surface and generates defects, potentially leading to a higher interface state density, even under similar oxidation and NO-POA conditions.

Table 2. DLTS measurement parameters.

Sample ID	Flat band voltage	Reverse voltage	Pulse voltage	Pulse width	Period width
D_1300	0.81 V	0 V	2 V	100 μs	199.68 ms
W_1300	3.24 V	2.5 V	4.5 V	100 μs	199.68 ms

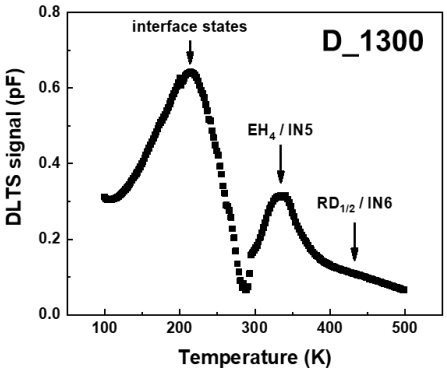

Fig. 8. DLTS profile of the dry-etched sample D_1300.

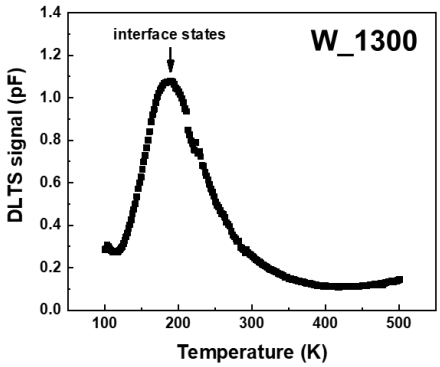

Fig. 9. DLTS profile of wet-etched sample W_1300.

Fig. 10 shows the current-voltage characteristics of the samples D_1300 and W_1300. These two samples have the same breakdown voltage. The barrier heights of Fowler-Nordheim tunneling are 2.68 eV and 2.85 eV for D_1300 and W_1300 at room temperature. These results indicate that the dry-etching induced degradation of surface roughness does not affect the breakdown field but the defects near the interface enhanced the F-N tunneling current which would degrade gate oxide reliability.

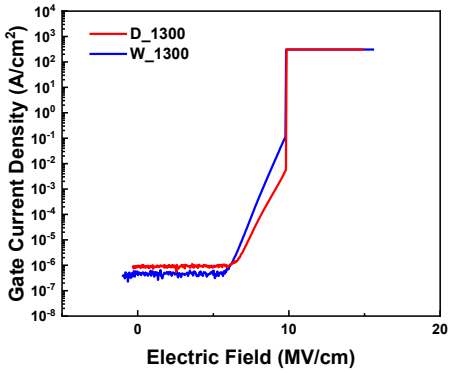

Fig. 10. Current-voltage characteristics of the samples D_1300 and W_1300.

Summary

According to the above results, the dry etching method can result in a higher interface state density compared to the wet etching method, even under similar NO-POA conditions. This is due to the damage to the surface, which leads to increased roughness and the generation of defects. Therefore,

it is recommended to avoid dry etching when opening the active area of MOSFETs, or to use an additional process such as sacrificial oxidation after dry etching the active area to remove the defect layer caused by dry etching.

Acknowledgement

This work was supported by the National Science and Technology Council, Taiwan, R. O. C. under the contract No. MOST 110-2218-E-A49-008 and MOST 111-2218-E-A49-020. Samples were processes by the Episil Precision Inc.

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