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High-k Gate Dielectric for High-Performance SiC Power MOSFET Technology with Low Interface Trap Density, Good Oxide Lifetime (t_{tddb}≥ 10^4s), and High Thermal Stability (≥ 800 ºC)

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Abstract: In this work, we demonstrate SiC/high-κ MOS capacitors with low leakage density of 10^{-8} Acm^{-2}, good device uniformity, good thermal stability (> 800 °C), and longer oxide lifetime > 10^4 s simultaneously. This is enabled by using atomic layer deposition (ALD) processed- HfAlO as the gate dielectric with a thickness of 35 nm, smooth surface (RMS roughness =0.70 nm), and high-quality SiC/ HfAlO interface with interface density (D_{it}) of 8×10^{10} $eV^{-1}cm^{-2}$.

Introduction

Silicon carbide (SiC) MOSFETs technology is the foremost candidate to substitute conventional Si-IGBT technology due to their higher breakdown voltage and high thermal conductivity [1,2]. Despite their successful market product, several issues associated with advanced metal gate stack technology remain to be solved to fully exploit the enormous potential of SiC power MOSFETs. Performance and reliability are significantly impacted by the highly defective thermal oxide/SiC interfaces, high-temperature process, and the strong electric field across the conventional SiO_2 gate oxides [3,4]. Therefore, it becomes essential to develop alternative gate dielectrics with superior interfacial quality, reduced electric flux discontinuity, and a low thermal budget process, which is an important factor for better performance achievement. Hafnium aluminum oxide (HfAlO) gate dielectric has been effectively investigated in the scaling of Si-CMOS technology owing to its high-k value, large band gap, and high crystallization temperature (≥ 800 °C) [5]. Such superior properties are also desired in a high-κ gate dielectric to swap the traditional SiO_2 in SiC power technology.

In this paper, the gate dielectric growth via atomic layer deposition (ALD) with different scheme of the HfAlO gate dielectric layer has been implemented on (0001)4H-SiC substrates at a low deposition temperature of 300 °C. The results show that the device performance was significantly improved such as least hysteresis, lowest interface trap density, and good oxide lifetime using in-situ O_2 plasma.

Results and Discussion

The 4° off-cut (0001) Si-face of 4H-SiC was used for fabricating the MOS capacitors, and a 10 µm thick N-doped homo-epilayer was formed on a highly doped n-type substrate. The deposition conditions of the ALD high-κ gate dielectric HfAlO are listed in Fig. (1). The high- κ films are in-situ treated with either ozone or oxygen plasma.

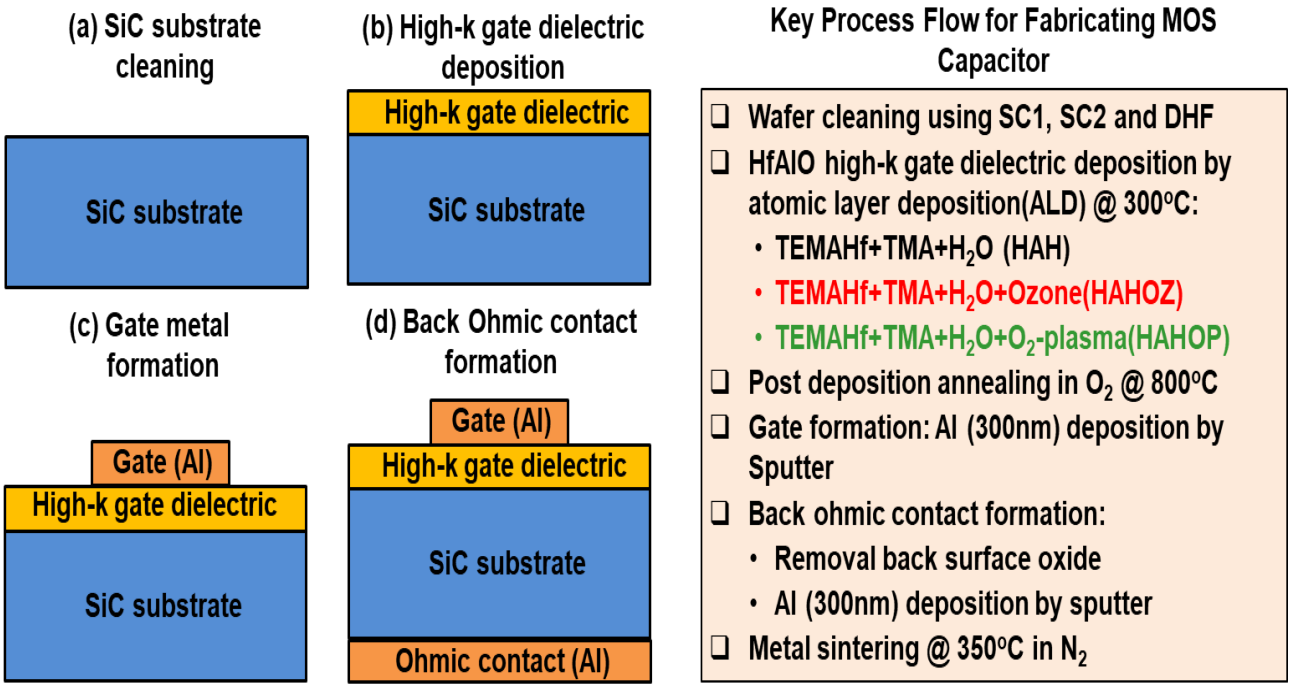

Fig. 1 (a-d) Illustration of fabricated MOS capacitors. The sample conditions are designated as follows, henceforth: TEMAHf+TMA+H_2O (HAH), TEMAHf+TMA+H_2O+Ozone (HAHOZ), TEMAHf+TMA+H_2O +O_2-plasma (HAHOP, control sample) and key process flow of MOS capacitors fabrication.

Fig. 2(a), shows the gate leakage density (J_G) plotted as a function of V_G, which may be used to interpret the HfAlO gate dielectric film quality. Samples that underwent *in-situ* oxygen (O_2) plasma treatment during ALD growth demonstrated significantly improved gate leakage current behavior with no trap-assisted leakage up to the trigger of FN tunneling at 5.8MVcm^{-1}. The *in-situ* O_2 plasma also showed near-ideal capacitance-voltage (*C-V*) behavior with low hysteresis and reduced flat-band voltage values, indicating a clear reduction of the interface and bulk trap charges (Fig. 2(b)). As-deposited, and *in-situ* ozone treatments are not discussed any further here due to their inferior performance.

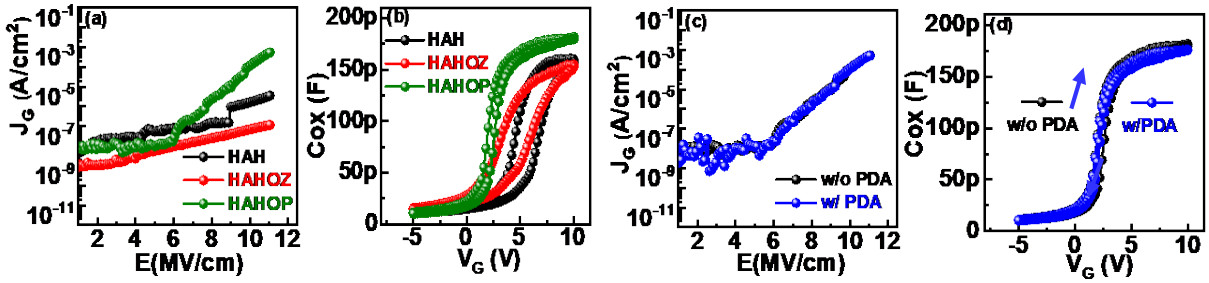

Fig. 2 (a) J_G -V_G for the MOS capacitors (b) Typical C_{ox}-V_G double sweep curves of the MOS capacitors (c) J_G -V_G for the MOS capacitors (control device (HAHOP) w/o PDA and w/PDA in O_2 at 800 °C and (d) Typical C_{ox}-V_G double sweep curves of the MOS capacitors w/o PDA and w/PDA in O_2 at 800 °C gate dielectric(control device HAHOP).

We carried out a set of post-deposition annealing (PDA) experiments in an O_2 environment at 800°C to examine the thermal stability of the gate dielectric. Unnoticeable changes in J-V and C-V behaviors, as shown in Fig (2c) and (2d), respectively, confirmed that deposited HfAlO high- κ films with *in-situ* O2 plasma treatment are thermally stable up to 800°C. Indeed, it has been found that the devices exhibit mildly improved hysteresis after PDA, attributed to further reduction of trap charges. To examine the device uniformity, HAHOP devices were randomly selected and measured. Excellent device-to-device uniformity was obtained for PDA devices (Fig. 3(a)).

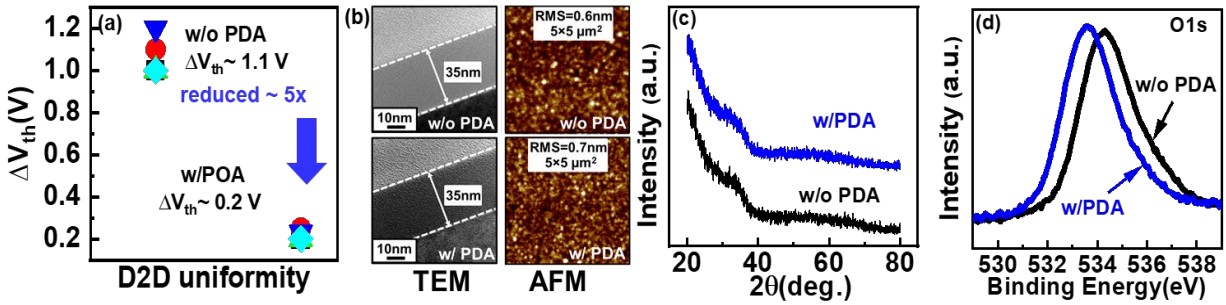

Fig. 3 (a) Distribution of gate leakage density for randomly selected devices (b) Cross-sectional TEM and AFM images (c) XRD patterns and (d) O1s XPS spectra of gate dielectric with and without PDA.

Atomic force microscope (AFM) characterization was carried out to investigate the surface morphology of the gate dielectric. The post-PDA RMS roughness of 0.70 nm is quite comparable to pre-PDA value of 0.6nm, indicating that PDA in O_2 is not adversely affecting the surface morphology of the gate dielectric (Fig. 3(b)). Next, high-resolution transmission electron microscopy (HRTEM) images were acquired for both samples to examine the existence of additional layers at the SiC/HfAlO interface after PDA. As shown in Fig 3(b), no additional layer was observed after PDA, implying that the PDA in the O_2 process only affects the gate dielectric trap charges and not the physical morphology (no oxidation of SiC surface). Fig. 3(c) shows the XRD data of HfAlO film. No apparent crystalline peaks after PDA in O_2 at 800 °C is an indication of good thermal stability of the deposited HfAlO gate dielectric.

To confirm the influence of PDA on the oxygen composition of the gate dielectric, the X-ray photoelectron spectroscopy (XPS) data of the gate dielectric layer was analyzed (Fig. 3(c)). With PDA in O_2, the O-1s peak has shifted to the lower binding energy which is attributed to fewer oxygen vacancies. The reduction of oxygen vacancies during the O_2 treatment improves trap density [6]. The D_{it} is extracted using the high-low method as shown in Fig. 3(d). Fig 4(a) shows the gate oxide lifetime of the MOS capacitors studied by the constant voltage time-dependent dielectric breakdown test, which was conducted to assess the impact of PDA treatment. The gate oxide lifetime extrapolates to $>10^4$ s at a stress bias corresponding to the oxide field of 7 $MVcm^{-1}$ at room temperature. Table -1 benchmarks the key parameters of our work with other reports, achieving the best performance of all published high-κ gate dielectrics-based SiC devices.

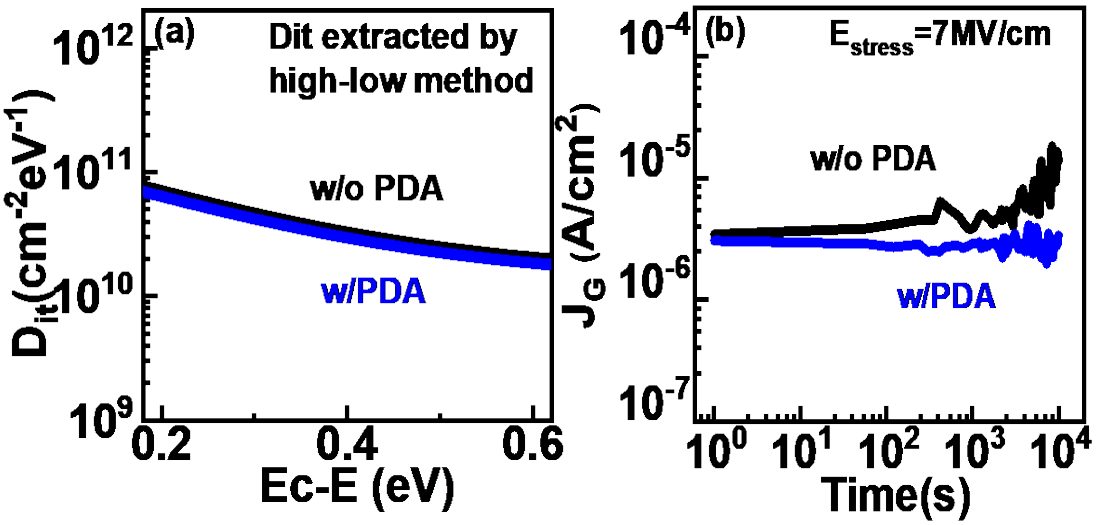

Table-1	Gate Dielectric (ALD)	Hysteresis (V)	Dit ($cm^{-2}eV^{-1}$)	Oxide lifetime (s)
This work	HfAlO(35nm)	0.20	8×10^{10}	$> 10^4$
Ref-7	HfO_2/Al_2O_3(30nm)	1	-	-
Ref-8	AlN(44.4nm)	-0.21	4.2×10^{12}	-
Ref-9	SiO_2(28nm)	0.18	2×10^{11}	-
Ref-10	Al_2O_3(13nm)	-	5×10^{11}	-

Benchmark

Fig. 4 (a) D_{it} extracted by the high-low method for the MOS capacitors (b) Time to breakdown for the MOS capacitors at forward stress of 7 MV/cm at room temperature and Comparision of various key parameters of our high-k gate dielectric-based SiC work with those in previously reported (Table-1).

Conclusion

In this work, we have presented the effect of *in-situ* O_2 plasma on the growth of ALD processed-HfAlO high-κ gate dielectric. We observed that the combination of H_2O+ *in-situ* O_2 plasma treatment and PDA in oxygen is an efficient way to improve the quality of high-k gate dielectric. These results suggest that HfAlO high-κ gate dielectric is a potential candidate for advanced SiC power MOSFET technology.

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