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Lift-Off Process for Patterning of a Sputter-Deposited Thick Metal Stack for High Temperature Applications on 4H-SiC

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Abstract. With the rising need for power devices suitable for harsh environment conditions like high temperature applications, contact materials and packaging of the devices have become critical factors in device fabrication [1, 2]. Therefore, a contact metal stack containing silver and titanium nitride which can be used at elevated temperatures under oxygen atmosphere was investigated. For patterning of the approx. 2 µm thick sputter-deposited metal stack on the wafer front side, a lift-off process using a negative photoresist was established. Characterization of the photoresist sidewall shape was performed by cross-sectional views prepared with SEM and top view images taken on a microscope. It was found that for a successful lift-off, a distinct undercut is needed so no metal is deposited at the downside of the undercut, ensuring a metal-free surface for the solvent to reach the photoresist. To obtain this, most influencing factors are exposure dose and development time, which were optimized considering the undercut shape as well as pattern fidelity. Lift-off with acetone proved to be good for the fabricated 4H-SiC MOSFET devices.

Introduction

With its properties such as wide bandgap and high thermal conductivity, silicon carbide (SiC) shows essential benefits in high power or high temperature applications for electronic devices exposed to harsh environment conditions [1]. In addition to the semiconductor material, the other components of the device, especially the contact metallization, also have to be stable at the operating conditions. Not only the temperature but also other factors like gases from the environment (e.g., oxygen, nitrogen, etc.) or humidity must be considered. Therefore, the metallization must have a high reliability at elevated temperatures while acting as a diffusion barrier at the same time [3].

To meet these requirements, a metal stack of silver (Ag), titanium nitride (TiN) and another Ag layer with a total thickness of approx. 2µm was investigated at IISB. Besides their high melting points, Ag is well suited as a contact metal due to its low electrical resistivity, corrosion resistance and sintering abilities whereas TiN acts as a suitable diffusion barrier at elevated temperatures [4, 5]. In this work, the given metal stack was applied on 4H-SiC MOSFET devices, which were also fabricated at IISB. Sputter deposition was chosen to apply the metal stack on the semiconductor as previous investigations have shown that sputtered metal layers did show better adhesion compared with corresponding evaporated ones. To investigate the metal stack in terms of high temperature stability and diffusion barrier capability, the metallized 4H-SiC MOSFET devices were subjected to a temperature treatment up to 400 °C under oxygen atmosphere.

To pattern the metal stack on the wafer front side in order to form the MOSFETs gate and source contacts, a lift-off process was applied due to several advantages compared to dry or wet metal etching. In general, the selectivity for etching processes must be high enough to avoid over-etching so that no other important elements of the MOSFET are removed, while for lift-off only an organic solvent is used to pattern the metal stack making the process more gentle to the surfaces in contact.

The isotropy, i.e. non-directional material removal, of wet etching, which leads to an under-etching of the etching mask, and low etching rates during dry etching are other disadvantages compared to lift-off [4]. Furthermore, the photoresist mask must be thick enough not to be etched away during dry etching or to serve as a diffusion barrier for the wet etch chemicals.

For lift-off, the photoresist is dissolved after metallization so the metal on top of the resist mask is lifted simultaneously. Compared to evaporation, where the metal is deposited in one spatial direction, sputter deposition is not a directional process, resulting in the metal being deposited on the resist sidewalls as well which inhibits the dissolution of the photoresist. To overcome this problem, an undercut profile, which can be derived with image reversal or negative-tone photoresists, can be beneficial. Another approach is a bilayer-lithography, where the upper resist layer can be a conventional positive-tone photoresist becoming developable at exposure with a photomask while the lower resist layer is completely soluble in developer. Therefore, during development the exposed regions of the upper resist layer and the underlying resist layer dissolve at once, resulting in a step profile depending on the grade of over-development. However, problems such as intermixing of the resist layers during the second coating step and additional necessary process steps lead to a higher process complexity [6]. Furthermore, the step height must be high enough so that the metal does not fully cover the step profile for a successful lift-off.

Experiment

Processing. For these reasons and to simplify the process, a negative-tone photoresist (AZ® LNR-003 [7]) with a thickness of approx. 5.1 µm after spin coating was used in this work. The measured dark erosion was approx. 70 nm, so the resist thickness after lithography amounts to approx. 5 µm. The exposure was performed at a Mask Aligner from Suss MicroTec (MABA6 or MABA8) with the aim to solely expose the upper part of the resist. Different exposure doses were tested by variation of exposure time. Furthermore, exposure with and without an i-line filter, which filters light with a wavelength above the i-line (365 nm), were tested. With i-line filter, the exposure energy is reduced, and therefore the exposure time must be increased to reach a similar exposure dose. The illuminated parts of the photoresist cross-link at the following post exposure bake at 100 °C, so that during development the non-crosslinked photoresist parts are dissolved and an undercut profile is formed depending on the light dose distribution inside the photoresist and development time.

Before the following metallization, the wafer surface was prepared with a short dip in buffered hydrofluoric acid (BHF) and a sputter etch step to etch away native oxide. The metallization was performed at a sputter deposition tool from Evatec process systems (CLN 200 II). Temperatures during sputter deposition were up to approx. 185 °C.

For lift-off, one wafer was put in a crystallizing dish with acetone lying in an ultrasonic bath. Acetone is used as solvent as it dissolves photoresists easily and the solvent must not contain sulfurous groups since these react with Ag and form non-conductive Ag_2S [8]. After 15 min treatment in the ultrasonic bath, the wafer was rinsed with deionized water to flush residues of metal and resist. This procedure was repeated several times until the lift-off result was satisfactory, which took up to 4 h in total.

Characterization. For verification of the resist thickness, measurements were carried out on a reflectometer from K-mac (ST5030-SL). Top-view images of the wafers were taken on a microscope from Nikon (Eclipse L200). For cross-sectional views of the wafers, scanning electron microscope (SEM) images were taken. For Si, the wafer was broken for imaging while for SiC the cross-section was prepared with focused ion beam (FIB). Here, a platinum (Pt) layer was deposited as a protection before cutting to prevent surface destruction before taking the images. Silicon (Si) cross-sections were taken on a SEM from Jeol (JSM-7610F), and for SiC a FIB tool from Thermo Fisher Scientific, formerly FEI (Helios Nanolab 600), was used.

As SEM cross-sectional images are destructive and preparation is time consuming, only a representative number of samples were characterized with cross-sectional views. Fig. 1 shows two examples of cross-sectional images and corresponding top-view images. Both examples show the photoresist mask on bare Si wafers, where exposure was carried out with an i-line filter. The structure

shown in Fig. 1 (a) and (c) was obtained with an exposure dose of approx. 150 mJ/cm^2, while the structure shown in Fig. 1 (b) and (d) was obtained with an exposure dose of approx. 160 mJ/cm^2. In the top-view images, the linewidth at the resist – wafer interface can be identified easily, as well as the undercut. The top linewidth is slightly harder to see, as it seems that the distinct shape of the photoresist, also called T-top, creates a shade on the wafer surface. The edges at the bottom of the T-top are harder to see from a top view, as can be derived from Fig. 1 (a) and (c), where not all the edges visible in the cross-section are visible in the top-view image. Therefore, for the evaluation of the lithography results the linewidth at the resist – wafer interface and the overall undercut was considered in particular.

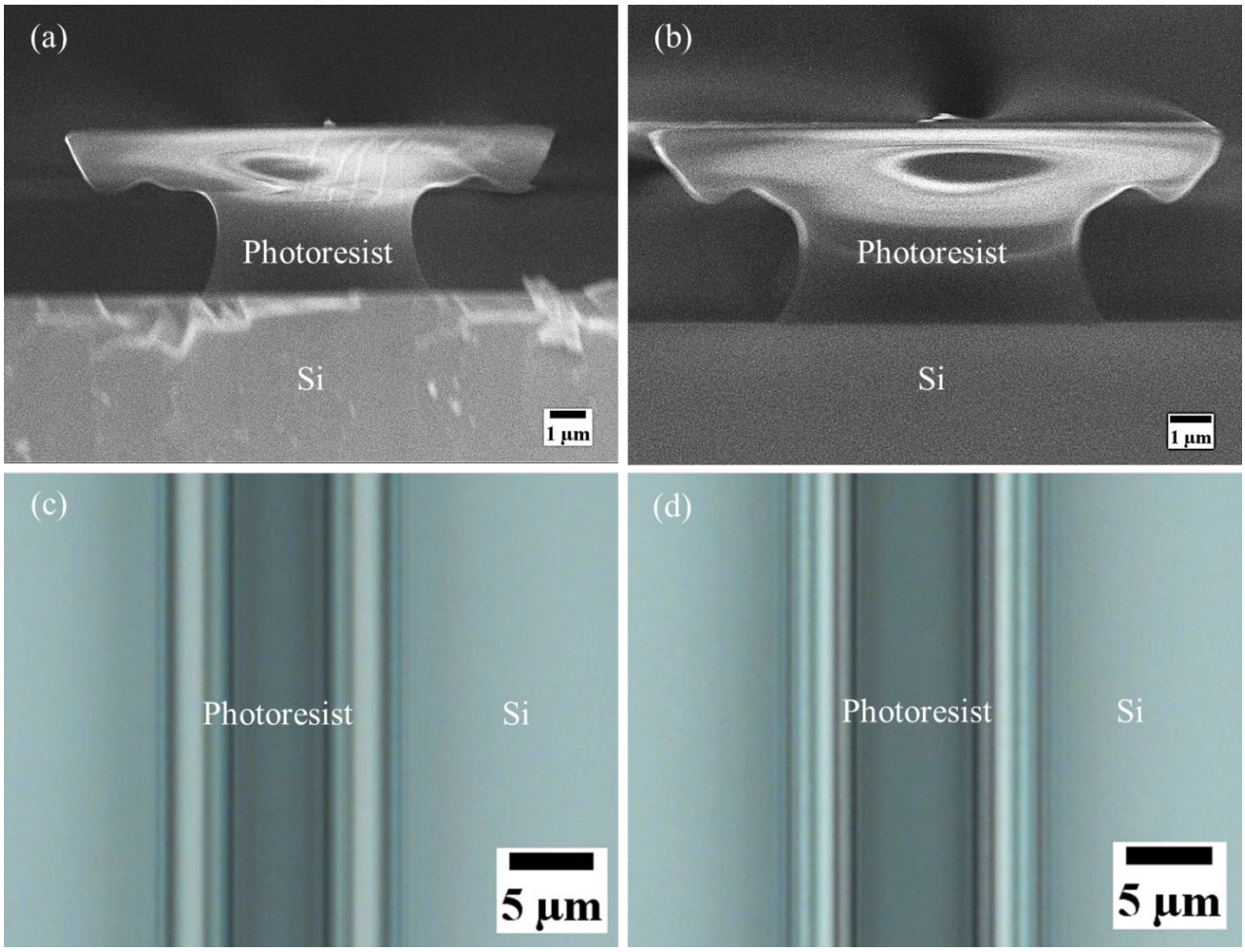

Fig. 1. SEM cross-section images (a, b) of photoresist after lithography and corresponding top-view microscope images (c, d) on bare Si. Exposure in (a), (c) was performed with an exposure dose of approx. 150 mJ/cm^2 and in (b), (d) with approx. 160 mJ/cm^2 using an i-line filter.

Electric characterization of the SiC MOSFET devices was carried out after front side and back side metallization and before temperature treatment on a wafer prober from FormFactor, formerly Suss (PA200). Electrical measurements on forward and blocking characteristics were carried out.

Results

Lithography. To create a distinct undercut in the negative photoresist, studies on the exposure dose and development time were carried out. Furthermore, the influence of the wavelength of light during exposure was investigated by performing exposure with broadband (g-line, h-line and i-line) and only i-line (365 nm). As the used photoresist is solely sensitive for i-line, only the back-reflection on the wafer surface and resulting interference of the UV-light and therefore dose distribution inside the photoresist causes the difference during exposure.

Fig. 2 shows SEM images of cross-sections through the photoresist. In Fig. 2 (a) an exposure dose of approx. 180 mJ/cm^2 was applied and the exposure was performed with broadband illumination, while in Fig. 2 (b) an i-line filter was used. Here, the exposure dose was approx. 150 mJ/cm^2. In comparison, in Fig. 2 (c) the photoresist profile on SiC after exposure with broadband illumination with an exposure dose of approx. 180 mJ/cm^2 is shown. One can see that the resist sidewall profile with i-line illumination and lower exposure dose on Si in Fig. 2 (b) shows not only a higher undercut height, but also a notch at the bottom of the T-top. For SiC, the photoresist profile is comparable to the one on Si shown in Fig. 2 (b) also without use of the i-line filter and higher exposure dose, which is assumed to be due to the lower back-reflection of light on the SiC surface [9,10].

Fig. 2 (d) depicts the cross-section after sputter deposition of Ag with a target thickness of 1 µm, TiN with a target thickness of 0.2 µm and another Ag layer with a target thickness of 0.5 µm. While some metal is deposited underneath the undercut, no metal is deposited at the notch on the downside of the T-top, making the distinct undercut profile the key factor for lift-off performance. Furthermore, with decreasing height of the undercut, the distance of the lowest point of the T-top to the wafer surface decreases, so the thickness of metal that can be deposited while leaving a space for the solvent to reach the photoresist surface also decreases. Thus, the higher the undercut height, the higher can be the liftable metal thickness.

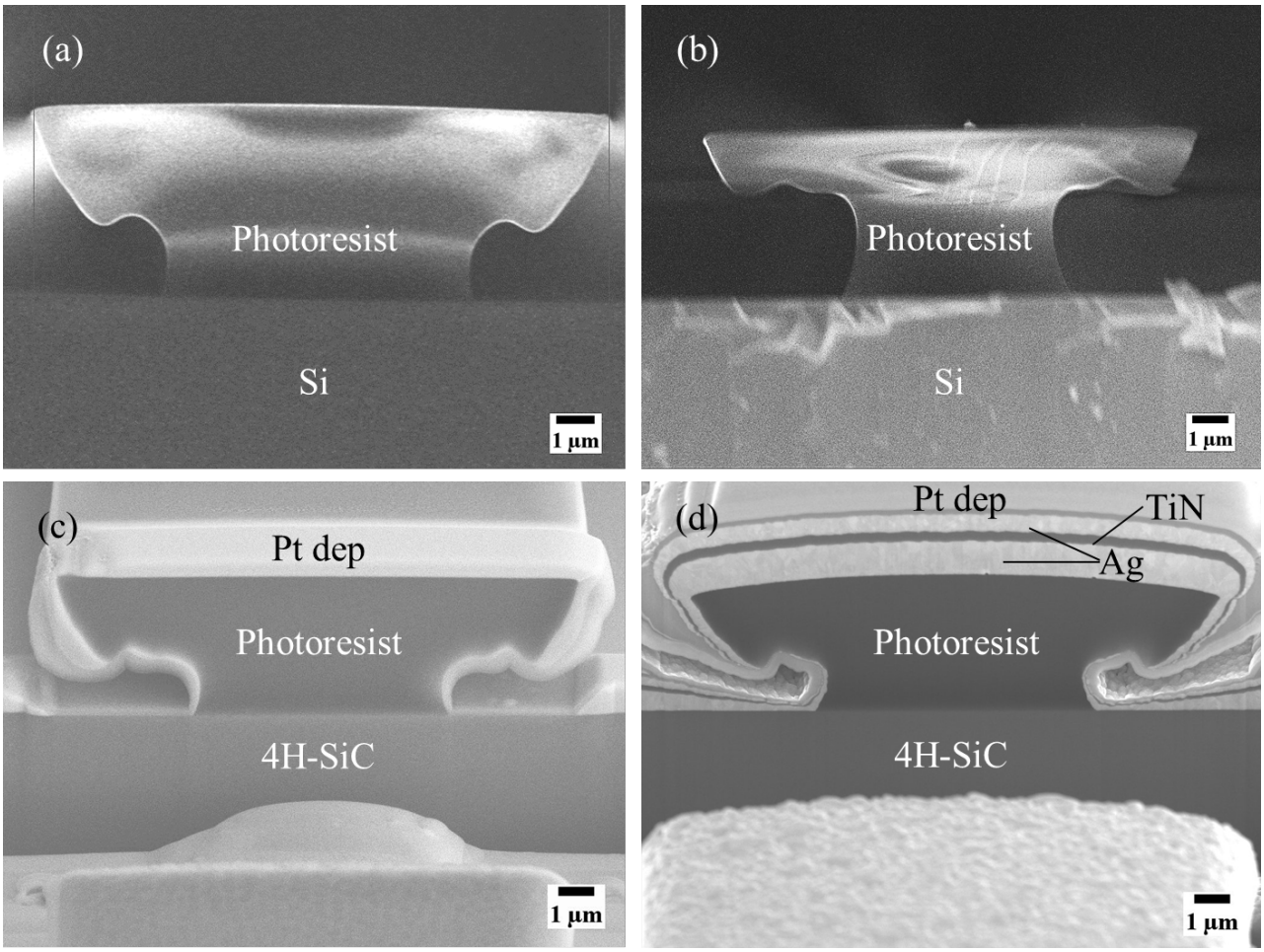

Fig. 2. SEM cross-sectional images of photoresist after lithography on bare Si without i-line filter and exposure dose of 180 mJ/cm^2 (a) and with i-line filter and exposure dose of 150 mJ/cm^2 (b). SEM cross-sectional images, prepared via FIB and covered by an in-situ deposited Pt layer, on bare SiC after lithography without i-line filter and exposure dose of 180 mJ/cm^2 (c) and with the deposited metal stack of 1 µm Ag (lower layer), 0.2 µm TiN and 0.5 µm Ag (upper layer) on top (d).

In Fig. 3 the linewidths of 15 µm structures (as drawn on the mask) on top of the resist, on the resist – wafer interface and the resulting undercut width are shown for a variation of exposure doses for an over-development time of 8 s. The depicted linewidths are taken from the middle of the wafers, but the uniformity over 150 mm wafers was good with linewidth variations of under 10 %. The development time was tested before, and showed best results for 8 s over-development, which means development was stopped 8 s after the non-exposed resist was developed visibly. This parameter was considered rather than total development time, as the time needed for development showed little variations which could be due to temperature fluctuations or developer consumption. For development, one would expect an increasing undercut width with increasing over-development time, while the top linewidth should be independent of development time. For tested over-development times, no dependence could be seen for the top linewidth as well as for the undercut width, which can be due to measurement errors, because the undercut could not be determined exactly from microscope images as depicted above. Additionally, as over-development time cannot be too long as the resist could lift off completely, the range of tested over-development times was limited.

For the variation of exposure doses, one can see that the top linewidth increases with increasing dose, while the undercut decreases, as expected due to the dose distribution. Furthermore, the measured linewidths on the resist – wafer interface are lower for SiC compared to Si, which confirms the lower back-reflection on the SiC surface. However, these measurements could contain the described measurement errors as well. To achieve a good pattern fidelity while creating an adequate undercut, an exposure dose of approx. 170 mJ/cm^2 was found as an optimum.

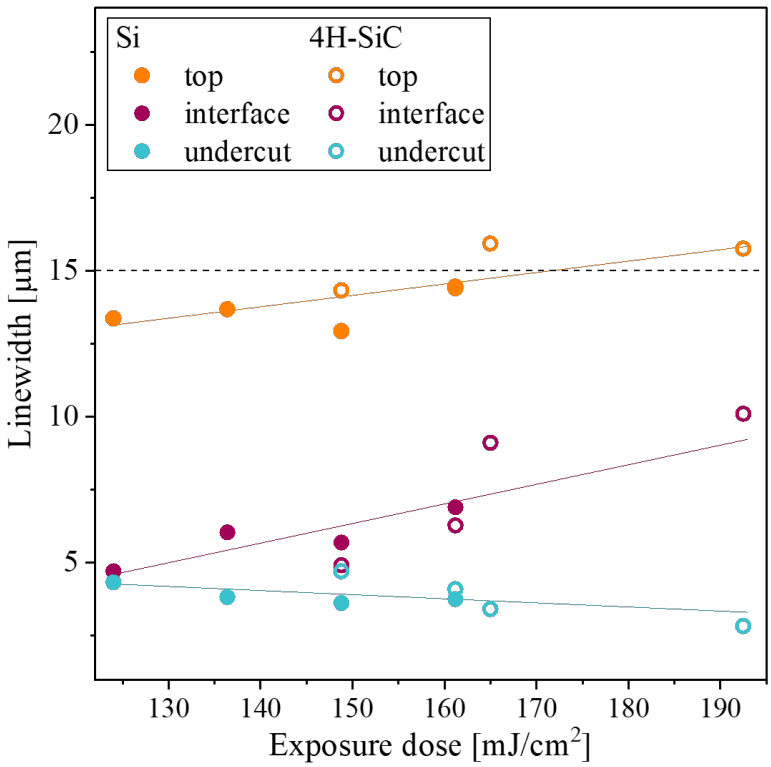

Fig. 3. Linewidths (target: 15 µm) on top of the resist, on the resist – wafer interface and resulting undercut width plotted over exposure dose for an over-development time of 8 s. Measurements were taken from microscope top-view images.

Lift-off. Fig. 4 (a) shows the described negative-tone lithography on a 4H-SiC MOSFET device. The gate runner, which is the critical structure that must be lifted off, in this device has a target linewidth of 15 µm. In Fig. 4 (b) the result after lift-off is depicted. The gate runner and the sawing lines could be structured with the presented lithography. The linewidth of the gate runner after lift-off is approx. 8 µm as the metal is deposited also underneath the undercut. Therefore, to obtain larger

linewidths, the photomask can be adjusted by adding the undercut dimension, which is a standard procedure for lithography with negative-tone photoresists.

After lift-off, an optical control revealed that on approx. 10 % of the devices the gate metallization also lifted off. Therefore, the metal adhesion could be improved by addition of a thin adhesion-enhancing metal layer in the future. As with the described resist thickness and optimum exposure dose and development time, the distance between the lowest point of the T-top and the surface should be high enough so the metal thickness can be increased further.

Moreover, some resist residues remained on the wafer, which is assumed to be due to thermal crosslinking during metal deposition. As this was not problematic here, for the photoresist is an insulating material, no further treatments have been applied. To overcome the problem, a following plasma ashing step could be applied, for instance.

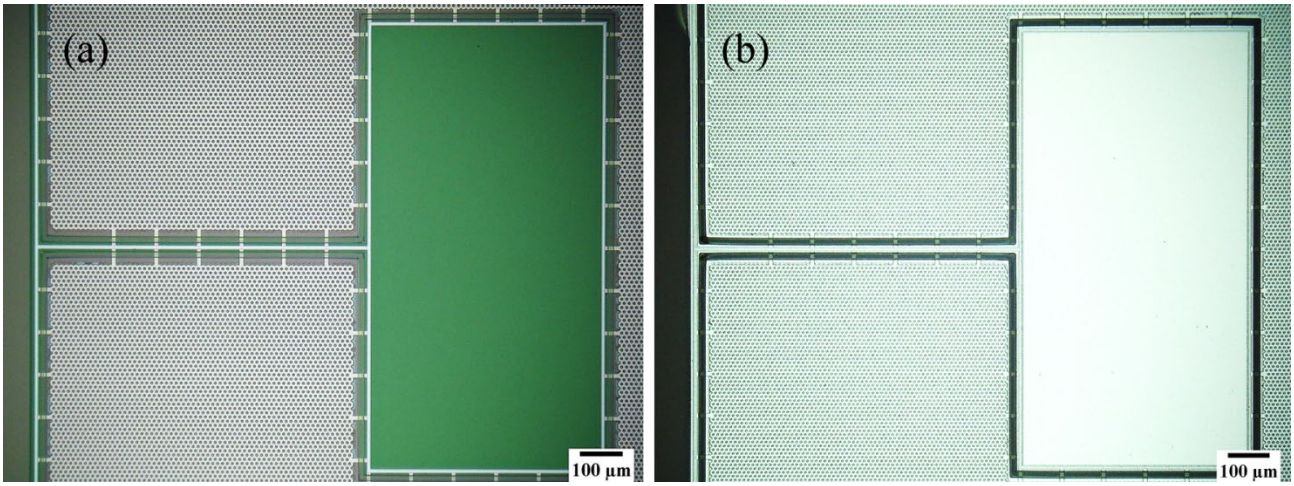

Fig. 4. Top-view microscope image of a 4H-SiC MOSFET device after lithography (a) and after lift-off with acetone (b). Critical structures that must be lifted off are the gate runner around the gate pad, on the right side of the images with a target linewidth of 15 µm, and sawing lines between the devices, on the utmost left side of the images.

Device characterization. For a yield analysis on the fabricated MOSFET devices, electrical measurements of the devices can be considered. The yield map gives an indication on successful metal stack structuring, however other issues in the device fabrication could lead to device failures as well. Concerning forward measurements, 74 % of the devices on the wafer shown above have a sufficiently small gate leakage and $R_{DS,\,on}$. This leads to the conclusion that the metal stack was successfully deposited and structured on at least 74 % of the devices as well.

Summary

As a summary, 4H-SiC MOSFET devices with an approx. 2 µm thick sputter-deposited metal stack composed of Ag and TiN were fabricated. For patterning of the front side metallization, investigations on a lift-off process with a negative-tone photoresist were carried out. Optimization of lithography parameters led to a distinct undercut in the photoresist in shape of a T-top which enables proper lift-off. Here, the undercut height as well as the shape of the T-top play a major role, which was demonstrated by cross-sectional images. Depending on the undercut height or the total resist thickness, respectively, even thicker layers of sputter-deposited metal are assumed to be liftable.

Concerning yield, an optical control of the wafer after lift-off showed that on approx. 10 % of the devices metal adhesion problems occurred. Therefore, the contact metal materials can be optimized concerning metal adhesion after lift-off as well as after treatment at elevated temperatures under atmosphere in further investigations. The overall yield was confirmed by electrical characterization which revealed 74 % device functionality.

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