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3rd Quadrant Surge Current SOA of SiC MOSFETs with Different Voltage Class

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Abstract. The aim of this work is to investigate the 3rd quadrant safe operating area (SOA) of different voltage class SiC MOSFETs under surge current conditions depending on the gate-source voltage. The extent to which an applied gate-source voltage can influence the surge current capability was investigated. For 650 V and 1.2 kV voltage class devices, surge current capability was higher with channel-on mode. However, this behavior was vice-versa for 2 kV and 3.3 kV devices. In this investigation, during the surge current event, the gate-source voltage was switched between different values to optimize the resulting voltage drop. This method can reduce power dissipation during a surge current event, especially for high voltage class SiC MOSFETs.

Introduction

The surge current capability of SiC MOSFETs is gaining more importance in applications where special fault conditions can occur, such as in active short-circuit (ASC), with a 3 phase permanent magnet synchronous motor (PMSM) as load. Further, grid-connected converters can suffer from special failure cases where a surge current capability is required. Due to the internal structure of a SiC MOSFET, it is possible to use the body diode in 3rd quadrant operation (channel-off mode), e.g., as a freewheeling diode during dead time. The additional possibility of operating the device in the 3rd quadrant by applying a positive gate-source voltage V_{GS} (channel-on mode) to bypass the pn-junction, at least below a certain current density level at which it activates again, provides an additional degree of freedom. In various publications the surge current capability of SiC MOSFETs has been investigated. There are many publications on 1.2 kV SiC MOSFETs body diodes in surge current mode [1] as well as on high-blocking SiC MOSFETs up to 6.5 kV [2]. However,there is none describing different voltage classes with comparable technology.

In this work, the focus is on the study of the surge current capability of different voltage class SiC MOSFETs in 3rd quadrant depending on the applied V_{GS}. This study also explores how to optimize the behavior of a device during a surge current event to reduce stress on it and potentially increase its safe operating area (SOA).

Measurement Setup and Methodology

To investigate the surge current capability of SiC MOSFETs in 3rd quadrant, a measurement setup described in [3] was used. The surge current capability was determined by gradually increasing the surge current amplitude $\hat{I}_{FSM}$, till the device under test (DUT) failed or a static electric parameter indicated the imminent destruction of the device. The investigation was carried out on devices from Infineon in the voltage class range of 650 V to 3300 V with comparable trench MOS-cell technology (see Figure 1). For better comparison, all DUTs chosen were in the TO-247-4 housing package and had similar assembly and interconnection technology (AIT). However, the AIT used is not representative for the actual AIT used in the application. Measurements were taken at $t_{Surge} = 10$ ms and at $T_{initial} = 25$°C and

150°C. Initially, for all devices, a positive V_{GS} of 18 V was applied to ensure that the n-channel was fully open. Then, a V_{GS} of -10 V was applied to fully close the n-channel to get a bipolar current flow through the device. Two devices per voltage class were measured at each condition.

The main difference in the chosen DUTs was the voltage class, and thus the thickness of the drift region. With increase in voltage class of the devices, the drift region must be dimensioned thicker and the doping density of the drift region reduced to achieve higher blocking voltages. These measures lead to an increase in the specific resistance $R_{drift,sp}$ of the drift zone of the device. The dependence of the specific resistance $R_{drift,sp}$ of the drift zone on the blocking voltage V_{BD} based on unipolar SiC-limit can be expressed by the following equation [4]:

$$R_{drift,sp} = 2.95 \cdot 10^{-11} V_{BD}^{2.28}\ \Omega\,cm^2 \quad (1)$$

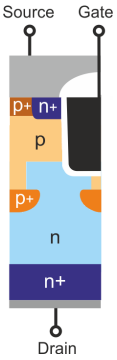

Fig. 1: Schematic cell structure of the used SiC MOSFETs

The total specific on-resistance $R_{DS(on),sp}$ consists of different layers of the device that the charge carriers pass through and can be expressed by the following equation:

$$R_{DS(on),sp} = R_{contact,sp} + R_{sub,sp} + R_{drift,sp} + R_{JFET,sp} + R_{ch,sp} + R_{n+,sp} \quad (2)$$

Here $R_{contact,sp}$ is the specific contact resistance, $R_{sub,sp}$ the specific substrate resistance, $R_{drift,sp}$ the specific drift resistance, $R_{drift,sp}$ the specific JFET resistance, $R_{ch,sp}$ the specific n-channel resistance, and $R_{drift,sp}$ the specific n^+-source resistance. This equation is valid during the surge current event in the 3rd quadrant of the SiC MOSFET during unipolar current conduction. Furthermore, in 3rd quadrant the impact of JFET resistance is not as significant as it is in 1st quadrant. The channel resistance is independent of the voltage class. However, its portion in the total resistance decreases with increasing voltage class. At 600 V and 1.2 kV, the proportion is approximately 66% and 48% respectively. Whereas, at 3.3 kV and 6.5 kV it decreases approximately to 13% and 3% respectively [4].

Measurement Results and Discussion

Influence of V_{GS} bias. Figure 2, shows a comparison between the critical current density $\hat{j}_{FSM}$ for channel-on and channel-off mode at $T_{initial}$ = 25°C for different voltage class devices.

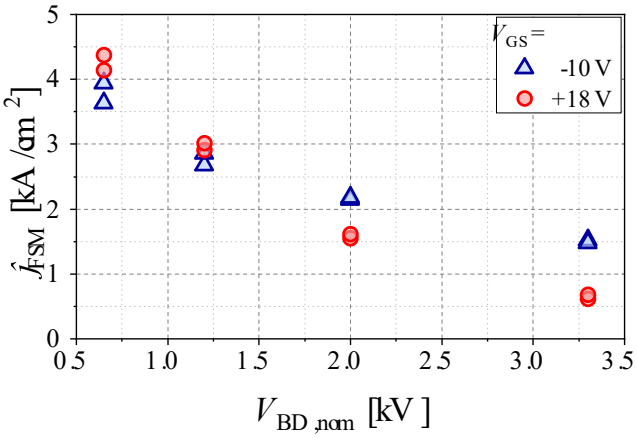

Fig. 2: Last-pass maximum surge current density of different voltage class SiC MOSFETs for different V_{GS} at t_{Surge} = 10 ms and $T_{initial}$ = 25°C.

The 650 V and 1.2 kV devices show a slightly higher surge current capability in terms of critical current density at V_{GS} = 18 V than at V_{GS} = -10 V. In contrast, for higher voltage class devices, i.e., 2 kV and 3.3 kV, the surge current capability is higher with V_{GS} = -10 V. For better analysis of this behavior,

the last non-destructive surge current pulse of the different voltage class devices in the I-V space for V_{GS} = -10 V and 18 V at $T_{initial}$ = 25°C are shown in Figure 3.

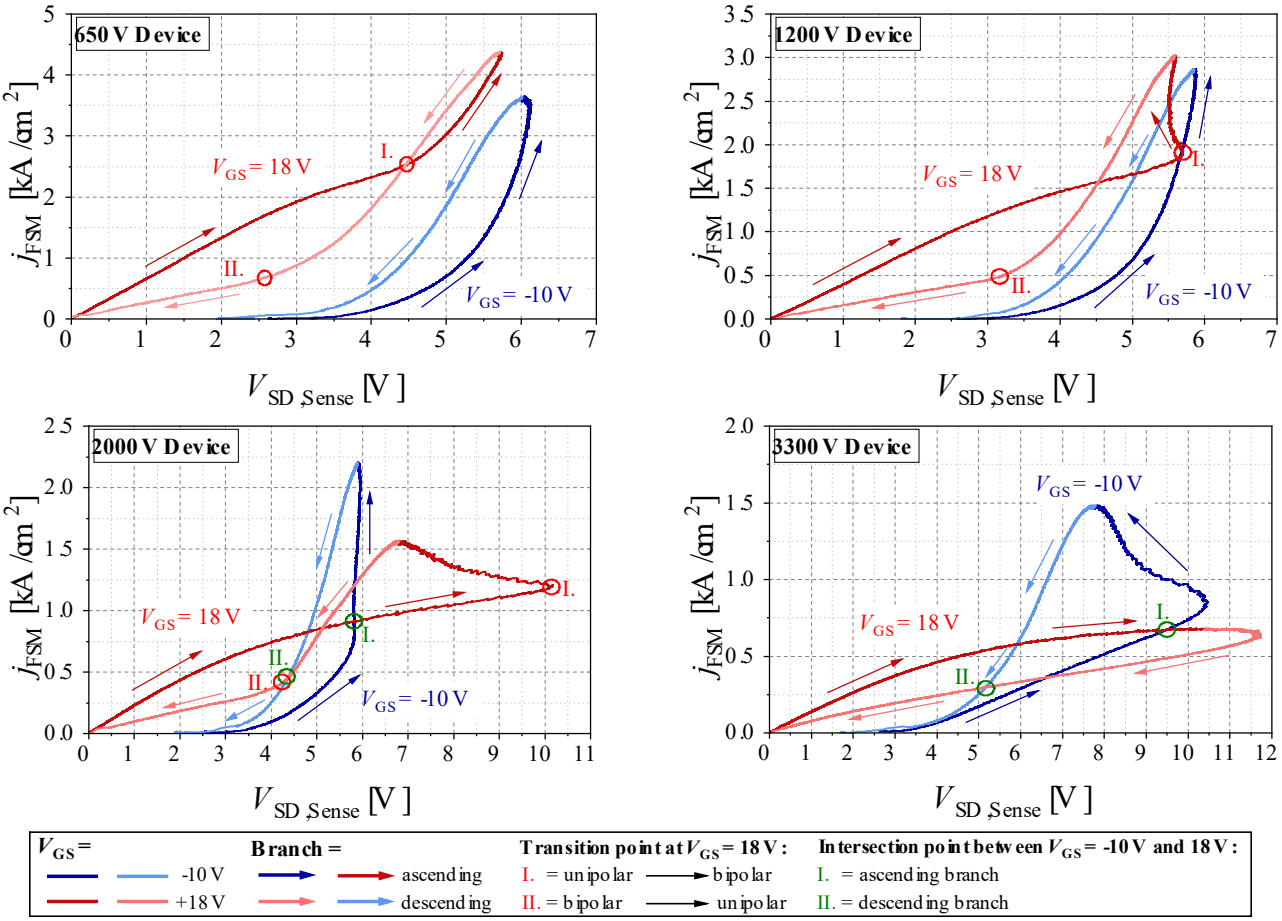

Fig. 3: Measured last non-destructive surge current pulse for different voltage class SiC MOSFET for different V_{GS} at t_{Surge} = 10 ms and $T_{initial}$ = 25°C

For all voltage classes measured it can be observed that for V_{GS} = 18 V, the surge current event starts directly at the coordinate origin, whereas for V_{GS} = -10 V the built-in voltage of the source side pn-junction has to be exceeded first. This is at approximately 2.7 V for SiC at T = 25°C. Consequently, there are lower losses at lower current densities when the channel is turned on. As the current density increases, the slope of the IV-curve decreases at V_{GS} = 18 V since the mobility of charge carriers in the channel as well as in the bulk decreases with elevated temperature. In the proximity of point I, marked in the graph, the triggering of the pn-junction occurs, and the p-regions consequently start to inject minority charge carriers. This happens, when the voltage drop caused by the electron current flow through the channel and in the vicinity of the p-region exceeds the built-in voltage of the pn-junction. At point I, the bipolar current exceeds the unipolar current in the device. The transition point I during the ascending branch for different voltage class devices is summarized in Table 1.

The transition from unipolar to bipolar current mode at V_{GS} = 18 V takes place at a higher V_{SD} with increased voltage class. As the proportion of the drift-resistance increases till it becomes the dominant resistance part in the total on-resistance, a higher proportion of the measured $V_{SD,Sense}$ drops across the drift-region. Therefore, as self-heating has to be considered, a higher $V_{SD,Sense}$ is necessary to reach the built-in voltage of the pn-junction at the given temperature. However, for the 3.3 kV device the pn-junction was not triggered up to the last-pass pulse.

A smooth transition from unipolar to bipolar current mode was observed for the 650 V device. For the 1.2 kV and 2 kV devices, a snapback phenomenon in the voltage was observed in the I-V curve during surge current. The snapback was more pronounced for the 2 kV device. In [5], the snapback

Table 1: Transition point from unipolar to bipolar current conduction during 10 ms surge current at V_{GS} = 18 V and $T_{initial}$ = 25°C (values extracted from Figure 3)

Voltage Class [V]	$V_{SD,Sense}$ [V]	j_{FSM} [kA/cm²]
650	4.5	2.6
1200	5.7	1.9
2000	10.1	1.2
3300	-	-

phenomenon and the triggering condition for the bipolar mode were intensively investigated for SiC MPS diodes. An important parameter is the ratio between the width of the p-layer and the thickness of the drift region. The snapback phenomenon decreases as this ratio increases. For devices with comparable cell technology, the thickness of the drift region increases. Therefore, devices with higher blocking voltage show a more pronounced snapback effect. However, for the 3.3 kV device, no snapback was visible as the bipolar mode was not triggered. After the snapback of the voltage, the curve continues with a negative differential resistance till the maximum is reached.

For the 650 V and 1.2 kV devices at V_{GS} = -10 V, the behavior of the ascending branch corresponds to a bipolar device with conductivity modulation. The descending branch is to the left of the ascending branch due to the negative temperature coefficient (NTC) behavior of the voltage. This is because the degree of ionization increases with elevated temperature and thus the injection efficiency of the p-emitter. Additionally, the lifetime of charge carriers increases with elevated temperature. However, for the 2 kV and 3.3 kV device, a sort of snapback in the voltage was seen for the ascending branch, which was more pronounced for the 3.3 kV device. This could be related to the fact, that the injection efficiency of the p-emitter is not strong enough to modulate the conductivity of the large drift region. This leads to a higher voltage drop and thus to a greater heating of the device. As the injection efficiency of the p-emitter increases with elevated temperature, the conductivity modulation gets enhanced and the voltage drop decreases strongly. As for the descending branch, an NTC behavior was observed. At V_{GS} = 18 V, the transition from bipolar to unipolar conduction mode in the descending branch, which is marked with II in Figure 3, took place at a much lower current density compared to the ascending branch as the temperature was much higher and the built-in voltage of the pn-junction decreases with elevated temperature. Simultaneously, the resistance in unipolar mode was at the descending branch higher due to the elevated temperature of the device.

In the first step, it can be concluded from the results, that the triggering of the pn-junction at high $V_{SD,Sense}$ as well as the snapback phenomenon leads to a reduced surge current capability at V_{GS} = 18 V than at -10 V for high voltage class devices. For the 3.3 kV device no triggering of the pn-junction was observed at all with opened channel. For the low voltage class device, the early activation of the bipolar mode, although the channel was open, helped to reduce the voltage drop. This means that at V_{GS} = 18 V a higher surge current capability can be reached in terms of current density for low voltage devices.

Influence of $T_{initial}$. The influence of $T_{initial}$ on the critical current density for different V_{GS} is shown in Figure 4. At V_{GS} = 18 V, the critical current density decreases with elevated $T_{initial}$ for 650 V and 1.2 kV. In contrast, for the 2 kV and 3.3 kV devices it stays nearly constant because the channel part of the total on-resistance is less dominating. Due to the decrease in carrier mobility in the n-channel and bulk during the unipolar current mode, V_{SD} increases with elevated $T_{initial}$ and shows a positive temperature coefficient (PTC). However, the triggering point of the bipolar current mode shifts to lower V_{SD} at elevated $T_{initial}$. Initially, the required built-in voltage for the pn-junction decreases and the voltage drop across the n-channel increases due to the reduced mobility. Thus, at increased $T_{initial}$, the bipolar current conduction is evoked quicker. However, this is not sufficient to greatly reduce the dissipated energy during surge current, because at lower current density the voltage drop increases due to unipolar conduction. Figure 5 shows this for the 1.2 kV device.

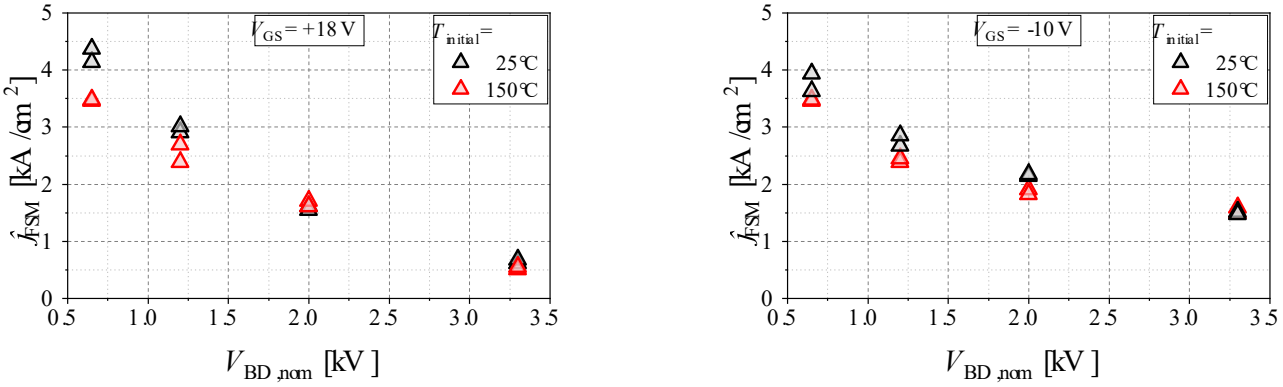

Fig. 4: Comparison between critical current density of different voltage class SiC MOSFETs for different V_{GS} and $T_{initial}$ at t_{Surge} = 10 ms.

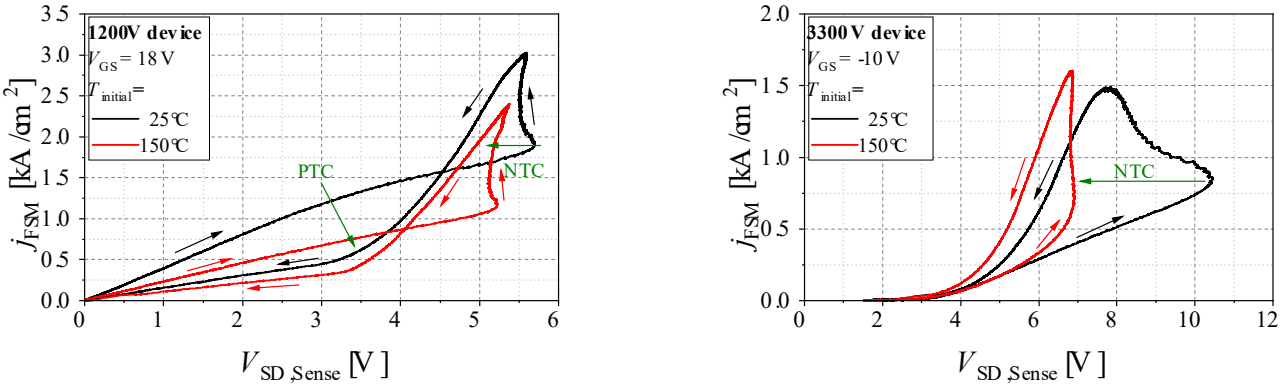

Fig. 5: Comparing the measured last non-destructive surge current pulse in the I-V space for different $T_{initial}$ at t_{Surge} = 10 ms.

At V_{GS} = -10 V, the critical current density decreases with elevated $T_{initial}$ for 650 V, 1.2 kV and 2 kV devices (see Figure 4). Despite lower power dissipation during the surge current pulse at increased $T_{initial}$ due to the NTC behavior of V_{SD}, the initial temperature is closer to the melting point of the metallization, which is a common failure mode during surge current [6]. However, for the 3.3 kV device the critical current density is nearly independent of $T_{initial}$. Due to an increasing ionization rate that leads to the increasing injection efficiency of the p-emitter, snapback of V_{SD} is significantly reduced at elevated $T_{initial}$. Thus the dissipated energy is strongly reduced and the melting point is attained at the same current density despite having a higher $T_{initial}$. This can be seen by comparing the last non-destructive surge current pulse for both $T_{initial}$ at V_{GS} = -10 V (see Figure 5) for the 3.3 kV device.

Optimizing the surge current behavior. The occurrence of two intersection points during the surge current pulse for high voltage class devices, i.e. 2 kV and 3.3 kV, can be seen in Figure 3 (marked in green circles). This was considered as an opportunity to switch V_{GS} during surge current and thus optimize voltage drop and losses, especially for the 3.3 kV device. Here, a big difference in the surge current capability was obtained by comparing the V_{GS} = 18 V and -10 V waveforms.

To investigate the influence of optimized V_{GS} switching during surge current event, two different approaches were selected. The gate-source voltage can be switched once at the first intersection point during the ascending branch in the surge current. Additionally, V_{GS} can be switched a second time during the descending branch when the second intersection point appears, which would be the optimum case with respect to minimal losses. In Figure 6, the influence of switching V_{GS} on the surge current event for the 3.3 kV device is shown for two different $T_{initial}$.

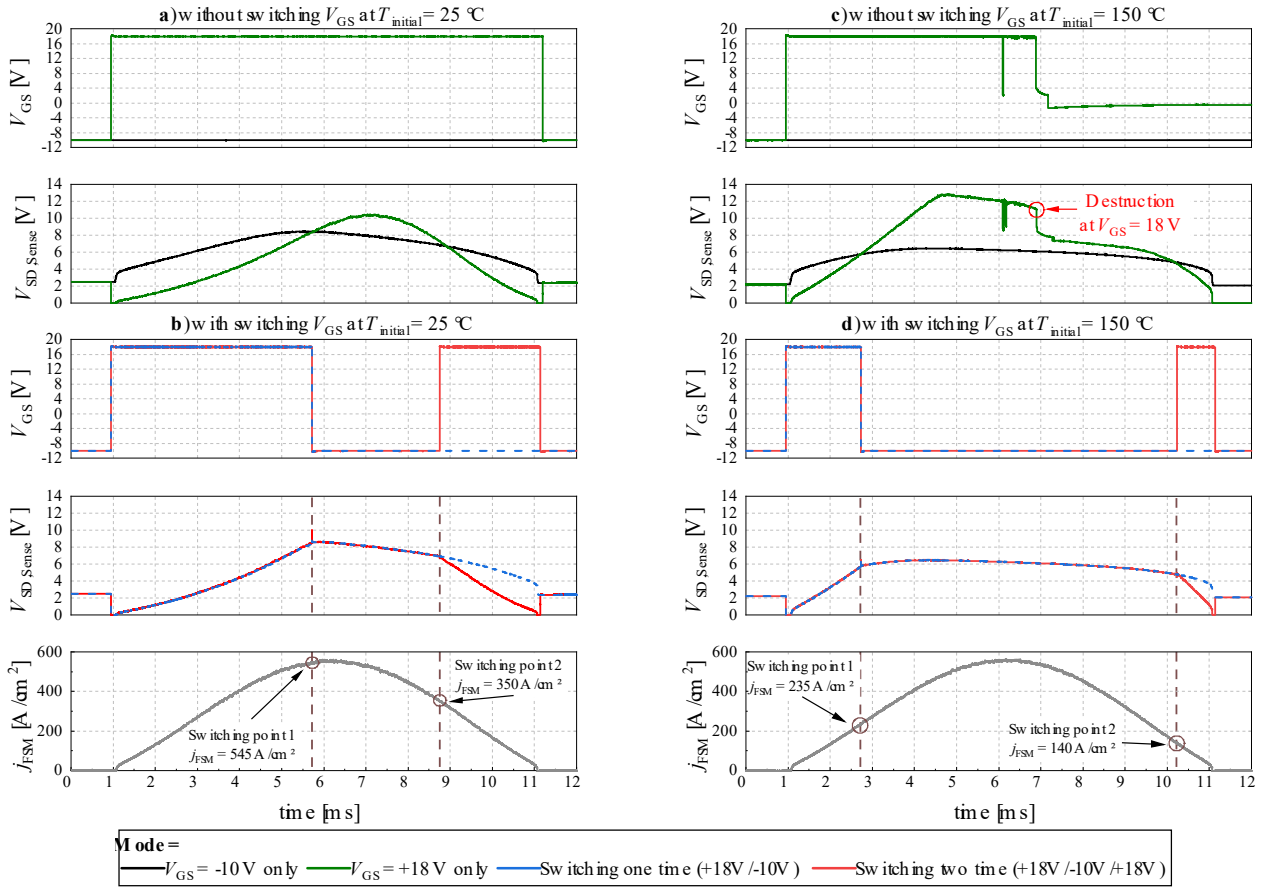

Fig. 6: Optimized switching of V_{GS} during 10 ms surge current event for the 3.3 kV device at $\hat{j}_{FSM}$ = 550 A/cm² for different $T_{initial}$

The voltage drop can be optimized, as shown in Figure 6, depending on which channel mode provides a lower source drain voltage drop at the respective current density. This allows the external definition of whether a unipolar or bipolar current flow is advantageous depending on the current density. Thus, the excessively high voltages required to achieve the built-in voltage of the pn-junction or pronounced snapback phenomena for high voltage devices can be avoided. The destruction of the device at V_{GS} = 18 V and $T_{initial}$ = 150°C can be seen in Figure 6c. However, this can be prevented by switching V_{GS} at the intersection point with V_{GS} = -10 V.

Table 2: Energy dissipation during a 10 ms surge current pulse at $\hat{j}_{FSM}$ = 550 A/cm² with different V_{GS} modes and $T_{initial}$ (Note: Energy reduction in brackets compared to V_{GS} = -10 V only)

Mode	$T_{initial}$ = 25°C	$T_{initial}$ = 150°C
V_{GS} = -10 V only	26.3 J/cm²	20.1 J/cm²
V_{GS} = 18 V only	24.7 J/cm² (6.1%)	- - J/cm²
Switching one time	23.3 J/cm² (11.4%)	19.9 J/cm² (1%)
Switching two time	22.7 J/cm² (13.7%)	19.8 J/cm² (1.5%)

The energy dissipated during a surge current pulse can be reduced by optimizing V_{SD} by switching V_{GS} (see Table 2), especially at $T_{initial}$ = 25°C. However, it does not differ significantly if V_{GS} is switched once or twice during the surge current event in terms of energy reduction. One reason for this is that the second switching during the descending branch occurs at a lower current density and therefore its contribution to the total loss is minor. Furthermore, at elevated $T_{initial}$ the energy saving is negligible. This can be attributed to the contrary temperature coefficient of the unipolar and bipolar current mode.

Both branches converge quickly and thus the difference in V_{SD} is minor (see Figure 6c). A further critical aspect at elevated $T_{initial}$ is the current density at which V_{GS} is switched during surge current. This current density is comparatively low and close to the application near current density value. If this approach is implemented in an application, this can lead to a false detection of a surge current and thus to an unintended switching of V_{GS}. Therefore, a third approach was implemented, where V_{GS} was switched at a defined current density. For the 3.3 kV device this was specified at the critical current density at V_{GS} = 18 V and $T_{initial}$ = 150°C, as the lowest surge current capability was achieved here.

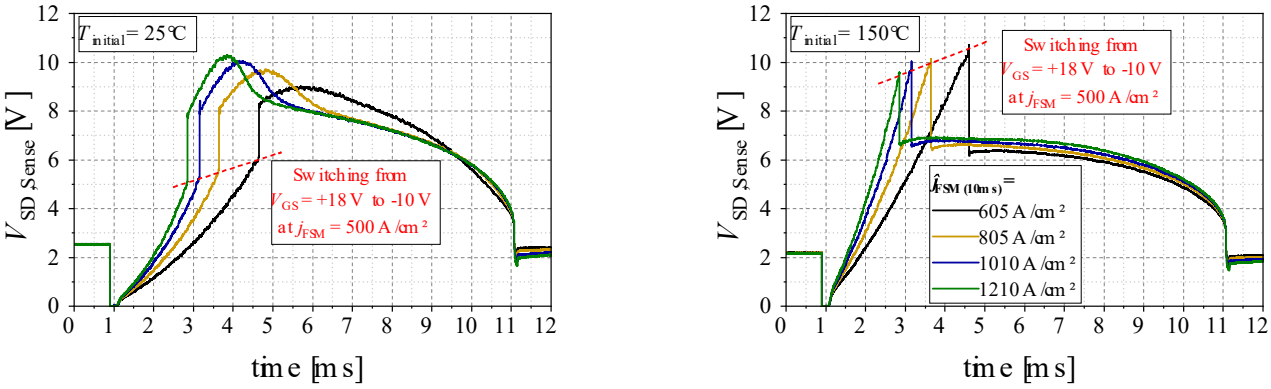

Fig. 7: Switching of V_{GS} at j_{FSM} = 500 A/cm² during a 10 ms surge current event for the 3.3 kV device for different $\hat{j}_{FSM}$ and $T_{initial}$.

Figure 7 shows a surge current pulse for different $\hat{j}_{FSM}$ while switching V_{GS} from 18 V to -10 V after j_{FSM} = 500 A/cm² is reached for the 3.3 kV device. For both $T_{initial}$, it can be seen in the V_{SD} curve that the switching point is not optimized. For $T_{initial}$ = 25°C the switching procedure occurs too early. On the other hand, it occurs too late at $T_{initial}$ = 150°C. This can be seen from the steep rise/fall of V_{SD} during the switching. Nonetheless, in this case also the surge current capability for V_{GS} = 18 V could be increased by switching V_{GS} to -10 V during the surge current event.

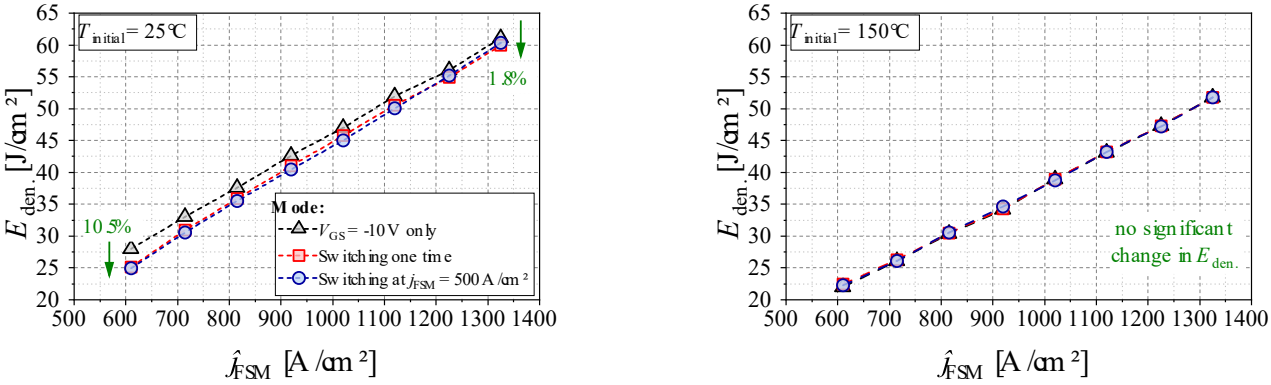

Fig. 8: Surge current energy densities for 3.3 kV device with different switching approaches during a 10 ms surge current event at different $\hat{j}_{FSM}$ and $T_{initial}$.

An overview of the surge current energy density for different switching approaches compared to the channel-off mode is shown in Figure 8 for both $T_{initial}$. A lower energy density can be reached by switching V_{GS} during surge current at lower current density for $T_{initial}$ = 25°C. As $\hat{j}_{FSM}$ increases, the curves for the different modes converge. The difference, therefore, becomes progressively lower. In addition, there is no significant difference in terms of energy density between switching once at the intersection point of the V_{GS} = -10 V and 18 V branch and switching V_{GS} when a defined current density is reached. At higher $T_{initial}$ no significant change in the energy for different modes was observed.

Summary

In this paper, the single-pulse surge current SOA for devices of different voltage classes, depending on V_{GS}, was investigated. Devices of voltage class 650 V and 1.2 kV achieve higher surge current capability if the n-channel is permanently turned on with V_{GS} = 18 V during the entire event. On the other hand, devices of voltage class 2 kV and above achieve higher surge current capability if the n-channel is permanently switched off with V_{GS} = -10 V. The triggering of the pn-junction at high V_{SD} as well as the snapback phenomenon lead to a reduced surge current capability at V_{GS} = 18 V.

A new method of switching V_{GS} during surge current and thus optimizing V_{DS} was introduced in this paper using 3.3 kV devices as an example. Three different approaches were chosen. In the first approach, V_{GS} was switched only once during the surge current. In the second approach, a second switching of V_{GS} was performed during the descending branch. It was found that early destruction of the device at V_{GS} = 18 V can be avoided by switching V_{GS} to -10 V and, thus, the SOA can be increased. As for the energy dissipated, a reduction could be achieved by switching V_{GS}. However, as the current density amplitude increases, the reduction potential decreases because the channel worsens. There was also no significant difference between switching V_{GS} once or twice during the surge current. The problem that emerged for both approaches at elevated temperatures was the current density value at which the switching occurs. The value is close to the application-compliant current density value and therefore could lead to an undesired switching of V_{GS}. Therefore, a third approach was chosen where the switching operation was performed at a defined current density value far above the application value. Again, the SOA for V_{GS} = 18 V could be increased by switching V_{GS}. In this approach, an energy reduction comparable to the first and second approaches was achieved.

For an application, switching V_{GS} during a surge current when the defined current density is reached is recommended. This can be implemented at the gate-driver and control level and combined with dedicated surge current detection by monitoring the current gradient.

References

[1] T. Basler, D. Heer, D. Peters, T. Aichinger and R. Schoerner, ”Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET,” in *Proc. PCIM Europe*, 2018, pp. 1-7.

[2] A. Mihaila et al., ”Surge current capability of 6.5kV-rated SiC MOSFETs,” in *Proc. 32nd ISPSD*, 2020, pp. 222-225, doi: 10.1109/ISPSD46842.2020.9170186.

[3] S. Palanisamy J. Kowalsky, J. Lutz, T. Basler, R. Rupp and J. Moazzami-Fallah, ”Repetitive surge current test of SiC MPS diode with load in bipolar regime,” in *Proc. 30th ISPSD*, 2018, pp. 367-370, doi: 10.1109/ISPSD.2018.8393679.

[4] T. Kimoto, H. Watanabe, ”Defect engineering in SiC technology for high-voltage power devices”, in *Appl. Phys. Express 13 (2020)*, doi: 10.35848/1882-0786/abc787.

[5] H. Niwa, J. Suda and T. Kimoto, ”Ultrahigh-Voltage SiC MPS Diodes With Hybrid Unipolar/Bipolar Operation,” in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 874-881, March 2017, doi: 10.1109/TED.2016.2636573.

[6] P. Hofstetter and M. -M. Bakran, ”Predicting Failure of SiC MOSFETs under Short Circuit and Surge Current Conditions with a Single Thermal Model,” in *Proc. 20th EPE’18 ECCE Europe*, 2018, pp. P.1-P.9.