Solid State Phenomena
ISSN: 1662-9779, Vol. 360, pp 111-118
doi:10.4028/p-EkvC4B

Submitted: 2023-09-13
Accepted: 2024-04-08
Online: 2024-08-23

Analytical Modelling of the Quasi-Static Operation of a Monolithically Integrated 4H-SiC Circuit Breaker Device

Norman Boettcher[1,a*], Mathias Rommel[1,b], and Tobias Erlbacher[2,c]

[1]Fraunhofer IISB, Schottkystrasse 10, 91058, Erlangen, Germany

[2]Friedrich-Alexander University, Cauerstrasse 6, 91058, Erlangen, Germany

[a]norman.boettcher@iisb.fraunhofer.de, [b]mathias.rommel@iisb.fraunhofer.de, [c]tobias.erlbacher@nexperia.com

Keywords: 4H-SiC, self-sensed, circuit breaker, SSCB, JFET, gate breakdown, analytical model.

Abstract. In this work, an analytical model describing the quasi-static operation of a monolithically integrated SiC solid-state circuit breaker (SSCB) device is rederived and refined. This SSCB is based on a 4H-SiC JFET technology offering a self-sensed blocking mechanism. The proposed model is solely based on physical parameters including the SSCB design parameters. With respect to the refinement, the proposed model is not limited to one-sided pn-junctions, considers incomplete ionization of dopants, and is able to represent breakdown characteristics. In this regard, the JFET gate breakdown characteristics are derived taking thermionic emission, space-charge-limited current and impact ionization into account. To calculate the SSCB output characteristics, a bisection-based optimization algorithm is applied carefully considering individual JFET operating states.

Introduction

In power electronic DC applications (e.g. 600 V to 900 V automotive and industrial applications), interrupting current flow in case of failure poses significant challenges in terms of reaction time, switching speed and energy conversion capacity. Recent studies concluded that solid-state circuit breakers (SSCB) represent the most potent solution to overcome these challenges due to their outstanding integration capability and the natural absence of arcing issues [1]. It is worth noticing, that most state-of-the-art SSCBs rely on an electronic auxiliary circuit consisting of at least a current sensor, a micro controller, and a gate driver to detect the fault state and, subsequently, stop the fault current by turning off the conducting semiconductor power switch. Moreover, these components must be supplied by additional isolated DC/DC converters. As a result, the design of conventional SSCB solutions require efforts of a rather high complexity on system level [2].

Recently, a self-sensed and self-supplied two-pole SSCB device technology has been presented and promising switching performance at up to 800 V has been demonstrated based on prototype devices [3-5]. Moreover, a first analytical modelling approach to the intrinsic blocking mechanism of these novel SSCB devices solely based on physical parameters has been proposed [6]. In this work, a refined modelling approach is presented allowing for the determination of the full range quasi-static SSCB operation including conduction, saturation, blocking and breakdown states.

Analytical Derivation of the Basic Operation

The novel SSCB device employs monolithic integration of two complementary normally-on JFETs. A schematic equivalent circuit diagram is shown in Fig. 1. In principle, both JFETs are arranged in anti-series configuration, with the source terminals (denoted with S) facing each other. In conduction state, the entire anode current (I_A) is assumed to flow from anode (A) to cathode (K) through the JFET channels as indicated by the red line. A key feature of this SSCB manifests in the gate (G) of the n-channel JFET (nJFET) being interconnected to drain (D) of the p-channel JFET (pJFET) and reversed. As a result, the drain-source voltage ($V_{\mathrm{DS,n/p}}$) of one JFET is equal to the gate-source voltage ($V_{\mathrm{GS,n/p}}$) of the other JFET. In this configuration, self-induced transition from conduction to blocking state is achieved as soon as I_A reaches a certain trigger current level [3-6].

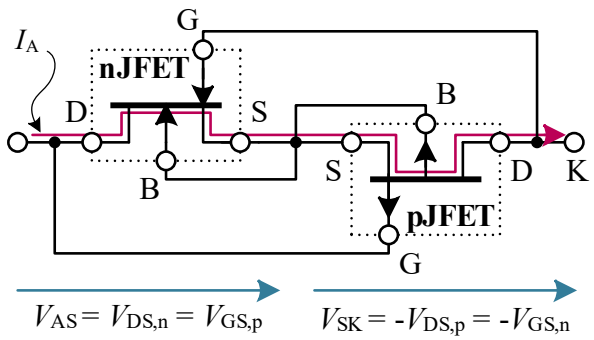

Fig. 1. Equivalent circuit diagram of the investigated SSCB. The JFETs are arranged in anti-series configuration with the source and back-gate terminals (S and B) being shorted. Additionally, each gate (G) is interconnected to the opposing drain (D). In conduction state, the anode current (I_A) is assumed to entirely flow through both JFET channels as indicated by the red line.

For the proposed modelling approach, well-known equations derived for the nJFET are adapted for the pJFET and, ultimately, applied to the circuit configuration shown in Fig. 1 [7]. Please note, that the following system of equations refers only to the pJFET. The characteristics of the nJFET are analogously derived considering adequate parameters as given in the literature [7].

pJFET Conduction Operation. In a first step, a pJFET in conduction state is considered according to the schematic cross section shown in Fig. 2 (a). The essential JFET characteristics can be understood by modelling only the channel region ranging from $x = 0$ to $x = l_{Ch}$ and assuming ideal drain (D) and source (S) contact regions. In the following, the source and backgate potentials are considered grounded ($V_S = V_B = 0$). As a result, a current flow from source to drain ($-I_D$) is established by applying a negative bias to drain ($V_D < 0$). Applying a positive bias to gate ($V_G > 0$) causes the depletion region at the gate-channel pn-junction to expand into the channel narrowing the effective channel and, eventually, causing complete channel pinch-off ($V_G \geq V_{th}$). This allows for a modulation of I_D at a given value of V_D with the aid of V_G. Any current between electrodes other than source and drain is neglected during the investigation of the conduction operation.

Assuming uniform current distribution in the channel, an expression for I_D only depending on V_D and V_G, and relevant design and material parameters (see Fig. 2) can be obtained as given in Eq. (1).

$$I_D = \sigma \cdot d_{Ch} \cdot \frac{W_z}{l_{Ch}} \cdot V_D \left\{ 1 + \frac{2}{3 d_{Ch} \cdot V_D} \left[\begin{array}{l} \sqrt{\frac{2\epsilon_{SiC}}{e \cdot N_B^*}} \left(\left(\Psi_{bi,B} - V_D\right)^{\frac{3}{2}} - \Psi_{bi,B}^{\frac{3}{2}} \right) + \\ \sqrt{\frac{2\epsilon_{SiC}}{e \cdot N_G^*}} \left(\Psi_{bi,G} - V_D + V_G\right)^{\frac{3}{2}} - \left(\Psi_{bi,G} + V_G\right)^{\frac{3}{2}} \end{array} \right] \right\} \quad (1)$$

Here, ϵ_{SiC} represents the dielectric constant of 4H-SiC and l_{Ch}, d_{Ch} and W_z are the channel length, channel depth and cell extent in the x-, y- and z-direction, respectively. The acceptor concentration in the channel ($N_{A,Ch}$) as major design parameter is accounted for by the terms $N_{B/G}^*$ according to

$$N_{B/G}^* \equiv \frac{N_{A,Ch}\left(N_{A,Ch} + N_{D,B/G}\right)}{N_{D,B/G}}, \quad (2)$$

where $N_{D,B/G}$ are the donor concentrations in the backgate and gate regions, respectively. Compared to previous modelling approaches known from literature, the terms $N_{B/G}^*$ allow for a wider range of doping levels (e.g. $N_{D,G} \leq N_{A,Ch}$) [6, 7]. The doping level of $N_{A,Ch}$ significantly affects the electrical conductivity in the channel region, which in Eq. (1) is accounted for by the parameter σ and is calculated by the elementary charge (q), mobility of holes (μ) and the ionized doping fraction of acceptors in the channel region ($N_{A,Ch}^-$) according to $\sigma = q \cdot \mu \cdot N_{A,Ch}^-$. Due to a higher probability of

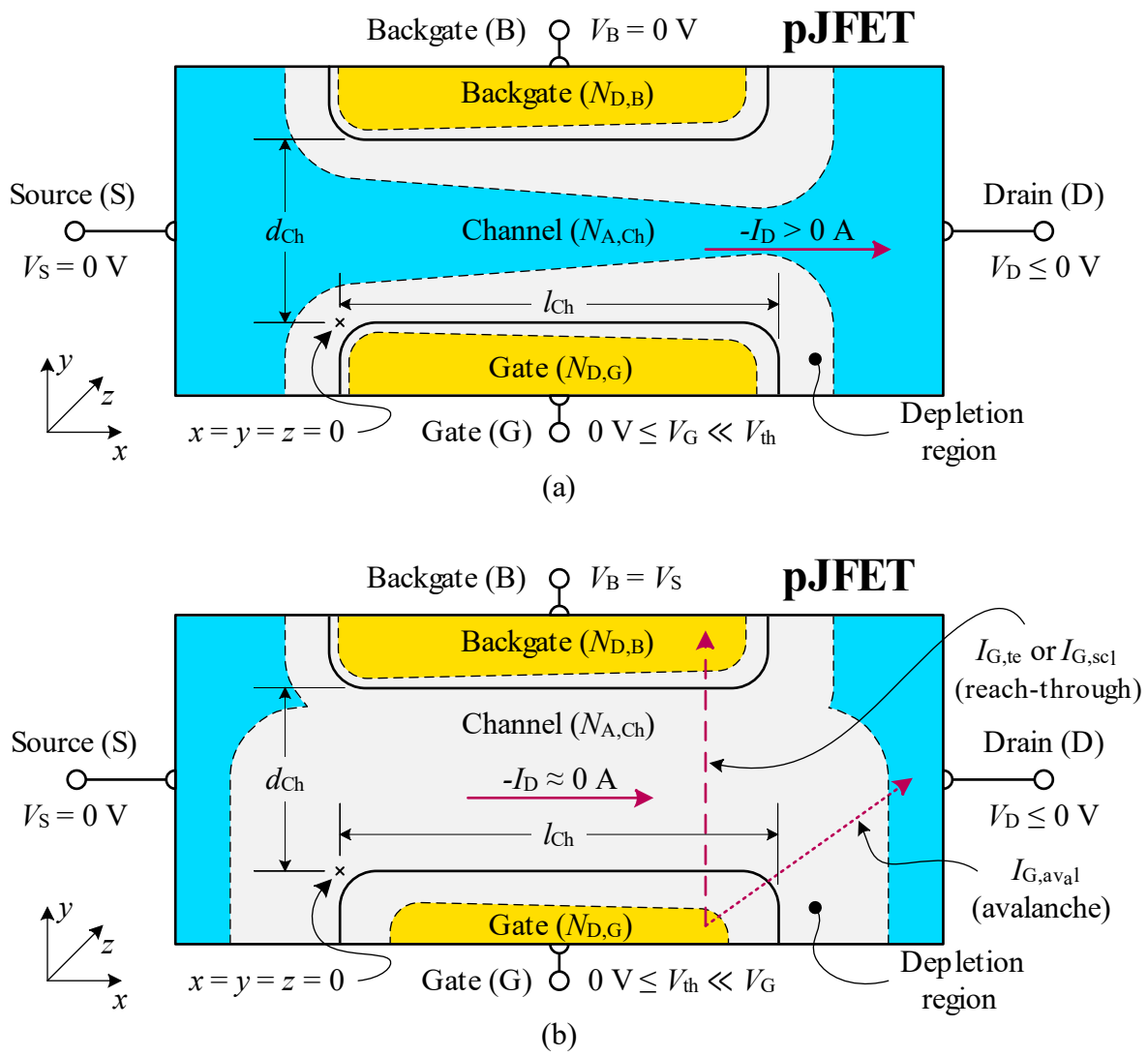

Fig. 2. Schematic cross-section of a pJFET in conduction (a) and blocking state (b) introducing all relevant design parameters used in the equations. In (b) the gate-breakdown mechanisms reach-through and avalanche are emphasized by the red dashed and dotted lines, respectively.

lattice scattering, μ decreases with increasing channel doping. This effect is considered in the model with the aid of empirical equations obtained from the literature [7].

The fraction of ionized acceptors strongly depends on the lattice temperature (T) according to the Fermi-Dirac distribution:

$$\frac{N_{A,Ch}^{-}}{N_{A,Ch}} = \left[1 + g_A \cdot \exp\left(-\frac{E_A - E_F}{k \cdot T}\right)\right]^{-1} \tag{3}$$

Here, $g_A = 4$ is the degeneration factor of acceptors, k is the Boltzmann constant, and E_F is the Fermi energy. Due to their relative high ionization energy (E_A) of approx. 200 meV, aluminum acceptors particularly suffer from incomplete ionization. At room temperature, in a reasonable range of doping concentration (e.g. 10^{16} cm^{-3} to 10^{19} cm^{-3}), only 5% to 30% of the successfully substituted aluminum atoms can be considered ionized in neutral regions, that is, outside of the depletion regions. In the proposed model, the neutrality equation is used to find a solution for E_F and, ultimately, determine the number of ionized dopants [7].

In thermal equilibrium of drift and diffusion currents, a built-in potential across the pn-junctions determined by the ionized donors and acceptors in the respective depletion regions ($N_{D,B/G}^{+}$ and $N_{A,Ch}^{-}$)

exist. In Eq. (1), the built-in potentials of the backgate, gate and channel regions are represented by the parameters $\Psi_{\mathrm{bi,B/G}}$. Knowing the intrinsic carrier density (n_i), $\Psi_{\mathrm{bi,B/G}}$ can be approximated to

$$\Psi_{\mathrm{bi,B/G}} \approx \frac{k \cdot T}{q} \cdot \ln\left(\frac{N^{+}_{\mathrm{D,B/G}} \cdot N^{-}_{\mathrm{A,Ch}}}{{n_\mathrm{i}}^2}\right). \tag{4}$$

The terms inside the curly brackets of Eq. (1) represent the expansion of the depletion region into the channel. Increasing $-V_\mathrm{D}$ and considering $V_\mathrm{G} \ll V_\mathrm{th}$, an asymmetric widening of the depletion region is observed, eventually, leading to pinch-off in a single point at the drain end of the channel as soon as the saturation voltage (V_sat) is reached. Assuming $N_\mathrm{D,B} = N_\mathrm{D,G}$ leads to $N^* \equiv N^*_\mathrm{B} = N^*_\mathrm{G}$ and $\Psi_\mathrm{bi} \equiv \Psi_\mathrm{bi,B} = \Psi_\mathrm{bi,G}$, and allows to estimate V_sat to:

$$V_\mathrm{sat} = -\frac{{V_\mathrm{G}}^2}{{d_\mathrm{Ch}}^2} \cdot \frac{\varepsilon_\mathrm{SiC}}{2q \cdot N^*} + \frac{V_\mathrm{G}}{2} - {d_\mathrm{Ch}}^2 \left(\frac{8\varepsilon_\mathrm{SiC}}{q \cdot N^*}\right)^{-1} + \Psi_\mathrm{bi} \tag{5}$$

Increasing V_D beyond V_sat has no effect on I_D. In the model, this is accounted for by substituting V_sat in Eq. (1) for V_D if the saturation condition is met.

pJFET Breakdown Operation. We now wish to derive the breakdown mechanisms limiting the blocking voltage capability of the investigated SSCB configuration shown in Fig. 1. Considering the shared source node of both JFETs (S) to be floating between the potentials of anode and cathode (V_A and V_K), careful observation reveals, that V_G of either JFET might reach values as high as the anode-cathode voltage (V_AK). With respect to the scope of high voltage DC applications, at least 900 V must be considered for V_AK. Hence, to derive the breakdown behavior of the SSCB, the voltage blocking limitations of the JFET gate structures must be understood.

The gate breakdown mechanisms of a JFET can be derived with the aid of the schematic cross-section of the pJFET in blocking state depicted in Fig. 2 (b). As soon as V_G exceeds V_th, the channel region is entirely pinched off preventing current flow between source and drain. Following the approaches known from literature, $V_\mathrm{G} = V_\mathrm{th}$ marks the point where pinch-off occurs at $x = 0$, which leads to the following expression:

$$\boldsymbol{V_\mathrm{th} = \left(\frac{\varepsilon_{SiC}}{q \cdot N^*_\mathrm{G}}\right)^{-1} \left\{\frac{{d_\mathrm{Ch}}^2}{2} - d_\mathrm{Ch}\sqrt{\frac{2\varepsilon_\mathrm{SiC}}{q \cdot N^*_\mathrm{B}} \cdot \Psi_\mathrm{bi,B}} + \frac{\varepsilon_\mathrm{SiC}}{q}\left(\frac{\Psi_\mathrm{bi,B}}{N^*_\mathrm{B}} - \frac{\Psi_\mathrm{bi,G}}{N^*_\mathrm{G}}\right)\right\}} \tag{6}$$

With the pinch-off, the electric field in y-direction originating from the gate-channel pn-junction reaches through the channel and, subsequently, biases the backgate-channel pn-junction in forward direction. Consequently, electrons from the backgate are injected into the channel through thermionic emission leading to an exponentially increasing gate current ($I_\mathrm{G,te}$, see Fig. 2 (b)) given by the Richardson equation [8]:

$$\boldsymbol{I_\mathrm{G,te} = W_z \cdot l_\mathrm{Ch} \cdot A^*_\mathrm{e} \cdot T^2 \cdot \exp\left(-\frac{q(V_\mathrm{fb} - V_\mathrm{G})^2}{4k \cdot T \cdot V_\mathrm{fb}}\right)} \tag{7}$$

Here, A^*_e is the effective Richardson constant [8]. For $V_\mathrm{G} \approx V_\mathrm{th}$, $I_\mathrm{G,te}$ is negligibly small but it becomes significantly large as soon as V_G approaches the flat-band voltage (V_fb) given by [7, 8]:

$$V_\mathrm{fb} = \frac{q \cdot N^*_\mathrm{G} \cdot d^2_\mathrm{Ch}}{2\epsilon_\mathrm{SiC}} - \Psi_\mathrm{bi,G} \tag{8}$$

Eventually, the injected electrons exceed $N_{\mathrm{A,Ch}}^{-}$ and, in turn, affect the electric field in the channel. As $I_{\mathrm{G,te}}$ is a drift current, the feedback of electric field and injected carriers is giving rise to the effect of space-charge-limited current ($I_{\mathrm{G,scl}}$), which increases linearly with V_{G} according to Eq. (9) [8].

$$I_{\mathrm{G,scl}} = W_{\mathrm{z}} \cdot l_{\mathrm{Ch}} \cdot q \cdot v_{\mathrm{sat}} \cdot N_{\mathrm{A,Ch}} \cdot \frac{V_{\mathrm{G}}}{V_{\mathrm{fb}}} \tag{9}$$

Here, v_{sat} represents the saturation velocity of electrons in 4H-SiC. Depending on the design of the device, $I_{\mathrm{G,scl}}$ is determining the value of I_{G} over a wide range of V_{G}. Nevertheless, by increasing V_{G} beyond the avalanche voltage (V_{aval}), the critical electric field of 4H-SiC (E_{crit}) is reached resulting in avalanche breakdown due to impact ionization. Typically, avalanche during gate breakdown occurs between gate and drain as is illustrated in Fig. 2 (b). Assuming E_{crit} is reached under non-punch-through conditions and considering Eq. (2), V_{aval} can be estimated to:

$$V_{\mathrm{aval}} = \frac{{E_{\mathrm{crit}}}^2 \cdot \varepsilon_{\mathrm{SiC}}}{2q} \left(\frac{1}{N_{\mathrm{D,G}}} + \frac{1}{N_{\mathrm{A,Ch}}} \right) \tag{10}$$

Calculation of the Quasi-Static Operation

Utilizing the introduced set of equations, the quasi-static characteristics of both JFETs and, ultimately, of the investigated SSCB circuit configuration can be calculated.

pJFET Quasi-Static Operation. The transfer and gate breakdown characteristics ($I_{\mathrm{D}}(V_{\mathrm{G}})$ and $I_{\mathrm{G}}(V_{\mathrm{G}})$) of the pJFET at room temperature are shown in Fig. 3. Here, the design parameters $N_{\mathrm{A,Ch}} = N_{\mathrm{D,B}} = 10^{17}$ cm^{-3}, $d_{\mathrm{Ch}} = 0.5$ µm and $l_{\mathrm{Ch}} = 1.5$ µm are used. The families of curves represent a variation of $N_{\mathrm{D,G}}$ in a range from 1.5×10^{16} cm^{-3} to 2×10^{17} cm^{-3}, emphasizing that V_{th} as well as the gate-breakdown voltage are strongly affected by the effect of non-one-sided pn-junctions accounted for by Eq. (2). This trend is observed, because for lower doping levels of $N_{\mathrm{D,G}}$, the depletion region extends rather into the gate region than the channel region. Consequently, both V_{th} and the onset of reach-through in the form of $I_{\mathrm{G,te}}$ occur at higher values of V_{G}. Typically, the desired V_{th} of a power transistor lies in the range of 5 V to 20 V. Hence, rather high doping concentration is employed in the gate region. However, as the JFET gate breakdown represents the

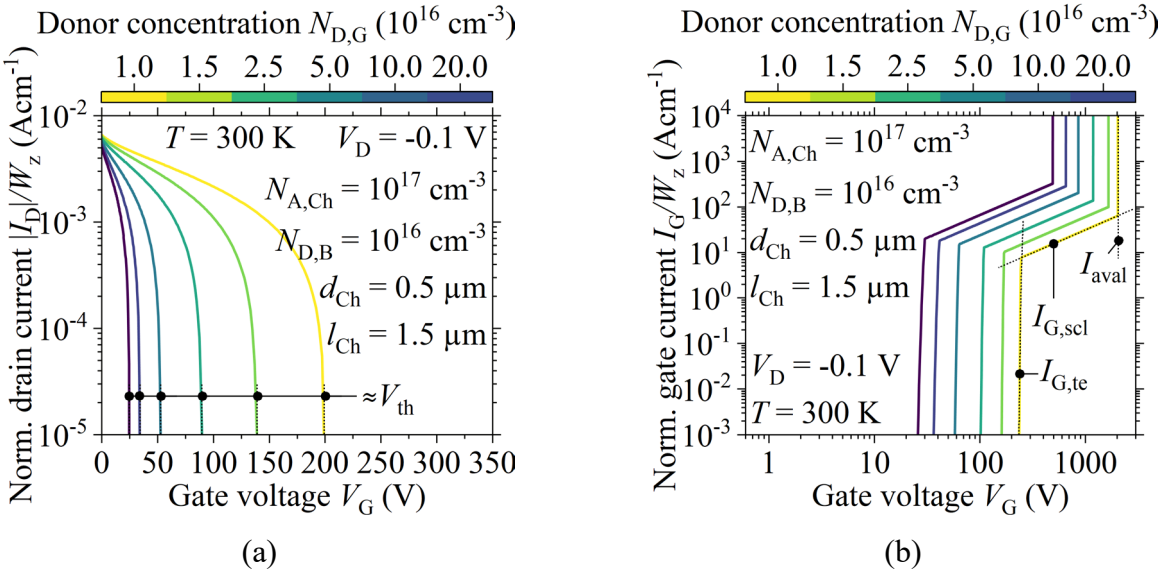

Fig. 3. Analytical calculation results of the pJFET transfer (a) and gate-breakdown characteristics (b). In (b), thermionic emission, space-charge-limited current and impact ionization are indicated by $I_{\mathrm{G,te}}$, $I_{\mathrm{G,scl}}$ and I_{aval}, respectively.

main breakdown mechanism of the investigate SSCB, low doping concentration in the gate regions poses a key design measure for achieving high anode-cathode voltage (V_{AK}) blocking capabilities up to several hundred volts.

Whether reach-through or avalanche is the limiting breakdown mechanism, is determined by the design parameters. Stating $V_{fb} < V_{aval}$ using Eq. (8) and Eq. (10), the boundary condition for reach-through to occur before avalanche can be estimated to:

$$d_{Ch} \cdot N_{A,K} < \frac{\varepsilon_{SiC} \cdot E_{crit}}{q} \tag{11}$$

Notably, Eq. (11) is independent of $N_{D,G}$, which agrees with the observed trend in Fig. 3 (b). Moreover, as Eq. (8) marks the maximum of the parabolic course of $I_{G,te}$ instead of a specific value representing a relevant reach-through current, Eq. (11) has limited validity for $V_{fb} \approx V_{aval}$.

SSCB Quasi-Static Operation. For better understanding, the visualization of the equivalent circuit diagram shown in Fig. 1 is exchanged for the one depicted in Fig. 4. Here, relevant design parameters as well as current paths during conduction and breakdown operation are emphasized. Please note, the indices "n" and "p" denote for the nJFET and pJFET, respectively. It should also be noted that only the channel, gate and backgate regions are considered in model. Metal-semiconductor junctions as well as interconnections are assumed ideal and parasitic components are entirely neglected.

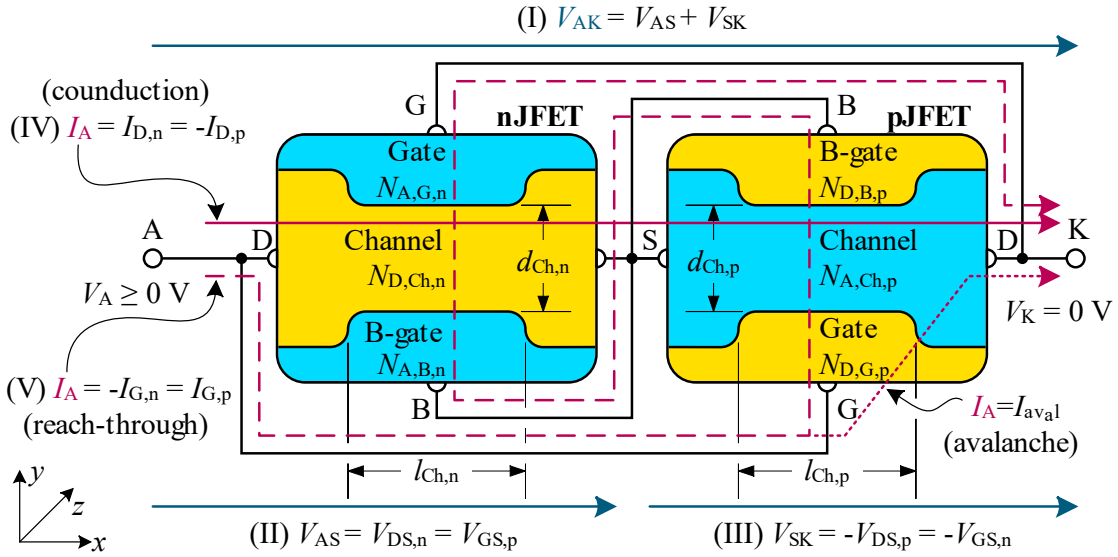

Fig. 4. Schematic equivalent circuit diagram of the proposed SSCB emphasizing design parameters and current paths during conduction and breakdown operation.

The basic operation of the investigated SSCB is based on positive feedback of V_{DS} and V_{GS} between both JFETs. This feedback loop makes a numerical calculation approach necessary to determine the quasi-static characteristics. In a first step, the JFET operating states are determined for each SSCB operating point according to Eq. (5), Eq. (6) and three basic assumptions: (I) $V_{AK} = V_{AS} + V_{SK}$, (II) $V_{AS} = V_{DS,n} = V_{GS,p}$ and (III) $V_{SK} = -V_{DS,p} = -V_{GS,n}$ (see Fig. 4). The results are illustrated in Fig. 5 (a). Here, the linear (denoted with 1), saturation (2) and blocking (3) operating states are illustrated for all combinations of V_{AS} and V_{SK} for $V_{AK} = \{0\text{ V}..250\text{ V}\}$. These solutions are obtained for the set of design parameters given in Fig. 6 and an acceptor concentration in the p-channel ($N_{A,Ch,p}$) of 10^{17} cm^{-3}. The pronounced asymmetry despite similar JFET design parameters

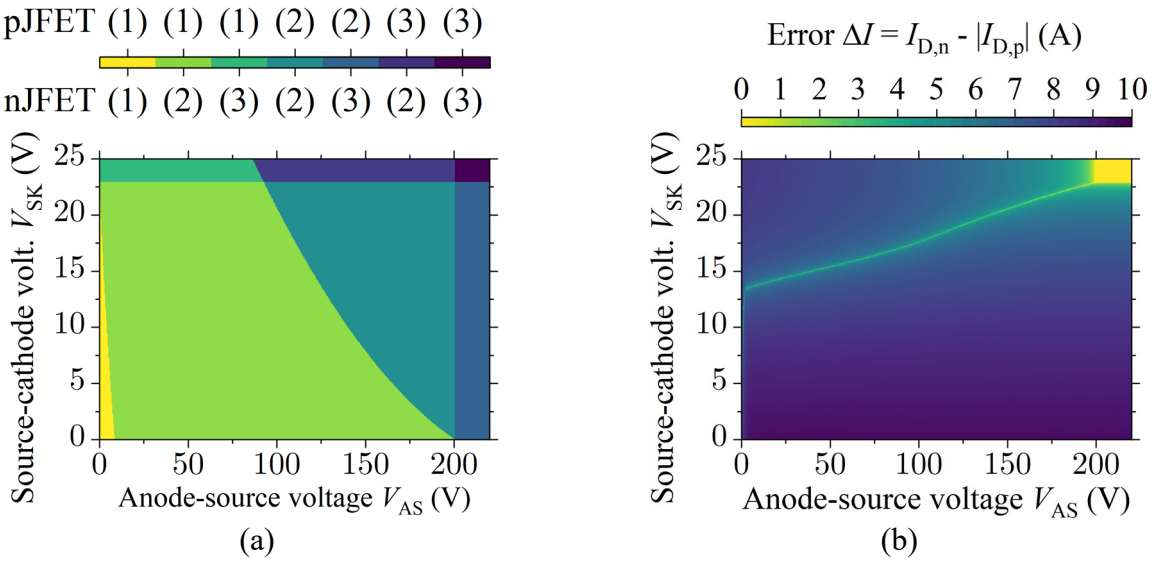

Fig. 5. JFET operating states (a) and optimization error (b) for SSCB operating points ranging from conduction to blocking state. In (a), the JFET linear (1), saturation (2) and blocking (3) operating states are illustrated.

exclusively originates from the lower doping level in the pJFET gate and backgate regions ($N_{\mathrm{D,G,p}}$ and $N_{\mathrm{D,B,p}}$). Notably, this effect is not covered by previous JFET modeling approaches [6, 7].

To obtain the trajectory through the calculated operating states, the anode current I_{A} is assumed to entirely flow through the JFET channels: (IV) $I_{\mathrm{A}} = I_{\mathrm{D,n}} = -I_{\mathrm{D,p}}$. Carefully considering the JFET operating states, I_{A} is calculated using a bisection-based optimization algorithm. The results of the error function $\Delta I = I_{\mathrm{D,n}} - |I_{\mathrm{D,p}}|$ shown in Fig. 5 (b), give rise to a distinct solution exhibiting minimum error for each SSCB operating point from conduction to blocking state. Transferring the trajectory of ΔI to Fig. 5 (a), the nJFET is found to saturate before the pJFET in the operating point $(V_{\mathrm{AS}}|V_{\mathrm{SK}}) \approx (13.5\ \mathrm{V}|2.5\ \mathrm{V})$. At $(V_{\mathrm{AS}}|V_{\mathrm{SK}}) \approx (200\ \mathrm{V}|23\ \mathrm{V})$, both JFET channels simultaneously are pinched off. Counterintuitively, the majority of V_{AK} drops over the nJFET ($V_{\mathrm{DS,n}} \gg |V_{\mathrm{DS,p}}|$) despite identical channel designs and the much lower ionization rate of acceptors and carrier mobility in the pJFET channel compared to the corresponding parameters in the nJFET channel. Again, this effect can be assigned to $N_{\mathrm{D,G,p}}$ and $N_{\mathrm{D,B,p}}$ having lower values than $N_{\mathrm{A,Ch,p}}$ accounted for in Eq. (2).

The breakdown characteristic can be calculated by applying the same approach as above stating I_{A} is flowing only across the JFET channels as depicted in Fig. 4 by the dashed line according to the assumption (V) $I_{\mathrm{A}} = -I_{\mathrm{G,n}} = I_{\mathrm{G,p}}$. Carefully considering JFET operating states that cause thermionic emission, space-charge-limited current or avalanche, respectively, the quasi-static output characteristics ($I_{\mathrm{A}}(V_{\mathrm{AK}})$) of the SSCB plotted in Fig. 6 are obtained. The family of curves represents a variation in $N_{\mathrm{A,Ch,p}}$. In the low voltage range, a linear correlation of I_{A} and V_{AK} is observed describing the on-state resistance (R_{on}). In this region, the SSCB is conducting the current during normal operation. The operating point in which the first JFET saturates, marks the characteristic trigger point of the investigated SSCB as the tipping point of the V_{DS}-V_{GS}-feedback loop is reached. Subsequently, the JFET channels progressively pinch off and by exceeding the SSCB pinch-off voltage (V_{po}), the SSCB is considered in blocking state. By further increasing V_{AK}, eventually, gate breakdown occurs as described above for the pJFET by either reaching the reach-through or avalanche voltage (V_{rt} or V_{aval}). As can be observed, R_{on}, the trigger current value (I_{trig}), V_{po} as well as V_{rt} are strongly affected by the variation of $N_{\mathrm{A,Ch,p}}$. Avalanche breakdown shows only a weak dependency in the investigated range of $N_{\mathrm{A,Ch,p}}$. Note, that with $N_{\mathrm{A,Ch,p}} = 2.7 \times 10^{17}\ \mathrm{cm}^{-3}$, the condition stated in Eq. (11) is not met anymore and avalanche occurs before reach-through. For $N_{\mathrm{A,Ch,p}} = 3.0 \times 10^{17}\ \mathrm{cm}^{-3}$, even V_{po} is higher than V_{aval} and, hence, the channels are not fully pinched off before the breakdown condition is met. The general trend observed in Fig. 6 agrees well

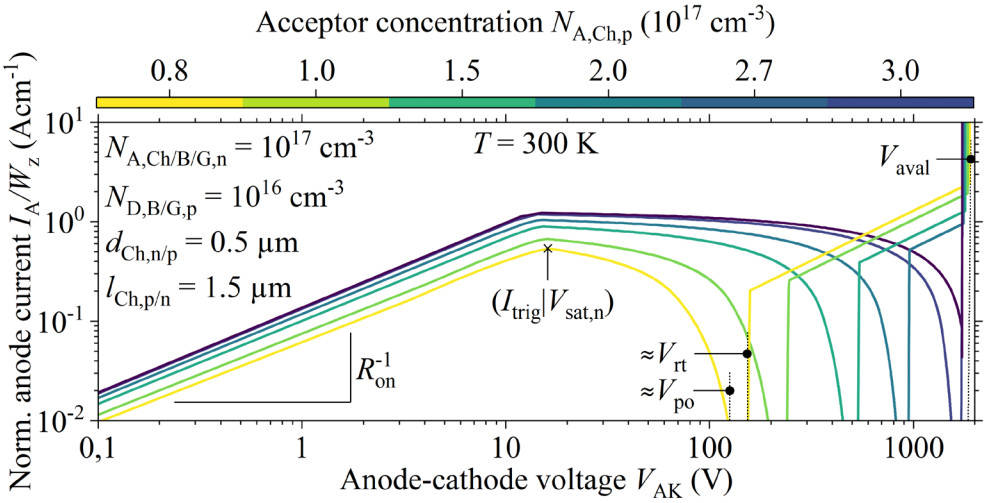

Fig.6. Output characteristics of the SSCB obtained from the proposed modelling approach. The family of curves represents a variation in $N_{A,Ch,p}$, where the curve for $N_{A,Ch,p} = 10^{17}$ cm^{-3} corresponds to the solution shown in Fig. 5.

with former investigations in TCAD as well as the electrical characteristics of the fabricated monolithically integrated SSCB prototypes [3, 4, 6].

Conclusion

In this work, an analytical modelling approach for the quasi-static operation of a novel SiC SSCB device is proposed. The model is solely motivated by physical parameters including the design parameters of the SSCB. Due to simplifications with respect to the actual SSCB device cell structure, the proposed model offers limited capabilities for quantitative predictions. Nevertheless, the general characteristics are in good agreement with experimental results of fabricated prototypes providing valuable insights in the working principle and design implications of this novel monolithically integrated two-pole SSCB [3-6]. Moreover, the model can be adapted to account for additional functionalities, such as the temporary current limiting mode offered by these devices [9].

References

[1] R. Rodrigues, et al., IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 364-377, Jan. 2021, doi: 10.1109/TPEL.2020.3003358.

[2] D. He, et al., IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1556-1565, Sept. 2019, doi: 10.1109/JESTPE.2019.2906661.

[3] N. Boettcher and T. Erlbacher, IEEE Electron Device Letters, vol. 42, no. 10, pp. 1516-1519, Oct. 2021, doi: 10.1109/LED.2021.3102935.

[4] N. Boettcher, et al, IEEE International Symposium on Power Semiconductor Devices and ICs, Vancouver, BC, Canada, 2022, pp. 261-264, doi: 10.1109/ISPSD49238.2022.9813628.

[5] N. Boettcher, et al. IEEE European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. P.1-P.9.

[6] N. Boettcher and T. Erlbacher, IEEE Workshop on Wide Bandgap Power Devices and Applications Asia, Suita, Japan, 2020, pp. 1-6, doi: 10.1109/WiPDAAsia49671.2020.9360279.

[7] Kimoto, T. and Cooper, J.A. (2014). Fundamentals of Silicon Carbide Technology, doi: 10.1002/9781118313534.

[8] J.L. Chu, G. Persky, S.M. Sze; Journal of Applied Physics, August 1972; 43 (8): 3510–3515, doi: 10.1063/1.1661745.

[9] T. Takamori, et al., IEEE Transactions on Industry Applications, June 2023 (early access), doi: 10.1109/TIA.2023.3288856.